EE2301: Lab Report 3

Building an 8- Hour Clock

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1 Objective

To build an 8- Hour Clock using D Flip-Flops.

2 Theory

2.1 D Flip-Flop

D Flip-Flop is an electronic device, which captures the data input (D) at the rising edge of the clock input (clk) and and then outputs (Q) the same input at the next rising edge of the clock input. The output does not depend on the current state of the DFF.
Here, $\overline{R}$ and $\overline{PR}$ are the asynchronous inputs to the DFF, which are active low. When R is low (0), the DFF will output low (0) irrespective of the clock and when PR is low (0), the DFF will output high (1), irrespective of the clock.
A set of 2 DFFs are packed into a single IC, *IC 7474*.

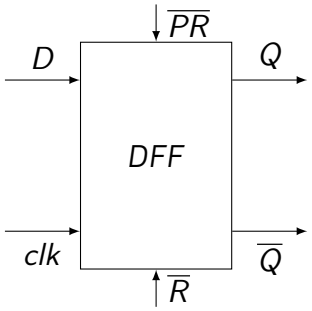

Figure 1: A typical DFF

The following is the state transition table of a DFF:

Current State ($Q(t)$)	Input (D)	Next State ($Q(t+1)$)	Output (Q)
0	0	0	0
0	1	1	1
1	0	0	0
1	1	1	1

Table 1.1: State Transition Table for D Flip-Flop

2.2 Counters

Counters are those devices which are used to count up or count down, by counting the number of times a certain edge of the clock in the flip- flop has occured.

They are usually of two types: Up counters, which count up from one number to another number and Down counters, which count down from one number to another.

Another classification of counters is given below.

Synchronous Counters

Synchronous counters are those counters where each flip-flop has the same clock signal. These counters are usually more reliable while they consume more space and require a large number of components.

Asynchronous Counters

Asynchronous counters are those counters where each flip-flop has a different clock signal. Usually, the output of a flip-flop is given as the clock input to the next flip-flop. These counters are less reliable but are space efficient.

Mod-10 Asynchronous Up Counters

Mod-10 Asynchronous Up Counters are those which count up from 0 to 9. 4 *DFF*s are required here, and the inverted output ($\overline{Q}$) is fed as the clock input to the next *DFF*. The output of the first *DFF* is the least significant bit (LSB) and the output of the last *DFF* is the most significant bit (MSB).
When the output of the *DFF*s read 10, i.e., 1010 in binary, we reset all the *DFF*s to make the counter a Mod-10 Counter. The reset signal *R* is the output of *NAND*ing Q_3, $\overline{Q_2}$, Q_1 and $\overline{Q_0}$.

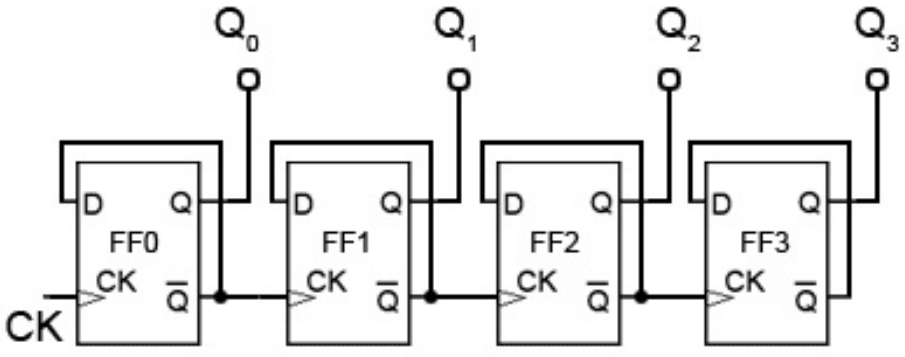

Figure 2: A Mod-10 Counter

Mod-6 Asynchronous Up Counters

Mod-6 Asynchronous Up Counters are those counters which count up from 0 to 5. 3 *DFF*s are required here, and the inverted output ($\overline{Q}$) is fed as the clock input to the next *DFF*. The output of the first *DFF* is the least significant bit (LSB) and the output of the last *DFF* is the most significant bit (MSB).
When the output of the *DFF*s read 6, i.e., 110 in binary, we reset all the *DFF*s to make the counter a Mod-6 Counter. The reset signal *R* is the output of *NAND*ing Q_2, Q_1 and $\overline{Q_0}$.

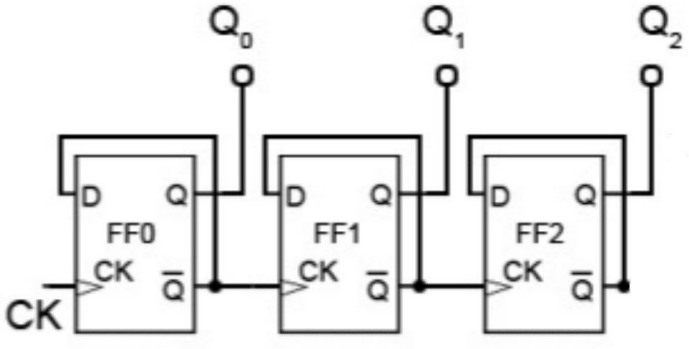

Figure 3: A Mod-6 Counter

The Mod-10 and Mod-6 counters are then cascaded twice to make a 60 minute clock, when the input clock signal is 1 Hz.

Mod-8 Asynchronous Up Counters

Mod-8 Asynchronous Up Counters are the counters which count up from 0 to 7. It is used to denote the hours in the clock which is being built. It has three *DFF*s cascaded in a similar manner as the previous counters and it requires three *DFF*s.
No reset signal is required as a typical 3 bit Asynchronous Counter is a Mod-8 counter.
The inverted output of the last *DFF* of the minutes clock is fed as clock signal to the Mod-8 Counter.

2.3 BCD to 7 Segment Decoder

A BCD to 7 Segment Decoder (*IC* 7447) is used to convert the outputs of the *DFF*s into a set of signals corresponding to each segment of the 7 Segment Display.
Each Counter is connected to a decoder, which then is connected to a 7 Segment Display which displays the time.

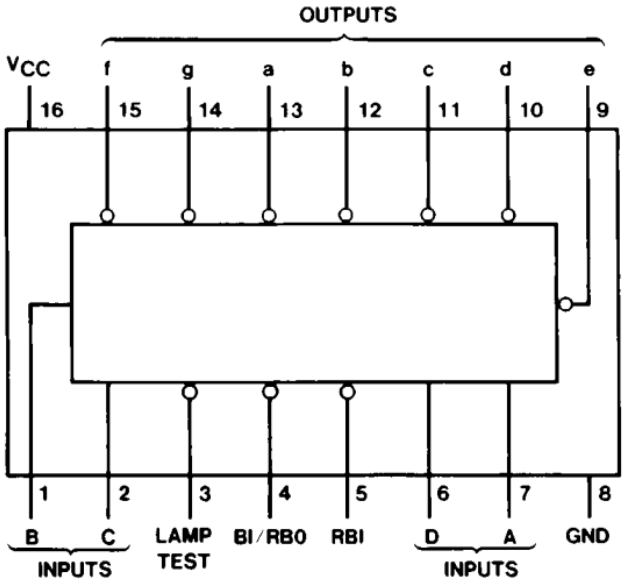

Figure 4: Pinout of a typical *IC* 7447

2.4 7 Segment Display

7 Segment Display is one of the most commonly used electronic component. it has 7 inputs and a V_{cc} input, each corresponding to one segment of the display. Corresponding output of the 7447 *IC* is taken as input to each of the 7 Segment Display's segments.

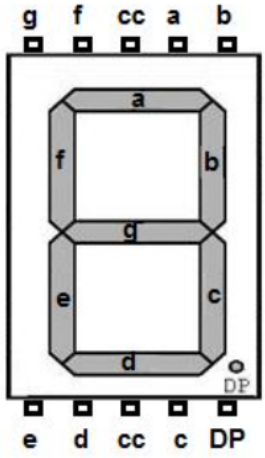

Figure 5: Pinout of a typical 7 Segment Display

3 Observations

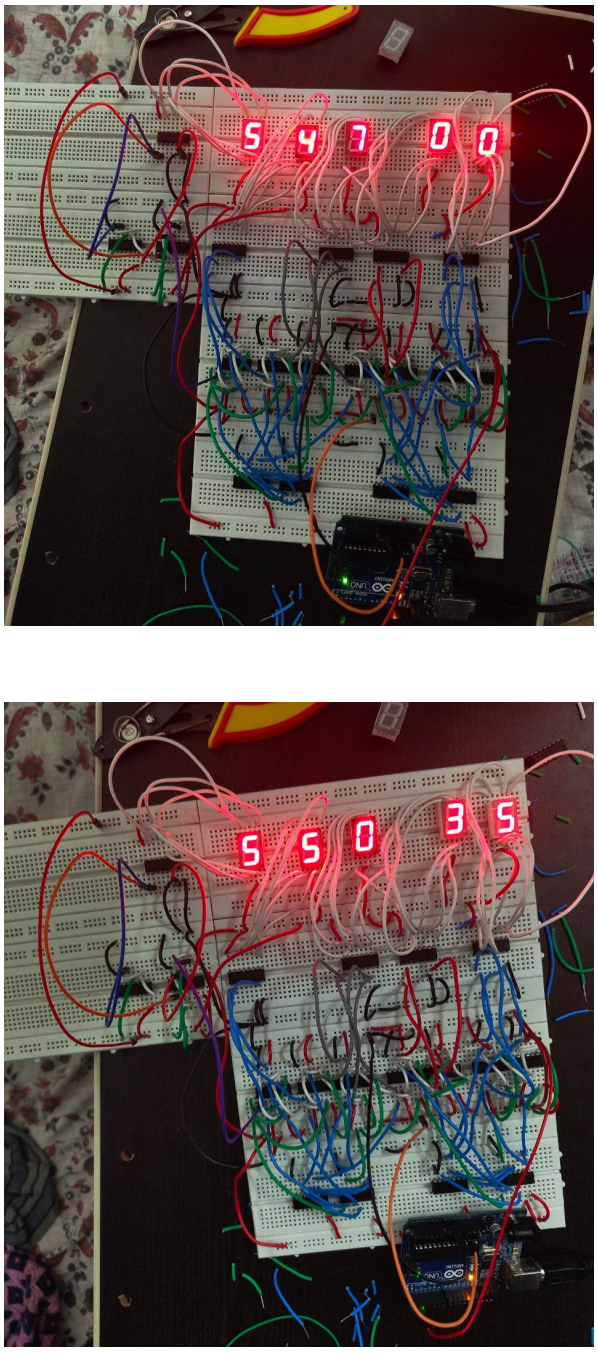

Figure 6: A few pictures of the working Clock Circuit

4 Sources of Error

1. Many wires had loose connections, which had to be taken care of constantly.
2. The ICs were malfunctioning all the time.
3. The jumper wires were constantly deforming, leading to them getting stuck in the breadboard or making them unusable.
4. Connecting many components to a single IC led to its malfunction, owing to Loading Effect.
5. Moving the Circuit, even by a small amount, at times led to the clock not working effectively.

5 Conclusion

An 8- Hour Clock was successfully built.