BHUYASHI DEKA

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Education

University of Wisconsin - Madison Sept 2024 - May 2026
Master of Science, Computer Science Madison, US
Courses: High Performance Computing, Computer Vision, Computer Graphics, Artificial Intelligence

Indian Institute of Technology, Bombay Jul 2016 - Aug 2021
Master & Bachelor of Technology, Electrical Engineering Mumbai, India
Courses: Processor Design, Computer Architecture, Digital Signal Processing, Probability & Statistics

Work Experience

Samsung Semiconductor India Research Bangalore, India
Hardware-Software Codesign: Computer Vision Jul 2021 - Aug 2024

- Implemented a **temporal denoising** engine using wavelet transform for 2× downscaling, neural engine for weight map estimation & bilinear interpolation for upscaling, achieving 30% noise reduction on real-time video application
- Worked on **dense optical flow** engine to reduce motion artefacts by 25% using vector maps between two frames
- Developed a **decision tree** and **neural network** model using **PyTorch** to replace the in-house SRAM memory area estimation tool; achieved 99.1% and 96.2% accuracy respectively, improving runtime performance by nearly 100x
- Designed a novel **Gamma Correction** architecture, reducing IP area logarithmically by 20% and chip area by 15%
- Automated the performance and area estimation for **PPA** analysis effectively reducing man hours by 50%
- Built an automation engine to streamline tool workflows using **Python** and **csh** with a **PyQt**-designed GUI; integrated tool setup and error reporting, which improved efficiency by 75% and reduced result review time by 90%

Power Management IC Design - Intern May 2019 - Jul 2019

- Designed behavioral model for Power Management IC like oscillators, dropout regulators, buck-boost converters
- Automated code generation using Perl; analyzed VerilogA, SystemVerilog, schematic models & created testbenches

Projects

RISC Processor Design *IIT Bombay*

- Implemented an 8-register, 16-bit, 5-stage pipelined RISC processor for a custom ISA of 15 instructions in **Quartus**
- Employed forwarding and hazard mitigation units to make the design entirely free of data and control hazards

Multi-agent RAG Debate Simulation Chatbot using LangGraph *UW-Madison*

- Developed a multi-agent RAG system using **LangGraph** and **WolframAlpha** API with FOR/AGAINST subgraphs
- Integrated Analyzer, Debator, Researcher & Refiner agents simulating evidence-based debates with real-time

Diffusion Models for Image Synthesis *UW-Madison*

- Developed a **UNet** model for image synthesis incorporating sinusoidal time embeddings and cross-attention
- Applied **latent diffusion** for iterative denoising, high-quality image reconstruction and generative modeling

Unsupervised Domain Adaptation for Semantic Segmentation *UW-Madison*

- Designed a **test-time** domain adaptation model to improve semantic segmentation on out-of-distribution data
- Dynamically adapted **batch normalization** during inference to handle domain-specific changes sans extra training

Research Experience

Spatio-Temporal Noise Reduction Algorithm for Low-end devicess *Samsung Semiconductor*

- Developed a light-weight denoising algorithm for low-end Samsung phones for the price-sensitive market
- Enhanced Non-Local Means algorithm using noise estimation, adaptive smoothing, and total variation minimization
- Presented the work at the Samsung Semiconductor India RnD TechCon 2023 and was awarded the **best paper**

Efficient architecture for 3D CNN Acceleration *Master's Thesis, IIT Bombay*

- Explored hardware architectures to efficiently run convolutional neural networks, improving **resource utilization**
- Implemented depthwise convolution, optimized looping and tiling order to reduce hardware and align it to dataflow

Skills

Languages: C, C++, Python, Assembly, Verilog, VHDL, SQL, JavaScript, MATLAB
Libraries & Tools: Keil, ModelSim, Magillem, Docker, git, Linux, PyTorch, OpenCV, CUDA, OpenMP, OpenGL
Boards: DE0-Nano FPGA, Raspberry Pi 3, Arduino, Tiva-C