

# BHUYASHI DEKA

☎ (608) 658-5211 | ✉ [bdeka@wisc.edu](mailto:bdeka@wisc.edu) | [in bhuyashi-deka](https://www.linkedin.com/in/bhuyashi-deka) | [github.com/Bhuyashi](https://github.com/Bhuyashi)

## EDUCATION

### University of Wisconsin - Madison

Master of Science, Computer Science

Sept 2024 - May 2026

Madison, US

Courses: Computer Vision, Computer Graphics, Artificial Intelligence

### Indian Institute of Technology, Bombay

Master & Bachelor of Technology, Electrical Engineering

Jul 2016 - Aug 2021

Mumbai, India

Courses: Processor Design, Computer Architecture, Digital Signal Processing, Probability & Statistics

## WORK EXPERIENCE

### Samsung Semiconductor India Research

Jul 2021 - Aug 2024

Hardware-Software Codesign: Computer Vision

Bangalore, India

- Developed a **temporal denoising** engine for weighted averaging of consecutive frames using wavelet transform for frame downscaling, neural engine-based weight map estimation, and bilinear interpolation for upscaling weight map
- Worked on **Dense Optical Flow** engine to reduce image motion artefacts by estimating vector maps between two frames
- Developed a **decision tree** and **deep learning** model to replace the in-house SRAM memory area estimation tool, achieving 99.1% and 96.2% accuracy respectively, while improving runtime performance by nearly 100x
- Designed and developed a novel architecture for **Gamma Correction** which is a recurring algorithm in the imaging pipeline
- Built an automation engine using **Python** and **csh** with a **PyQt**-designed GUI to streamline tool workflows, integrating tool setup, execution, and error reporting, which improved efficiency by 75% and reduced result review time by 90%
- Automated the performance and area estimation process for **PPA** analysis effectively reducing man hours by 50%
- Received the **Spotlight Award** three times in a span of two years for exceptional performance and contributions to the team
- Promoted to Associate Staff Engineer position for showcasing strong technical skills and exemplary work

Power Management IC Design - Intern

May 2019 - Jul 2019

- Designed behavioral model for Power Management IC modules like oscillators, dropout regulators, buck-boost converters
- Automated code generation using **Perl**; analyzed **VerilogA**, **SystemVerilog**, and schematic models, and created testbenches

### Intello Labs

Dec 2018 - Jan 2019

Data Analytics - Intern

Mumbai, India

- Compiled a dataset from manually collected invasive sugar level measurements to fine-tune a non-invasive medical device
- Analyzed the data collected and fit a **polynomial regression** curve to the device parameters to improve its prediction

## RESEARCH EXPERIENCE

### Spatio-Temporal Noise Reduction Algorithm for Low-end devices

Samsung Semiconductor

- Developed a light-weight spatio-temporal denoising algorithm for low-end Samsung phones for the price-sensitive sector
- Enhanced the **non-local means** algorithm by using noise estimation, adaptive smoothing, and total variation minimization
- Presented the work at the Samsung Semiconductor India RnD TechCon 2023 and was awarded the **best paper**

### Efficient architecture for 3D CNN Acceleration

Master's Thesis, IIT Bombay

- Experimented with hardware architectures to efficiently run **convolutional neural networks**, improving resource utilization
- Implemented depthwise convolution, optimized looping and tiling order to reduce hardware and align it to data flow

## PROJECTS

### Surveillance video people detection and counting

IIT Bombay

- Developed a people-tracking system using background subtraction, image cleaning, and bounding boxes for object detection
- Trained an **SVM** with Aggregate Channel Features and optimized sliding window stride to reduce over-counting

### Comparative Analysis of Pathfinding Algorithms

IIT Bombay

- Developed a maze generation system using depth-first search to simulate real-time pathfinding with visual representation
- Implemented multiple algorithms like **A\***, **DFS**, **BFS** in Python to compare their efficiency on dynamically generated mazes

## SKILLS

**Languages:** Python, C, C++, SystemVerilog, VHDL, Assembly, SQL, JavaScript, MATLAB

**Libraries & Tools:** PyTorch, TensorFlow, OpenCV, Numpy, Scikit, Pandas, Matplotlib, OpenGL, git, Linux

**Boards:** DE0-Nano FPGA board, Raspberry Pi 3, Arduino, Tiva-C