EE 789
Assignment 1: RTL assignment
Due on 1/9/2022

August 25, 2022

1. Install docker and verify the installation.

2. The shift and add multiplier VHDL implementation has been shared with you via Moodle. Run the testbench and confirm correctness of the implementation using GHDL simulation. For more information on GHDL, see the GHDL Main/Home Page at http://ghdl.free.fr.

3. Design a shift and subtract (long-division) 8-bit divider in RTL. You may assume the same interface as in the shift and add multiplier shared with you. The inputs A and B may be assumed to be non-negative integers. Given A, B, if the result is Q, then $A = (B \times Q) + R$, where R is an integer $< B$. You may assume that $B \neq 0$.

   (a) Work out the pseudo code.

   (b) Implement in VHDL, and verify using a testbench (adapt the testbench shared with you for the shift and add multiplier).