Name: _____ Section: _____

Cache Memory Problem Set: (Answer #7 first)

0. A cache contains 4 blocks. The main memory contains 16 blocks. Each block is 2 words. Each word is 16-bit.
    a. How many bits are there in a main memory address?
    b. In the main memory address, how many bits are there in each of the TAG, BLOCK and WORD fields (direct)?
    c. In the main memory address, how many bits are there in each of the TAG and WORD fields (full associative)?
    d. In the main memory address, how many bits are there in each of the TAG, SET and WORD fields (block set associative; 2 blocks /set)
    e. What is the size of the cache memory (in bits) assuming direct-mapping?
    f. What is the size of the cache memory (in bits) assuming full associative mapping?
    g. What is the size of the cache memory (in bits) assuming block set associative with 2 blocks per set?
    h. What is the size of the main memory (in bits)?
    i. In which cache block will memory block 9 blocks be mapped (direct mapping)?
    j. In which cache block will memory address 9 be mapped (direct mapping)?
    k. In which cache set will memory block 9 blocks be mapped (block set associative mapping)?
    l. In which cache set will memory address 9 be mapped (block set associative mapping)?
    m. Given the following main memory block access: 1,7,5,0,2,1,3,6,1,3,4,7,9 and assuming that cache access time is 1ns and memory access time is 10ns.
        i. Show the cache memory (direct-mapped) after memory blocks are accessed
        ii. Compute for the total time needed for the instruction during execution of the program
        iii. Show the cache memory (Full associative+LRU) after memory blocks are accessed
        iv. Compute for the total time needed for the instruction during execution of the program
        v. Show the cache memory (Full associative+MRU) after memory blocks are accessed
        vi. Show the cache memory (Block set Associative+LRU) after memory blocks are accessed
        vii. Compute for the total time needed for the instruction during execution of the program
        viii. Compute for the total time needed for the instruction during execution of the program
1. A direct-mapped cache consists of a total of 64 blocks. The main memory contains 4096 blocks, each consisting of 128 words. Each word is 16-bit.
    a. How many bits are there in a main memory address?
    b. In the main memory address, how many bits are there in each of the TAG, BLOCK and WORD fields?
    c. What is the size of the cache memory?
    d. What is the size of the main memory?
    e. In which cache block will memory block 1000 blocks be mapped?
    f. In which cache block will memory address 1000 be mapped?
2. An associative cache consists of a total of 64 blocks. The main memory contains 4096 blocks, each consisting of 128 words. Each word is 16-bit.
    a. How many bits are there in a main memory address?
    b. In the main memory address, how many bits are there in each of the TAG and WORD fields?
    c. In which cache block will memory block 1000 blocks be mapped?
    d. In which cache block will memory address 1000 be mapped?
3. A 4-way block set associative cache consists of a total of 64 blocks. The main memory contains 4096 blocks, each consisting of 128 words. Each word is 16-bit.
    a. How many bits are there in a main memory address?
    b. In the main memory address, how many bits are there in each of the TAG, SET, and WORD fields?
    c. In which cache set will memory block 1000 blocks be mapped?
    d. In which cache set will memory address 1000 be mapped?

4. A byte-addressable computer has a small data cache capable of holding 32 bytes. Each cache block consists of 4 bytes. When a given program is executed, the processor reads data from the following sequence of hex addresses:

    200, 204, 208, 20C, 2F4, 2F0, 200, 204, 218, 21C, 24C, 2F4

    a. Show the contents of the cache if a direct mapped cache is used. Assume that the cache is initially empty.
    b. Repeat part (a) for an associative-mapped cache that uses the LRU replacement algorithm
    c. Repeat part (a) for a four-way block-set associative cache

5. A computer system has a main memory consisting of 1Mwords. It also has a 4K-word cache organized in the block-set-associative manner, with 4 blocks per set and 64 words per block.
    a. Calculate the number of bits in each of the TAG, SET, and WORD fields of the main memory address format.
    b. Suppose that the processor fetches 4352 words from locations 0,1,2, …, 4351, in that order. It then repeats this fetch sequence nine more times. Cache access time is 1 ns. Memory access time is 10 ns. Compute for the total time needed for the instruction fetch during execution of the program if there is NO cache memory.
    c. Assume that the cache is initially empty. Suppose that the processor fetches 4352 words from locations 0,1,2, …, 4351, in that order. It then repeats this fetch sequence nine more times. Cache access time is 1 ns. Memory access time is 10 ns. Compute for the total time needed for the instruction fetch during execution of the program assume cache memory is used. Assume that the LRU algorithm is used for block replacement.
6. A program consists of two nested loops (see figure below) is to be run on a computer that has a direct mapped cache with the following parameters: MM memory size: 64Kwords, cache size = 1Kwords, block size = 128 words; memory access time is 10ns and the cache access time is 1ns.
    a. Specify the number of bits in the TAG, BLOCK, and WORD fields in the main memory addresses
    b. Compute the total time needed for the instruction fetch during execution of the program (address in decimal)