0. A cache contains 4 blocks. The main memory contains 16 blocks. Each block is 2 words. Each word is 16-bit.
   a. How many bits are there in a main memory address?
      16 blocks * 2 words = 32 (2^5) -> 5 bits
   b. In the main memory address, how many bits are there in each of the TAG, BLOCK and WORD fields(direct)?
      2,2,1
   c. In the main memory address, how many bits are there in each of the TAG, SET and WORD fields (block set associative; 2 blocks /set)
      3,1,1
   d. What is the size of the cache memory (in bits) assuming direct-mapping? 140 bits
   e. What is the size of the cache memory (in bits) assuming full associative mapping? 148 bits
   f. What is the size of the cache memory (in bits) assuming block set associative with 2 blocks per set? 144 bits
   g. What is the size of the main memory (in bits)? 512 bits
   h. In which cache block will memory block 9 blocks be mapped (direct mapping)? 9 mod 4 = block 1
   i. In which cache block will memory address 9 be mapped (direct mapping)?
      9 -> 1001
      01 00 1 -> block 0
   j. In which cache set will memory block 9 blocks be mapped (block set associative mapping)?
      cache sets = 4 blocks in cache / 2 blocks per set
      9 mod 2 = set 1
   k. In which cache set will memory address 9 be mapped (block set associative mapping)?
      9 -> 1001
      0010 0 1 -> set 0
   l. Given the following main memory block access: 1,7,5,0,2,1,3,6,1,3,4,7,9 and assuming that cache access time is 1ns and memory access time is 10ns.
      i. Show the cache memory (direct-mapped) after memory blocks are accessed

Seq	Hit	Miss	Block
1		1	1
7		7	3
5		5	1
0		0	0
2		2	2
1		1	1
3		3	3
6		6	2
1	1		1
3	3		3
4		4	0
7		7	3
9		9	1

Block	Data
0	0,4
1	1,5,1,9
2	2,6
3	7,3,7

Block	Data
0	4
1	9
2	6
3	7

Cache Memory

      ii. Compute for the total time needed for the instruction during execution of the program
      Total access time: 2*2*1 + 11*2*11 + 11*1 = 257ns
      iii. Show the cache memory (Full associative+LRU) after memory blocks are accessed

Seq	Hit	Miss	Block
1		1	0
7		7	1
5		5	2
0		0	3
2		2	0
1		1	1
3		3	2
6		6	3
1	1		
3	3		
4		4	0
7		7	3
9		9	1

Block	Age	Data
0	2	1,2,4
1	0	7,1,9
2	3	5,3
3	1	0,6,7

Block	Data
0	4
1	9
2	3
3	7

Cache Memory

      iv. Compute for the total time needed for the instruction during execution of the program
      Total access time: hit*words*cat + miss*words*(mat+1) = 2*2*1 + 11*2*11 + 11*1 = 257ns
      v. Show the cache memory (Full associative+MRU) after memory blocks are accessed

Seq	Hit	Miss	Block
1		1	0
7		7	1
5		5	2
0		0	3
2		2	3
1	1		
3		3	0
6		6	0
1		1	0
3		3	0
4		4	0
7	7		
9		9	1

Block	Last	Data
0		1,3,6,1,3,4
1	1	7,9
2		5
3		0,2

Block	Data
0	4
1	9
2	5
3	2

Cache Memory

vi. Show the cache memory (Block set Associative+LRU) after memory blocks are accessed

Seq	Hit	Miss	Set
1		1	1
7		7	1
5		5	1
0		0	0
2		2	0
1		1	1
3		3	1
6		6	0
1	1		1
3	3		1
4		4	0
7		7	1
9		9	1

Set	Block 0	Block 1
0	0,6	2,4
Age	1	0
1	1,5,3,9	7,1,7
Age	0	1

Set	Block 0	Block 1
0	6	4
1	9	7

Cache Memory

vii. Compute for the total time needed for the instruction during execution of the program
Total access time: 2*2*1 + 11*2*11 + 11*1 = 257ns