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Design and Synthesis of Carry Lookahead Adders

Aim:

- To model a 4-bit Carry Lookahead Adder using Dataflow modeling.
- To compile, simulate and plot the results using Xilinx ISE Tools.
- To implement the proposed systems using Xilinx Tools and generate the synthesis report.

Software used:

Xilinx ISE Tools

Functional Description:

Full Adder:

Truth Table

A	B	Carry-in	Sum	Carry-out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Boolean Equation:
Inputs: A, B & Cin

Outputs: Carry generate: Gi= A(i) & B(i)

Carry propogate: Pi= A(i) ^ B(i)

Sum: Si= P(i) ^ C(i)

Carry output: C(i+1)= G(i)+P(i) &C(i)

where i-bit position

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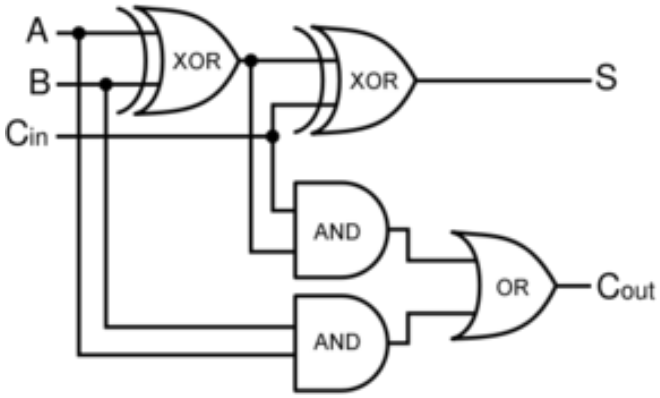
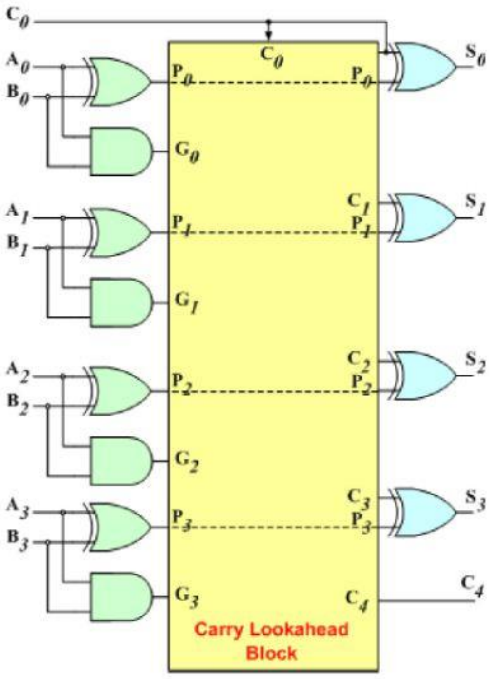
Full adder:

Block Diagram:

Logic Diagram:



4-Bit Carry Lookahead Adder:



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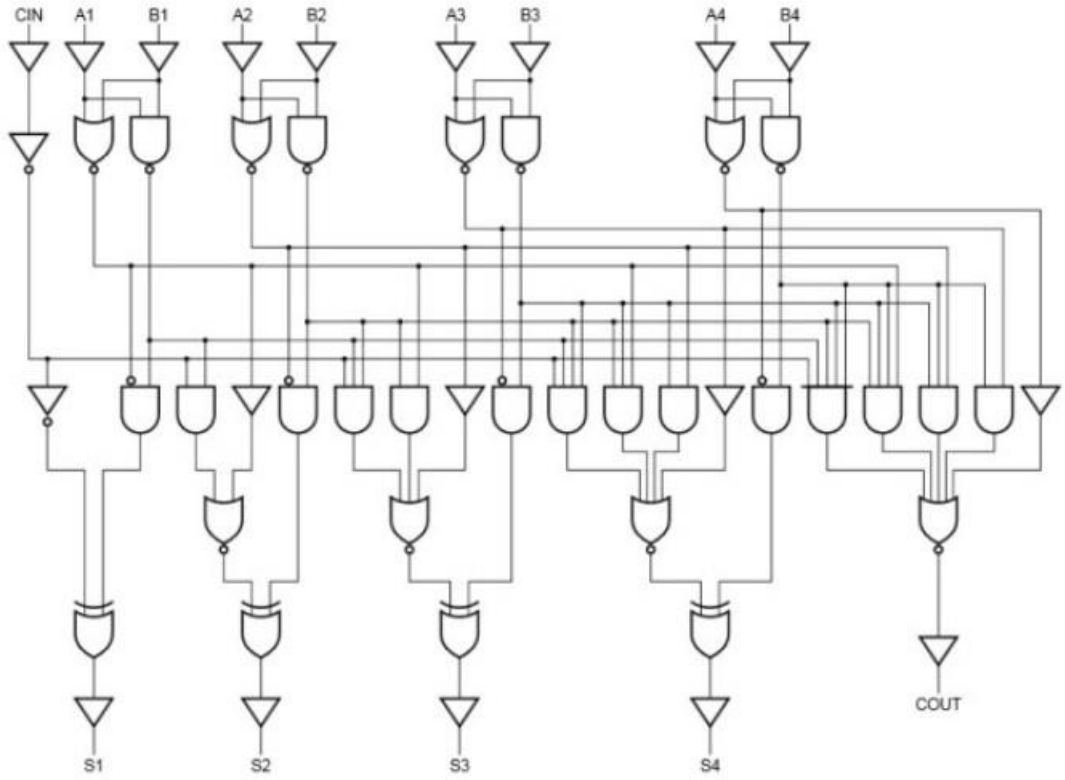
Schematic Diagram:
4-Bit Carry Lookahead Adder:



Modeling using Verilog HDL:
4-Bit Carry Lookahead Adder:
Design module:

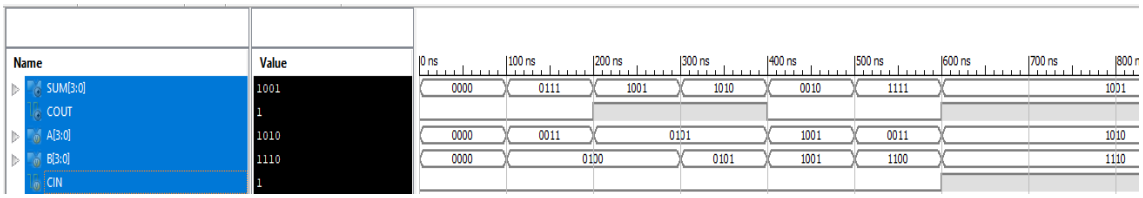
```
module CLA_Adder(a,b,cin,sum,cout);
input[3:0] a,b;
input cin;
output[3:0] sum;
output cout;
wire[3:0] p,g,c;
assign p[3:0]=a[3:0]^b[3:0];
assign g[3:0]=a[3:0]&b[3:0];
assign c[0]=cin;
assign c[3:1]=g[2:0]|(p[2:0]&c[2:0]);
assign cout=c[3];
assign sum[3:0]=p[3:0]^c[3:0];
```

```
endmodule
```

Stimulus file:

```
module test_cla;
        // Inputs
        reg [3:0] A;
        reg [3:0] B;
        reg CIN;
        // Outputs
        wire [3:0] SUM;
        wire COUT;
        // Instantiate the Unit Under Test (UUT)
        CLA_Adder uut(A,B,CIN,SUM,COUT);
        //Print statement
        initial begin
                $monitor($time," A= %b,B=%b,CIN= %b,COUT= %b, SUM= %b",A,
B, CIN, COUT, SUM);
        end
initial begin
                A = 4'd0; B = 4'd0; CIN = 1'b0;
                #100 A= 4'd3; B= 4'd4;
                #100 A= 4'd3; B= 4'd4;
                #100 A = 4'd5; B = 4'd5;
                #100 A = 4'd9; B = 4'd9;
                #100 A = 4'd3; B= 4'd12;
                #100 A = 4'd10; B = 4'd14; CIN = 1'b1;
end
endmodule
```

Simulation Results:



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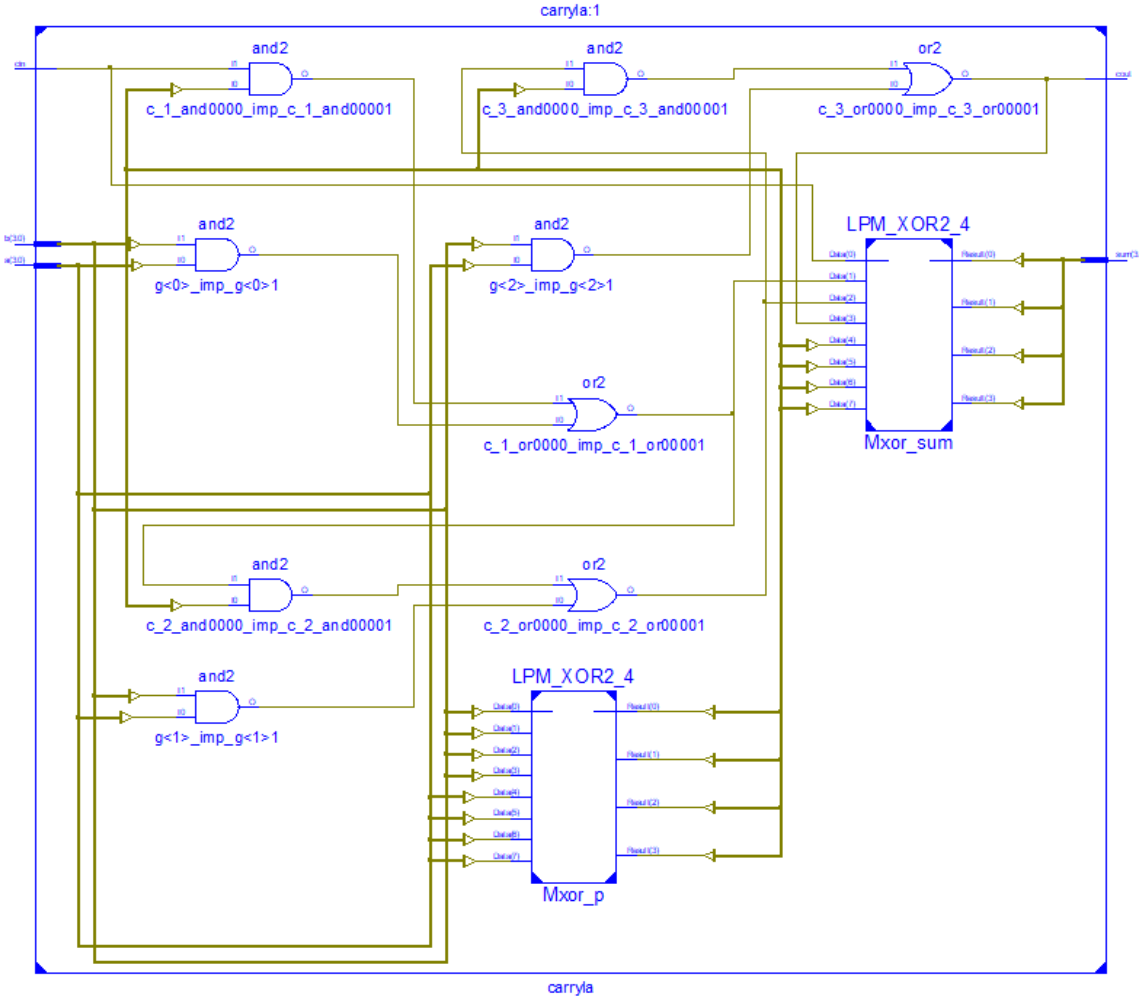
RTL Schematic Diagram:



Design Summary:

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of 4 input LUTs	7	4,896	1%
Number of occupied Slices	5	2,448	1%
Number of Slices containing only related logic	5	5	100%
Number of Slices containing unrelated logic	0	5	0%
Total Number of 4 input LUTs	7	4,896	1%
Number of bonded IOBs	14	158	8%
Average Fanout of Non-Clock Nets	1.63		

Result:

Thus, a model for 4-bit Carry Lookahead Adder using Dataflow modelling was compiled, simulated, synthesized, and implemented.