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Study of Xilinx FPGA Trainer Kit

Aim:
To Study the Xilinx FPGA Trainer Kit

Software used:
Xilinx ISE Tools

Kit Specifications:

1.1 FPGA Specifications:

Hardware:
Family: Spartan3E
Device: XC3S250E
Package: PQ208
Speed Grade: -4

1.2 Software:
Synthesis Tool: XST (VHDL/Verilog)
Simulator: ISE Simulator (VHDL/Verilog)

2. Other hardware:

2.1 Clock Generation:
The trainer kit has two clock sources:

- Fixed clock of 4MHz connected to PIN No: 181
- Manual clock by push-to-on switch connected to PIN No: 178. When the key is pressed once, one positive going pulse will be applied to the clock pin of FPGA.

2.2 Input Signal Generation:
The input signal level is generated using DIP switches. The DIP-switch has 8 separate switches. The switch diagram is shown below:

Switch S2								
Signal	S2-1	S2-2	S2-3	S2-4	S2-5	S2-6	S2-7	S2-8
Pin	159	169	174	175	183	184	194	204

Switch S3								
Signal	S3-1	S3-2	S3-3	S3-4	S3-5	S3-6	S3-7	S3-8
Pin	159	169	174	175	183	184	194	204

When the switch is ON position the output will be ‘0’ level, which is fed to FPGA
as input. When the switch is OFF position the output of this will be ‘1’ level.
The ‘RC’ is used to limit the current, while connecting to ground point.

2.3 Output’s:

The FPGA device outputs are connected to bar-graph LEDs which shows the output level. The output is ‘1’ level the LED will be glowing and when the output is at ‘0’ level the LED will be in off.

2.4 Bi-directional Lines:

The PIN Nos. 106, 107, 108, 109, 112, 113, 115 & 116 of FPGA can be used as bi-directional, in which the output can be viewed at DS7 and the input can be set by switch S1. The circuit diagram of single line is given below:

Switch S1								
Signal	S1-1	S1-2	S1-3	S1-4	S1-5	S1-6	S1-7	S1-8
Pin	106	107	108	109	112	113	115	116

2.5 Edge Triggered Signals:

PIN Nos. 126, 127 and 128 are connected to push-to-on switches, which generate a positive going pulse.

2.6 Keyboard:

The trainer kit has a 4*4 key matrix connected to the FPGA I/O lines. The connection details are given below:

Scan Lines	
SC0	123
SC1	122
SC2	120
SC3	119

Return Lines	
RT0	137
RT1	138
RT2	139
RT3	140

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2.7 Seven Segment Display:

The trainer kit has 4 digit seven segment displays, which are multiplexed. The connection detail is given below.

7-segment display select lines	
DS1	119
DS2	120
DS3	122
DS4	123

Segments	
A	144
B	145
C	146
D	147
E	150
F	151
G	152
DP	153

2.8 LCD:

The trainer kit has one 16*2 LCD display. The connection details are given below:

LCD Control Signals			
Signal	RS	R/W	EN
Pin	55	61	62

LCD Data lines								
Signal	D0	D1	D2	D3	D4	D5	D6	D7
Pin	63	64	65	68	69	76	89	90

RS - LCD Register Select Signal

R/W - LCD Read / Write Signal

EN - LCD Enable Signal

D7-D0 - LCD Data Lines

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2.9 26-pin FRC Lines:

FRC Pin	1	2	3	4	5	6	7	8	9	10	11	12	13
FPGA Pin	2	3	4	5	8	9	11	12	15	16	18	19	33
FRC Pin	14	15	16	17	18	19	20	21	22	23	24	25	26
FPGA Pin	34	35	36	39	40	41	42	45	47	129	132	+5 V	GND

FPGA Kit Interfacing Diagram:

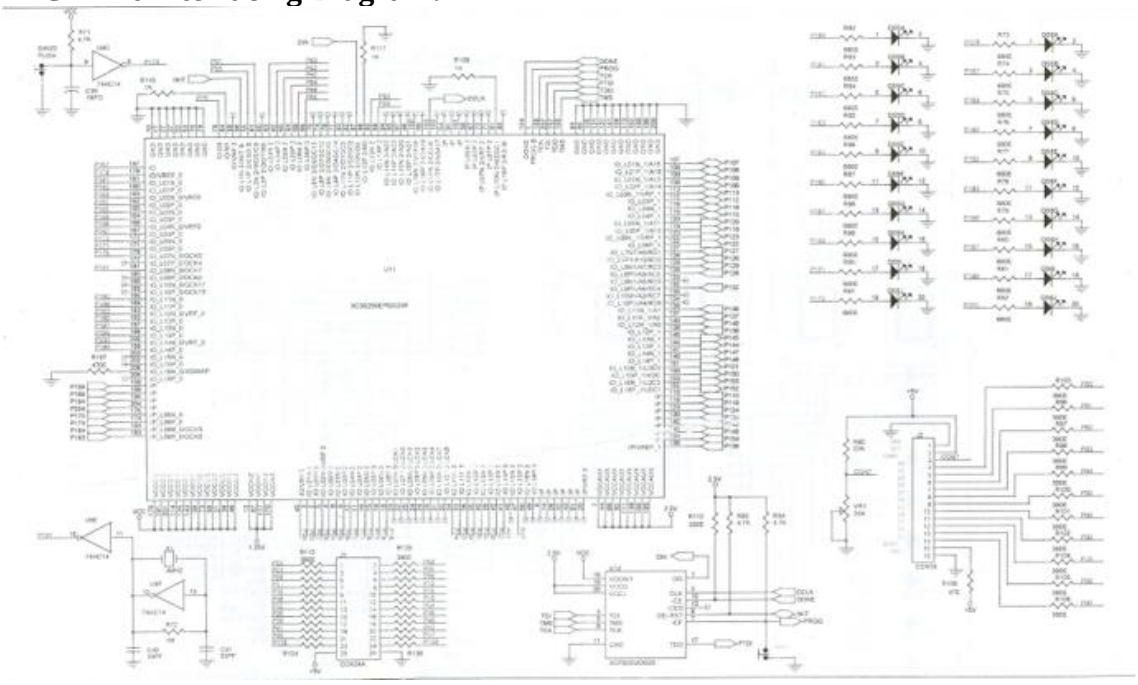

Fig. 1 – FPGA Spartan3E-250K

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XILINX SPARTAN 3E TRAINER KIT SPECIFICATIONS
Model No: VSK-SPARTAN 3E

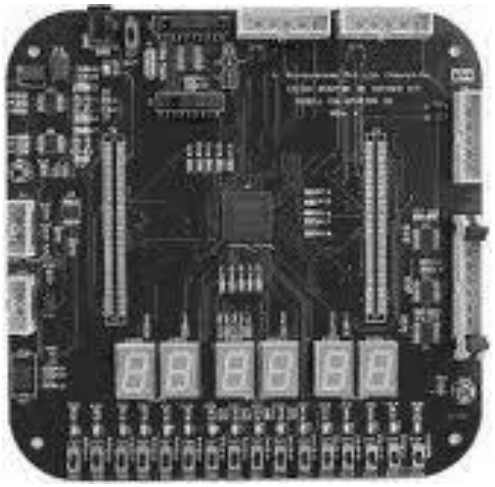

Fig. 2 – FPGA Spartan3E-500K

Key components and features:
Family: **Xilinx Spartan3E FPGA**
Device: **XC3S500E**
Package: **FT256**
Speed Grade: **-4**
16 Nos. of digital input using slide switches
16 Nos. of digital output using discrete LEDs FPGA configuration through

- JTAG port
- Slave serial
- Onboard Flash PROM XCFO4S

Onboard programmable oscillator from 3 MHz to 200 MHz

16 Nos. of digital input using slide switches:

Input switches								
Switches	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11
FPGA Pin	T14	T12	T9	T7	T2	G12	H1	R3
Switches	SW12	SW13	SW14	SW15	SW16	SW17	SW18	SW19
FPGA Pin	N11	N3	M13	M7	M3	K4	J12	J11

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16 Nos. of digital output using discrete LEDs

Output LEDs								
LEDs	L1	L2	L3	L4	L5	L6	L7	L8
FPGA Pin	P14	T13	R13	P13	N12	N9	P12	N10
LEDs	L9	L10	L11	L12	L13	L14	L15	L16
FPGA Pin	R10	T8	R6	T5	T4	K3	R2	R1

Result:

Hence the Xilinx FPGA Trainer Kit has been studied and been familiarized with.