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Ex No: 04
Date: 13.09.2024

DESIGN OF CMOS D-FLIP FLOP

AIM:

To design and implement a D-Flip Flop using Cadence Virtuoso 90nm CMOS technology

TOOLS REQUIRED:

Cadence Virtuoso Analog Design Environment

PROCEDURE:

- Open Virtuoso and create a new library with existing gpdk090nm technology.
- File -> New -> Cellview -> Schematic
- With the help of the circuit diagram, implement the D-Flip Flop using cmos by adding instances and connect the instances using wire
- Add the source and ground to the required pins
- Complete the circuit with the wireconnections
- Launch ->ADE L
- Choose Transient analysis
    - Set the stop time
    - Click on moderate
- Select input and output pins from the design by clicking on the corresponding wires
- Then run the simulation process to get the transient response
- Thus, the pre layout simulation results are obtained

CIRCUIT DIAGRAM AND TRUTH TABLE:

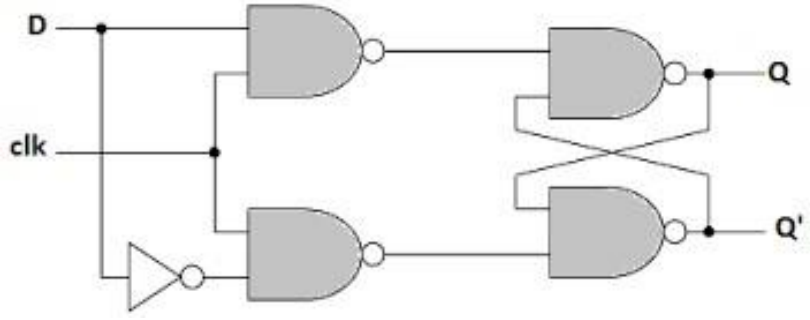

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Fig 4.1 Circuit diagram of CMOS D-Flip Flop

clk	D	Q	$\overline{Q}$
0	0	Q	$\overline{Q}$
0	1	Q	$\overline{Q}$
1	0	0	1
1	1	1	0

Table 4.1 Truth Table for D-Flip Flop

TRANSIENT ANALYSIS:

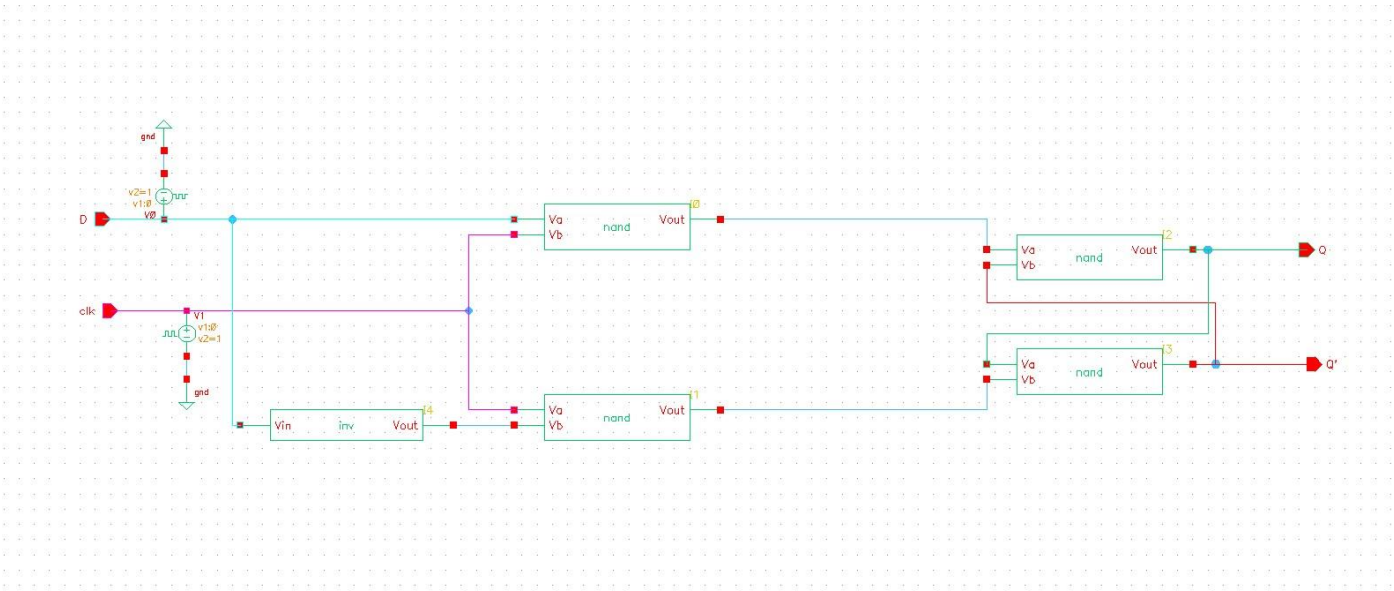

Fig 4.2 Schematic diagram of CMOS D-Flip Flop

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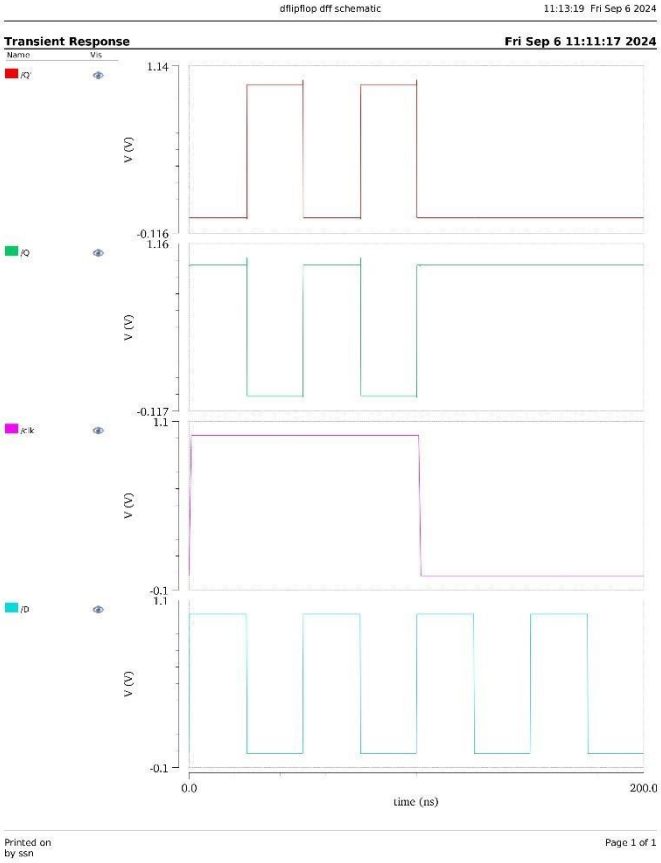

Fig 4.3 Transient Analysis of CMOS D-Flip Flop

RESULT:

Thus, the CMOS based D-Flip Flop was implemented and verified using Cadence Virtuoso Analog Design Environment.