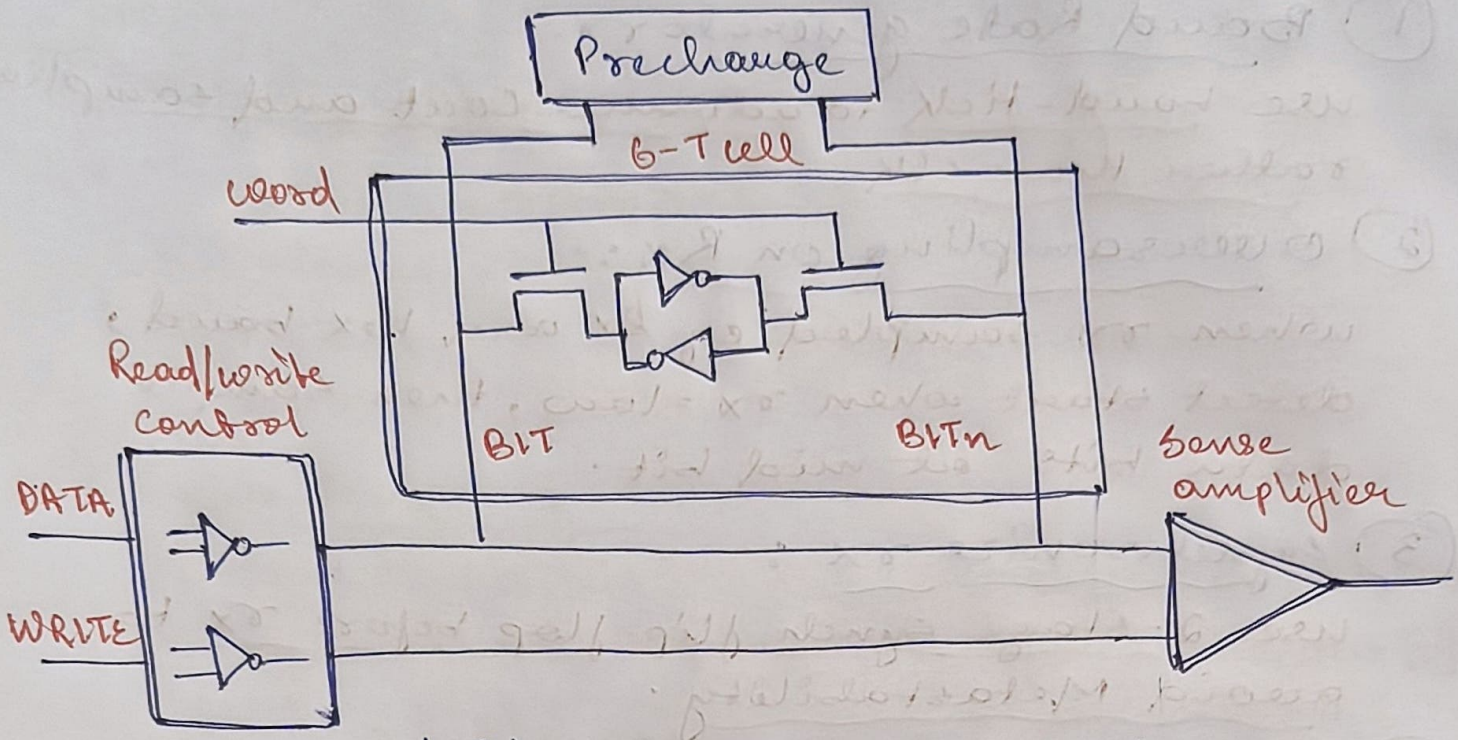
1-Bit SRAM (Static Random Access Memory)

- It can store 1-bit data and perform both read and write opn.



1-Bit SRAM structural block

- It uses clk-controlled storage element to write data and an address ctrl signal to determine if the cell is active

(1) when read_write = 1 & address = 1
ckt {writes} i/p data_in into int. storage (data)

(2) when read_write = 0 & address = 1
ckt {reads} the stored data and sends it to o/p data_out

(3) when address = 0 ⇒ cell is inactive and o/p in high impedance (1'bz) disconnecting it from databus

- So, simple 1-bit SRAM cell mimics a basic memory unit capable of controlled read/write opⁿ using clk and address signals.

- Step-by-step Explaination

① I/p and o/p :-

⇒ data_in - bit to be written into memory

⇒ read_write - control (1→write, 0→Read)

⇒ address - Enable the memory cell

⇒ clk - clk signal

⇒ data_out - output for read data

② Internal Reg :-

reg_data acts as storage element to hold 1-bit

③ write operatⁿ :

on every +ve clk edge, if read_write = 1 and address = 1

* data_in stored into data

④ Read operatⁿ :

if read_write = 0, address = 1

* The stored value data is sent to data_out

⑤ Otherwise, when address = 0

⇒ output is set to high impedance (1'bz)

⇒ Cell is not driving Bus.