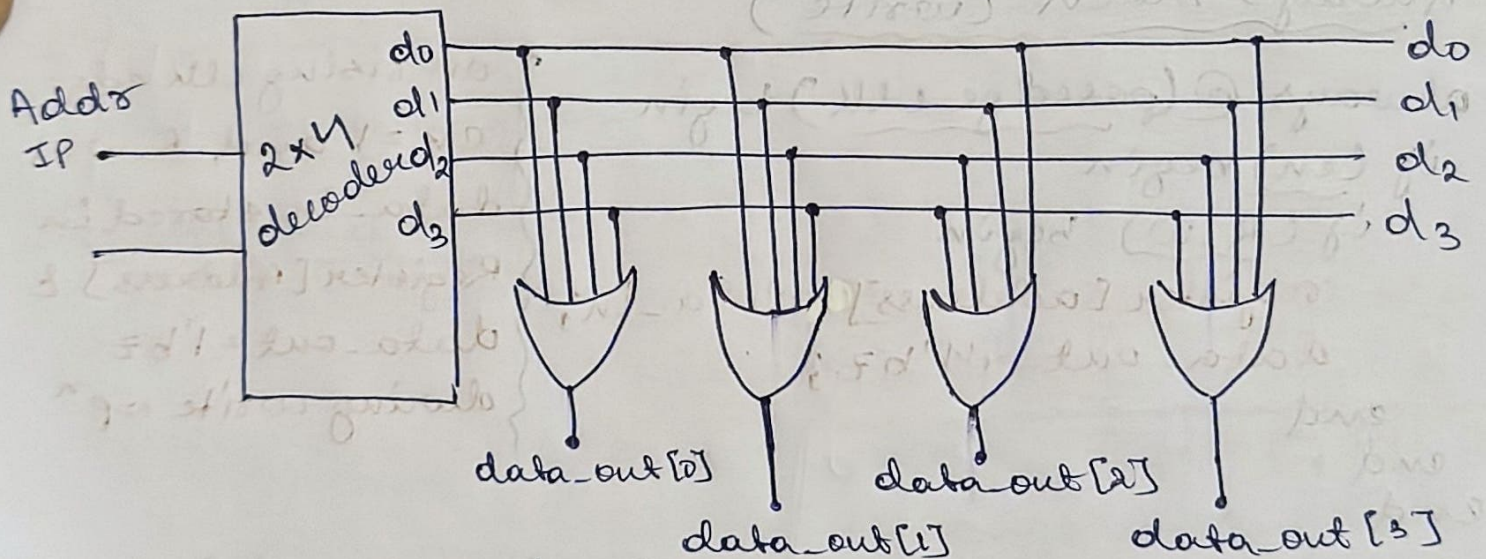
4x4 ROM (4 words x 4 bits)

- A small ROM with 4 address (2-bit addr) and 4-bit data words.
- Suppose contents are preinitialised (0, 5, 10, 15)
- when en=1, ROM o/ps [data_out = mem[address]] synchronised on the rising clk
- when en=0, ROM o/p to [high impedance (1'bz)]
- Since this is Read-only lookup table - no write
- Formula almost similar to RAM

> Memory capacity = 2^n words x m bits/word



- Storage :- [3:0] register [0:3] - 4 entries, each 4 bits
- Initialization :- loads register[0]=0, register[1]=5, register[2]=10, register[3]=15 and set data_out=0

- Read logic :- on each rising clk
  - ⇒ if en=1, reg[addr] is shown on data_out. (synchronous read)
  - ⇒ if en=0, data_out = 1'bz

Logic block

```
always @(posedge clk) begin
  if (en)
    data_out = register[address];
  else
    data_out = 4'dz;
end
```