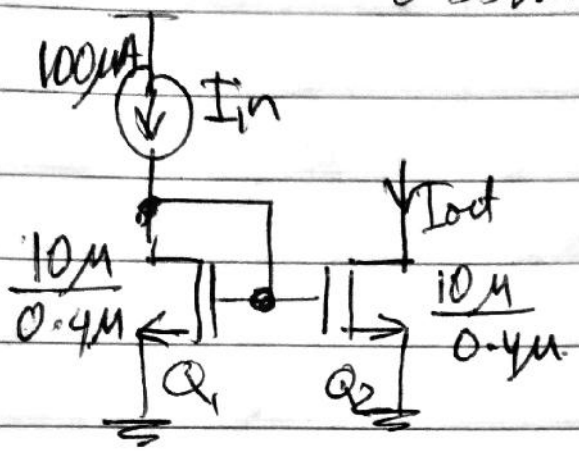
Problem 8.3

0.35μm nMOS $\mu_n C_{ox} = 190 \frac{\mu A}{V^2}$

$\lambda \cdot L = 0.16$

$C_{ox} = 4.5 \frac{fF}{\mu m^2}$

$V_{eff2} = 205mV$



Find resulting change in Iout for

(a) threshold voltage of Q_2 increase by 5mV

(b) μ_n of Q_2 increases by 5%

(c) L_2 increases to 0.42μm.

Solution:

(a) $I_{out}' = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{eff} + \Delta V_{tn})^2$

$= I_{out} \left(1 + \frac{\Delta V_{tn}}{V_{eff}}\right)^2$

$\overset{\sim}{=} I_{out} \left(1 + \frac{2\Delta V_{tn}}{V_{eff}}\right) = 1.05 \cdot I_{out}$

$= \underline{105\mu A}$

5% error.

(b) $I_{out}' = 1.05 \mu_n C_{ox} \frac{W}{L} (V_{eff_2})^2$

$= 1.05\, I_{out}$

$I_{out}' = 105\,\mu A$ ← 5% error.

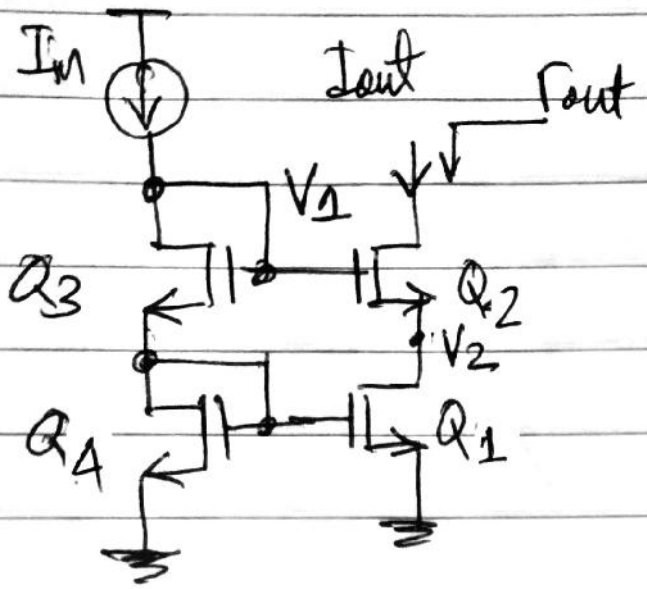
(c) $I_{out}' = \frac{\mu_n C_{ox}}{2} \frac{W}{L(1+0.05)} V_{eff}^2$

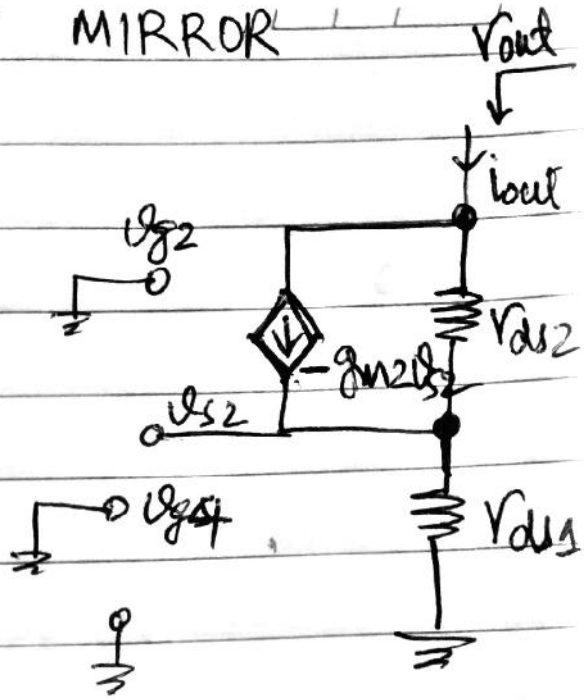
Using Taylor expansion of $\frac{1}{1+\Delta x} \simeq 1-\Delta x$

$\therefore I_{out}' \simeq (1-0.05) I_{out} = 95\,\mu A$

$\therefore$ 5% error in I_{out} for 5% error in L

CASCODE CURRENT MIRROR





Based on our result from source degen CM we can write

$$r_{out} \geq r_{ds2}(1 + g_{m2} \cdot r_{ds1})$$

Compliance:

Assuming all transistor identical.

$$V_1 = 2V_{GS}.$$

$$V_2 = V_1 - V_{GS} = V_{GS}$$

$$\therefore V_{o(min)} = V_2 + V_{eff_2} = V_{tn} + 2V_{eff}$$

↳ wasted headroom.

P 3.20

0.35 μm CMOS : $\lambda \cdot L = 0.16\ \mu m/V$

$I_{in} = 300\ \mu A$

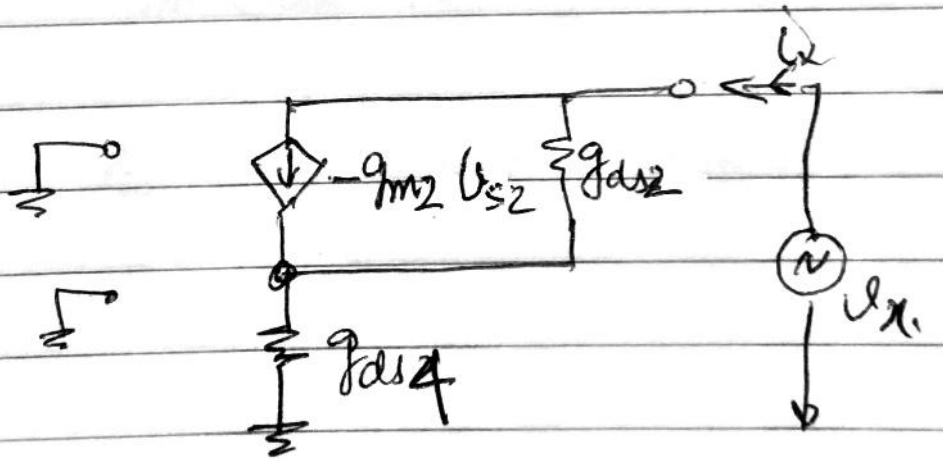
$\left(\frac{W}{L}\right)_{1,2,3,4} = \frac{50\ \mu m}{0.5\ \mu m}$, $V_{tn} = 0.57$

$$V_{eff_{1,2,3,4}} = \sqrt{\frac{2 \times 300\ \mu A}{190\ \mu A/V^2 \cdot \frac{50}{0.5}}} = 177\ mV$$

$$V_o(min) = V_{tn} + 2V_{eff} = 0.924\ V$$

costly

Output Impedance:



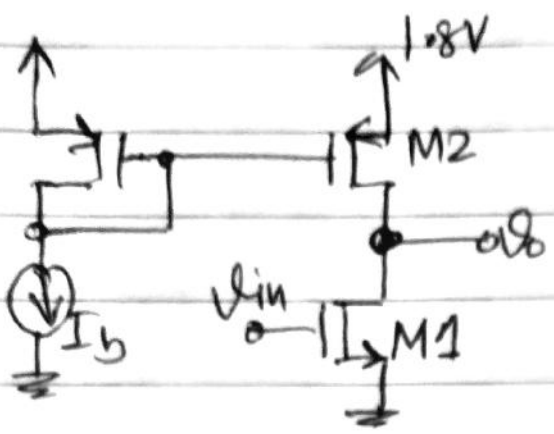
$$\therefore r_{ds2} = r_{ds4} = \frac{1}{\lambda \cdot I_D} = \frac{0.5\mu}{0.16 \times 300\mu} = 10.41\ k\Omega$$

$$g_{m2} = \frac{2I_D}{V_{eff}} = \frac{2 \times 300\ \mu A}{0.177\ V} = 3.38\ mS$$

$$r_{out} \cong 10.41k(1 + 3.38m \times 10.41k) = 376.69\ k$$

36 × improvement !

PROBLEM 8.10



Technology : 0.18μm CMOS
Power = 1mW
$V_{eff_{1,2}} = 250\,mV$
$L = 0.25\,\mu m$
Gain > 5
$\mu_n C_{ox} = 270\,\frac{\mu A}{V^2}$, $\mu_p C_{ox} = 70\,\frac{\mu A}{V^2}$

For 1mW power : $1.8V \times I_{D1} = 1mW$

$\Rightarrow I_{D1} = I_{D2} = 555\,\mu A.$

$$r_{ds1} = r_{ds2} = \frac{1}{\lambda I_D} = \frac{0.25\mu}{0.01\frac{\mu m}{V} \cdot 555\mu A} = 5.6k\Omega$$

$$\therefore \text{gain} = g_{m1}(r_{ds1} \| r_{ds2}) = \frac{2I_D}{V_{eff}} \cdot \left(\frac{5.6k}{2}\right)$$

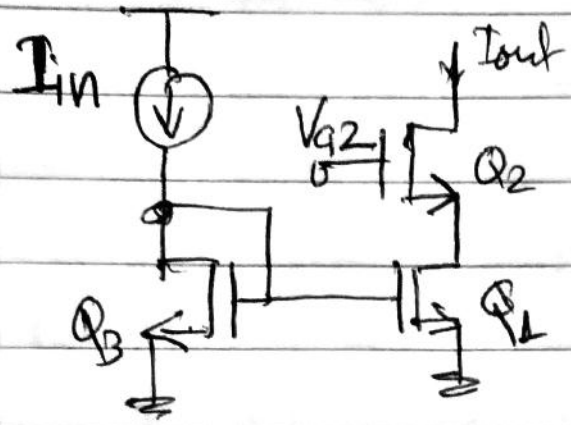
$$= \frac{2 \times 555\mu}{0.25V} \cdot 2.8k = 24.8 > 5$$

$$\frac{W_1}{L_1} = \frac{I_{D1} \times 2}{\mu_n C_{ox}(0.25)^2} \simeq 65$$

Also

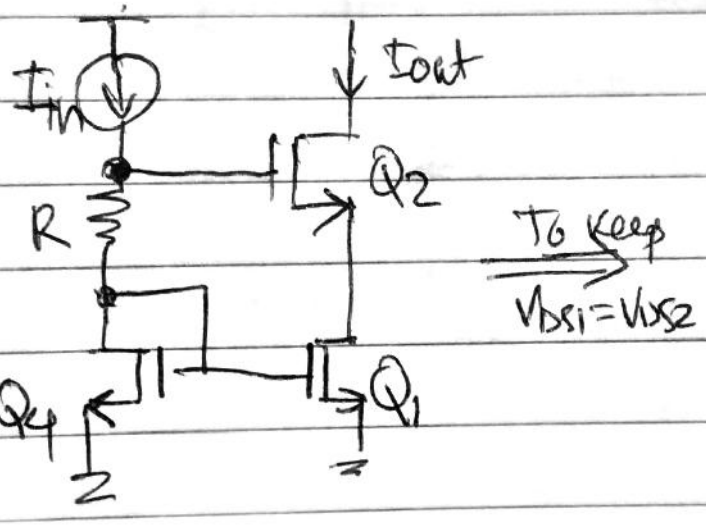
$$\frac{W_2}{L_2} = \frac{I_{D1} \times 2}{\mu_p C_{ox}(0.25)^2} = 253$$

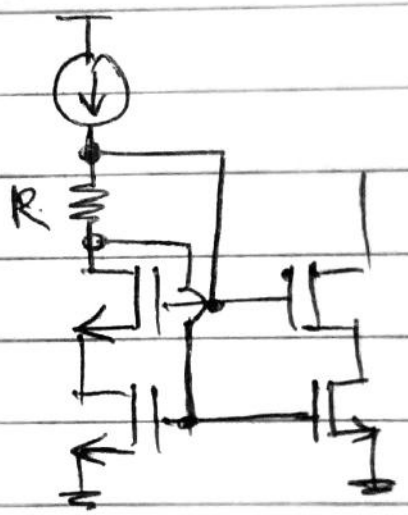
WIDE SWING CURRENT MIRROR



$$V_{g2}(min) = V_{DS1}(min) + V_{GS2}$$

$$= V_{eff1} + V_{GS2}$$



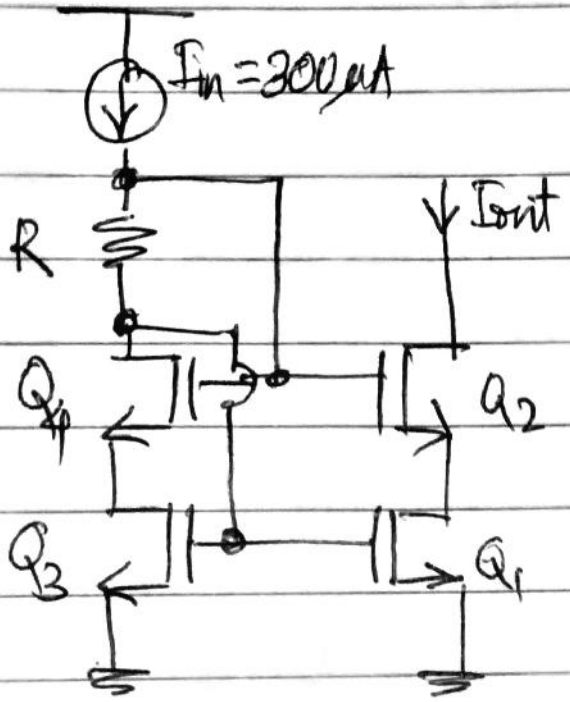


Choose R such that $I_{in}R = V_{dsat_1}$

An example:

0.35μm CMOS

$$\left(\frac{W}{L}\right)_{1,2,3,4} = \frac{50\,\mu m}{0.5\,\mu m}$$



$V_{tn} = 0.57V$, $V_{eff} = 177mV$

$\therefore$ Choose $R = \frac{177mV}{300\mu A}$

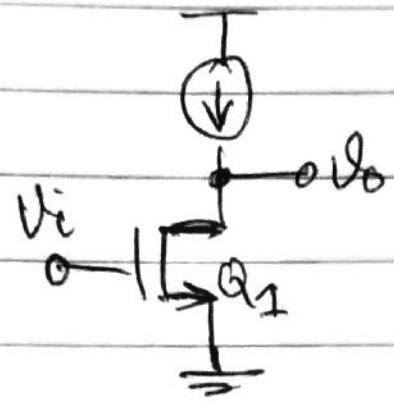
$= 590\,\Omega$

$V_{DS1} = V_{GS3} + I_{in}R - V_{GS2}$

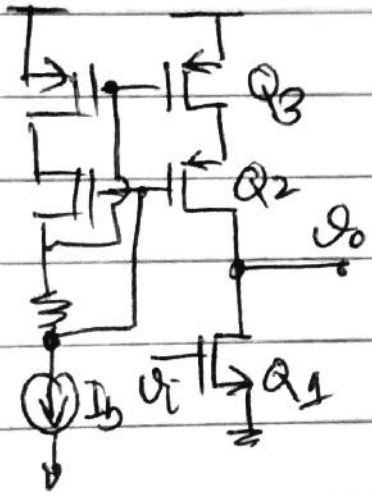
$= 177mV \leq V_{eff1}$

$V_o(min) = V_{DS1} + V_{eff2} = 2 \cdot V_{eff} = 0.354\,V$

COMMON-SOURCE AMP WITH CASCODE LOAD



$$A_v \cong g_{m1} \cdot r_{ds1}$$



$$A_v \cong g_{m1} \cdot r_{ds1} \,||\, [r_{ds2}(1 + g_{m2} r_{ds3})]$$

small || big

small.