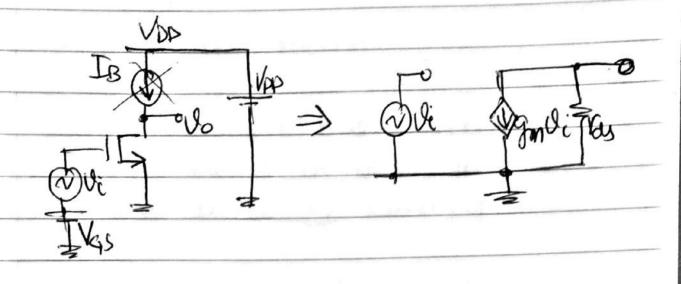
KECAP & SMALL-81GNAL MODELING



- -> Set all AC(small-signal) independent sources to zero; a - open, i - short -> Find the DC operating point gm /35/60
- -> Set all the DC (Bias) independent sources to zen
- -> Replace all non-linear elements with their small-signal equivalent.

 - Calculate the small-signal verpose.

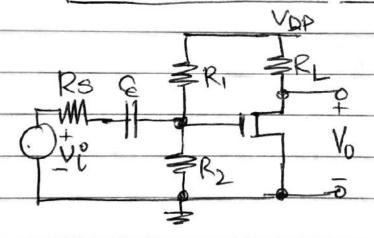
CURRENT MIRRORS

Why current nurrors ?

-> Provide bias current for multiple blocks in an IC from one single pristine source ex. Bandgap reference.

-> Active load for amplifiers.

BIAS CIRCUIT FOR DISCRETE MOS



Not suitable for IC:

- Resistors consume big area.
- also big orea
 - Bèas current variations huge.

Current Mirrors as bies aurrents VDD VOD VDD) Prisitive Source <u>J2</u> IIN > Current Mirrors. Why Active Load? P1.19 sti IDS → Key: Bias current is independent of output impedance

Resistive Load. R1=0.9N=40BK > yob=zok A = 9m× (Vall R) = 9mR_ = 28. Load line RL = 4.5K of Bias current and output impedance are NOT independent.

How to Greate Current Myrvors. Let's day we want 80 nA. Eg. MMOS bieved in saturation is a current mirror. 0.8 um NMOS B=Unlex=92MA VGS= ? I Vefy = 166ml Vin=0.8V W = 100m ID = Unlox. W Veff => Veff = PID = 0.166V 00 VGS = VT + Veff = 0.966V & Us > Veff. How bo generate 0,966V rom

80mA·R = 0.966V => R=0.966V =12KA IBIR = VGS 2 Two reasons this not preferable (1) Large area for hit resistor D Lorge variation due to Process, Tay Better way! 1004 51 0.966V 15 Tress Voltage Compliance aurvent source When Vout > Veff >V out Vett

Error in Output current due to finite, impedance. 0.8m nMOS 6 DV 30 4V Vous > 02 = 0.12mm/V Vds ~ 1 = 666 KD DL = D = 0.77 nA Error 1 = 0.77 ml = 3.8%. Small-signal Analysis of Diode Connected Transfor => \$ Vin = 19my

R

Jam vin Tras (1) 2, Yout = Yds. To find output impedance * Turn Off all independent sources (Ac, DC) to zero * Apply a fest voltage (vy) to this
port of interest & measure
current by * Impedance - ex/in

Problem 3.1 O. SMM nMOS Mulax = 92 M/2 Van = 0.84 X.L= 0.12 Mm/ 1-6A Find 1 nominal o/p current 3 Output voltage compliance. 1 Nominal of pourrent = 20 nA 2) sout = 666 KS2 previously calculated. 3 Veff = 0.166V

degenerated Current Mirror. M,=M2 Lout Vy = Iin R+Vqs 1/2 1 | M2 | Tout = Mulox W2 (1/4 - 1/52-47) VR BR R VR OU V1 = In. R+ Vasi or I out = Mn(ox W2 (Int-Iaut)R+VGSI-VT] of Mi=Mz only soln is I'm = Jour Anollur way to prove it? (DIJ Jour > I'm => 12 VGS2 < VGS1 & oo IDSZ < IR < not possible. @ If Jout < In => Vgs2 > Vgs1 0°0 IDS2 > IR < again not possible 0° Tout = I'm

