IIIT BANGALORE

VLS 502

Analog CMOS VLSI Design

Project Report

Submitted By:-

Bibin B Jacob- MT2024513

Utkarsh Jain- MT2024538

Vaibhav Naresh Dachewar- MT2024539

Submitted To:-

Prof. Sakshi Arora

Assistant Professor,
VLSI Lab,
International Institute of Information Technology - Bangalore

Externally compensated LDO

1. Specifications

In this project we have designed an LDO subject to different conditions. For this design we are designing the LDO for both externally and internally compensated LDO. For the below figure we are considering 45nm technology node.Our aim is to design the LDO for a max and a min load condition.

Table 1: Specifications Summary

Parameter	Value
Vin	1.4V
Vout	1V
PSRR	60dB
Iload (min)	2mA
Iload (max)	10mA
Cload	1uF
Iquiescent	50uA
Transient duration	1u

2. Purpose of an LDO

Low Drop-Out (LDO) regulators are critical components in Very Large Scale Integration (VLSI) circuits, where the demand for stable power supply is paramount due to the increasing complexity and sensitivity of integrated circuits. In VLSI applications, LDOs help maintain consistent voltage levels, which is essential for the reliable operation of digital, analog, and mixed-signal components within a chip.

Key Purposes of an LDO

- **Voltage Regulation:** Maintains a stable output voltage despite variations in input voltage or load current, ensuring consistent operation of sensitive electronic components.
- **Low Noise Power Supply:** Provides clean, low-ripple power, which is essential for noise-sensitive applications such as RF circuits, audio devices, and ADCs/DACs.
- **Load Current Stability:** Supports a range of load currents while maintaining stability, which is vital in circuits with dynamic power requirements.
- **Protection for Downstream Components:** Safeguards sensitive downstream components from voltage fluctuations and overvoltage conditions.
- **Power Efficiency at Low Dropout:** Operates efficiently when the difference between input and output voltage is minimal, reducing energy loss compared to traditional linear regulators.

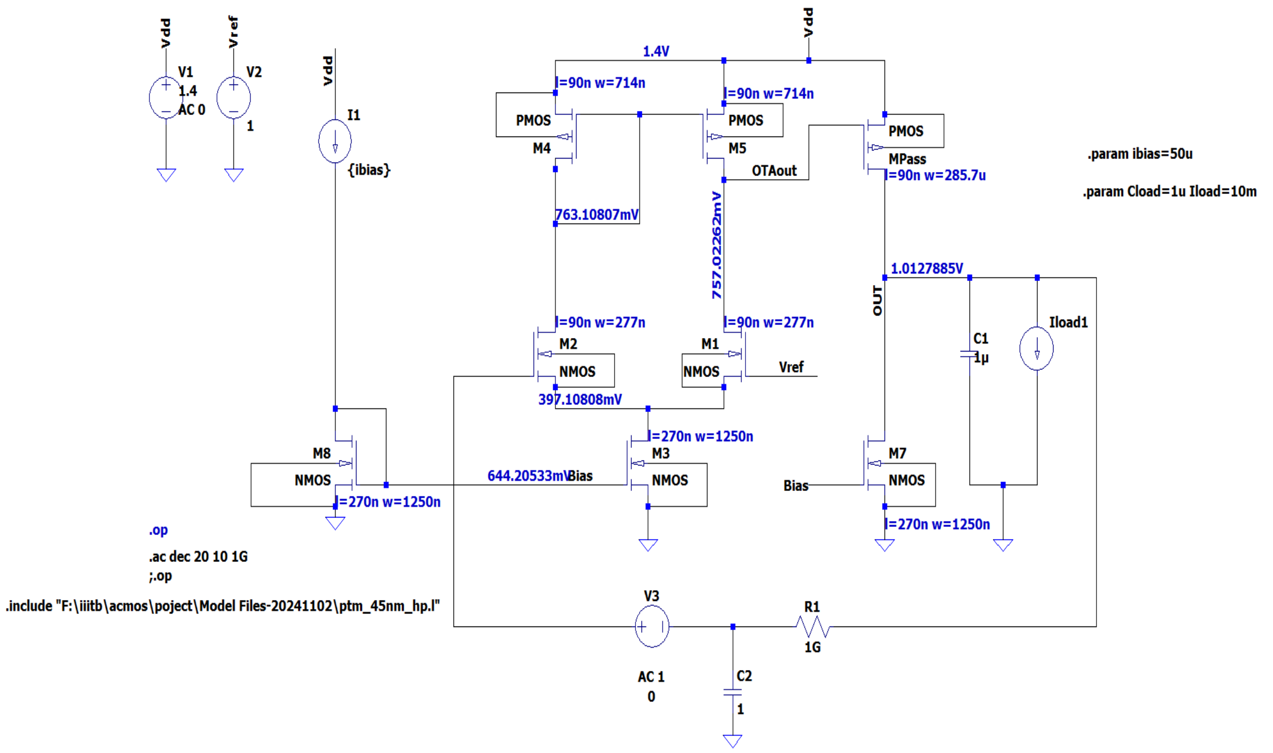


Figure 1: LDO schematic

3. Relevance of Techplots

We include all techplots generated.

- **Github Link**: https://github.com/BibinBJacob/AnalogProject
  Technology node : 45 nm
- f_T improves with shorter channel lengths, making circuits faster with scaling.
- Compared to 180 nm the FOMs
- We chose the Vds to be 0.4 mV, and we expect that to result in some error because the Vds across every MOSFET might not be the same after sizing the circuit under a particular load. It is very possible that the Vds across the MOSFETs can change under different values of load current. The above phenomenon can be understood from the output log files mentioned below.

NMOS Techplots

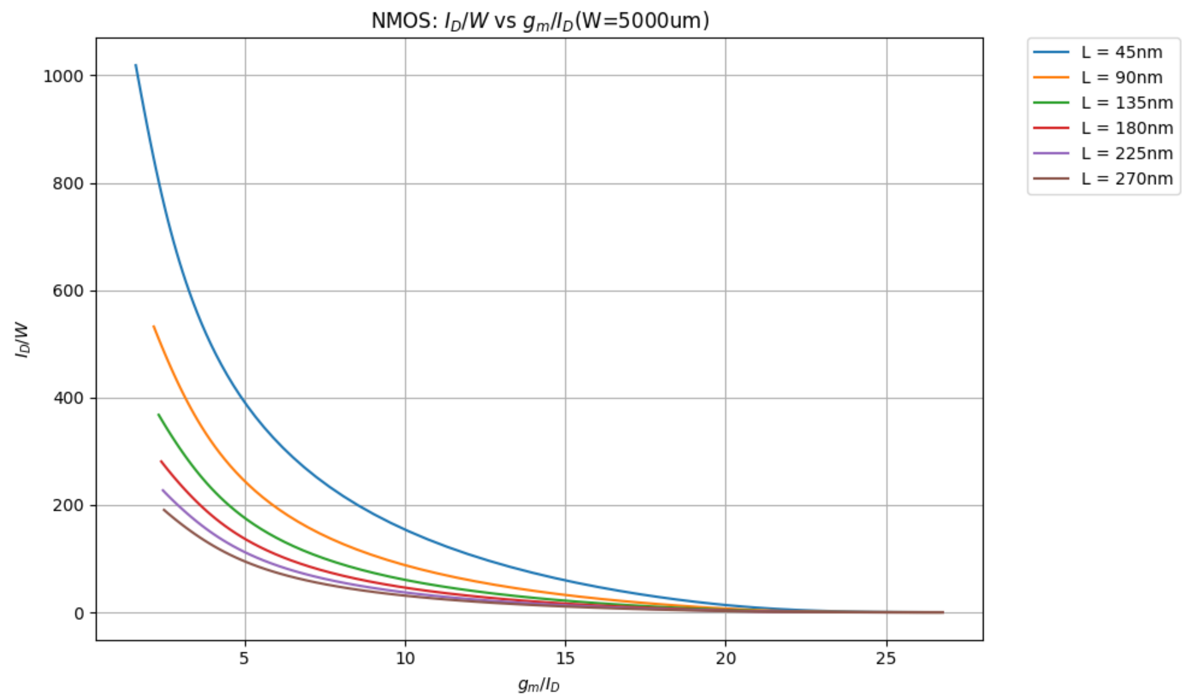


Figure 2: Id/W vs gm/Id

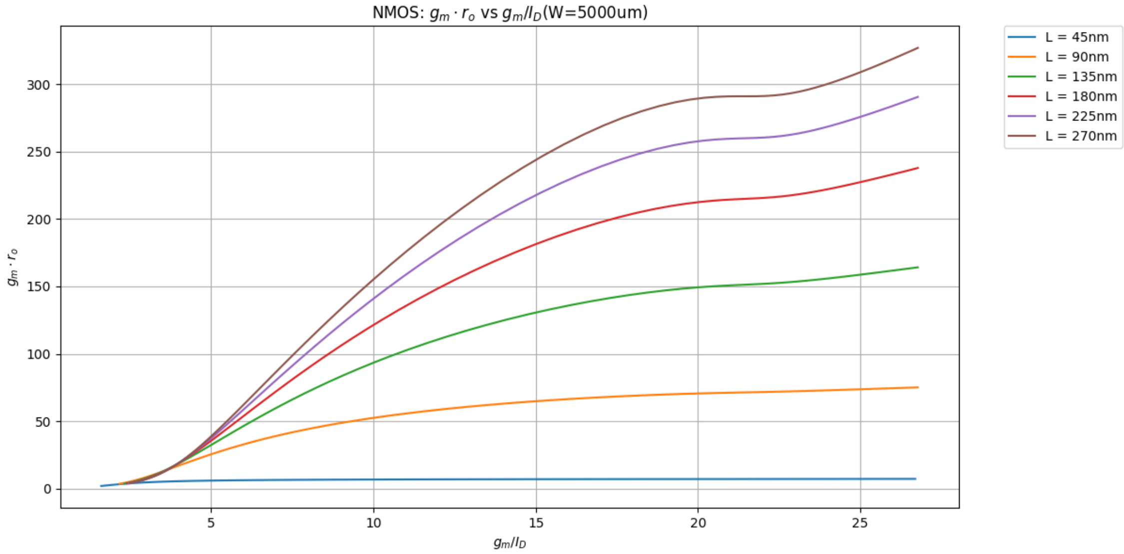


Figure 3: gmro vs gm/Id

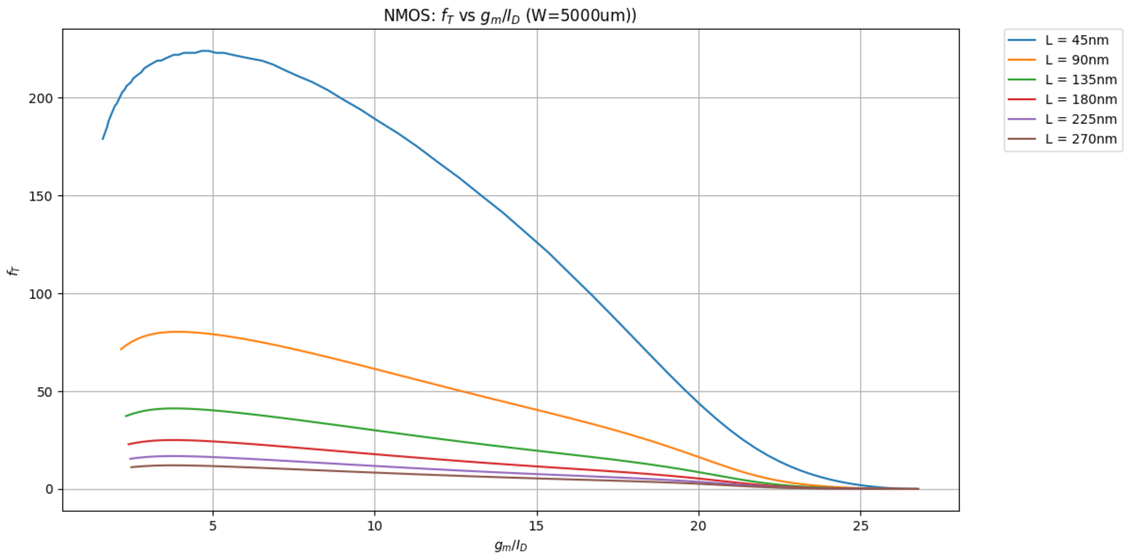


Figure 4: fT vs gm/Id

PMOS Techplots

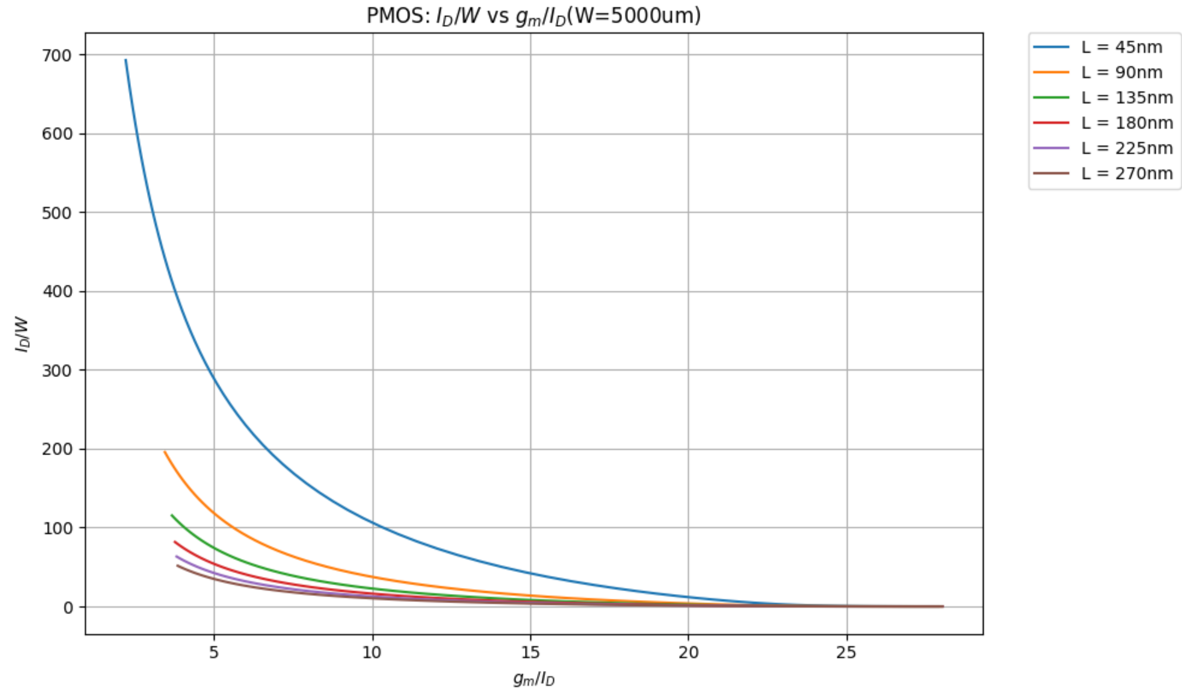


Figure 5: Id/W vs gm/Id

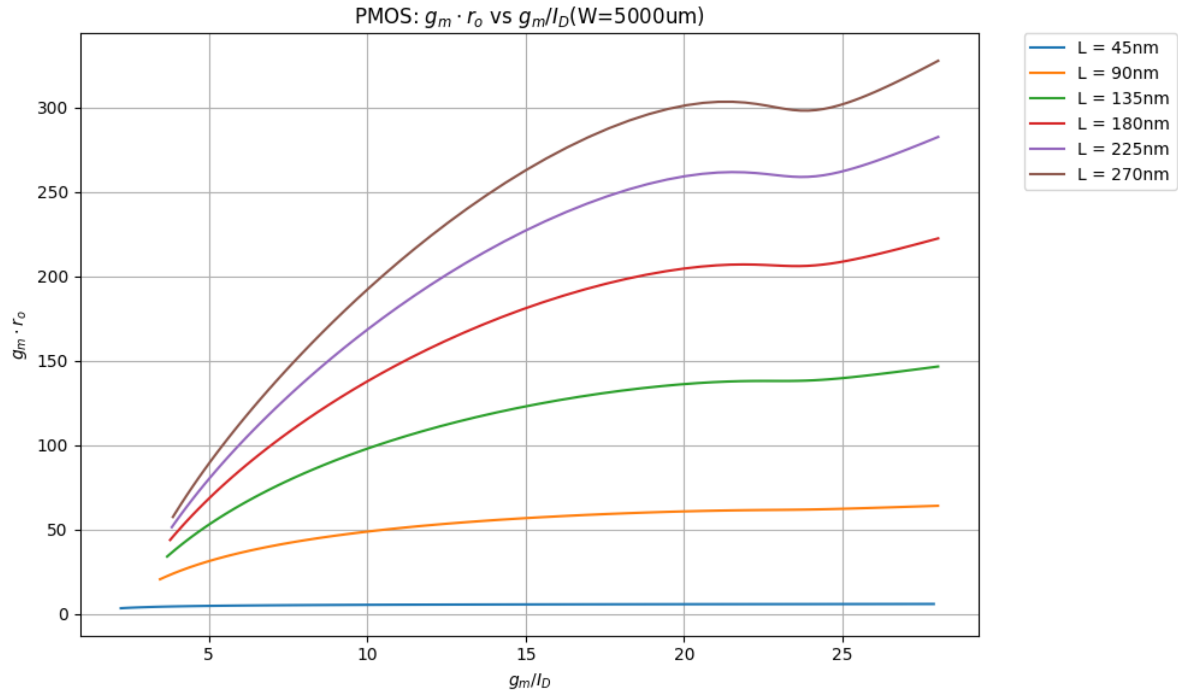


Figure 6: gmro vs gm/Id

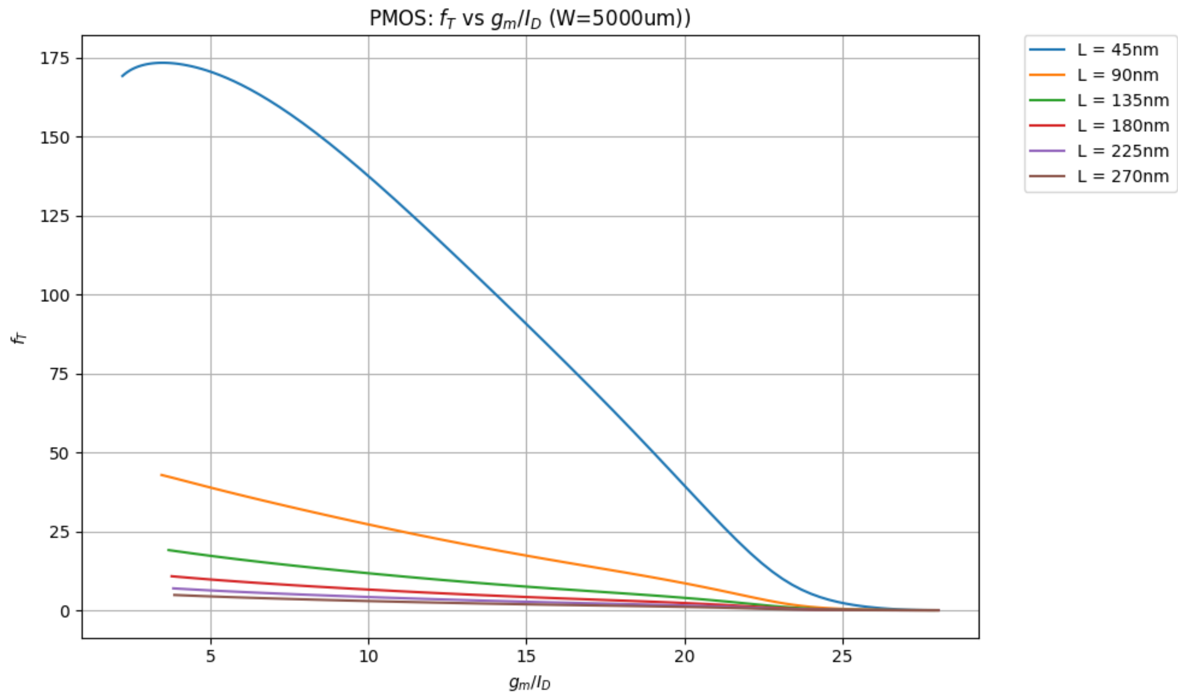


Figure 7: fT vs gm/Id

Table 2: Key Differences Between 180nm and 45nm Technology Nodes for NMOS

Parameter	**180nm Technology Node**	**45nm Technology Node**
gmro	20	7
Id/W (μA/μm)	28	154
fT (Hz)	1.6×10^{10}	19×10^{10}

Table 3: Observations on Technology Scaling Effects

Parameter	**Observation**
gmro	As the channel length decreases, the output resistance (r_o) decreases significantly, which dominates the intrinsic gain ($gmro$). As a result, the overall value of $gmro$ decreases.
Id/W	With reduced channel length, the drain current (I_d) increases due to higher mobility and lower channel resistance. Consequently, I_d/W increases, which is evident from the data.
fT	A decrease in channel length increases the transconductance (g_m), which directly leads to an increase in the unity-gain cutoff frequency (f_T). This trend is observed in the values.

4. FET Sizes

We Provide the sizes of the passFET, differential amplifier, and mirror transistors. here we also Include small-signal parameters and figures of merit (FOMs). Discuss loop gain under heavy and light load conditions.

Table 4: FET Sizes and Parameters

Transistor	Size (W/L)	g_m/I_d	$g_m * r_o$	I_d/W	f_t
PassFET pmos	285.7u/90n	10	50	35	28 GHz
Diff-Amp pmos	714n/90n	10	40	35	28 GHz
Diff-Amp nmos	277.7n/90n	10	40	90	60 GHz
Current Mirror nmos	1250n/270n	10	154.1	40	10 GHz

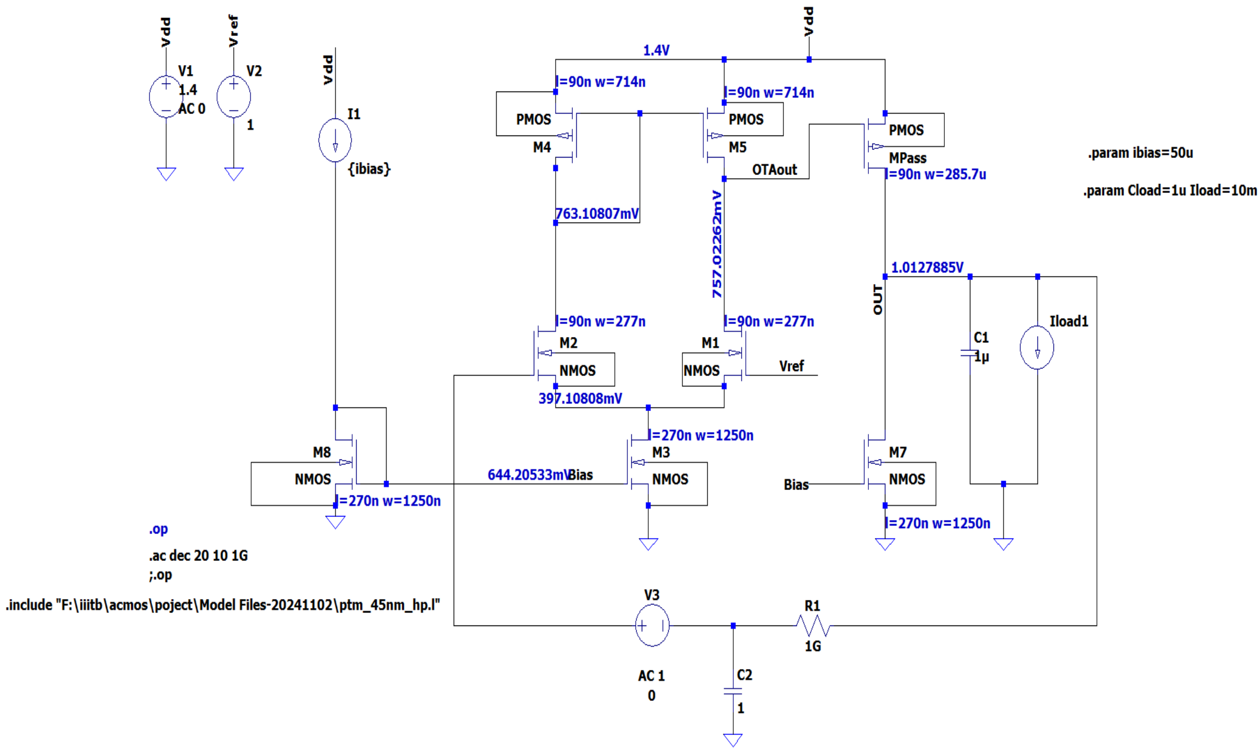


Figure 8: FET sizes and characteristics.

5. Stability Analysis

For Heavy load we get the following curve:

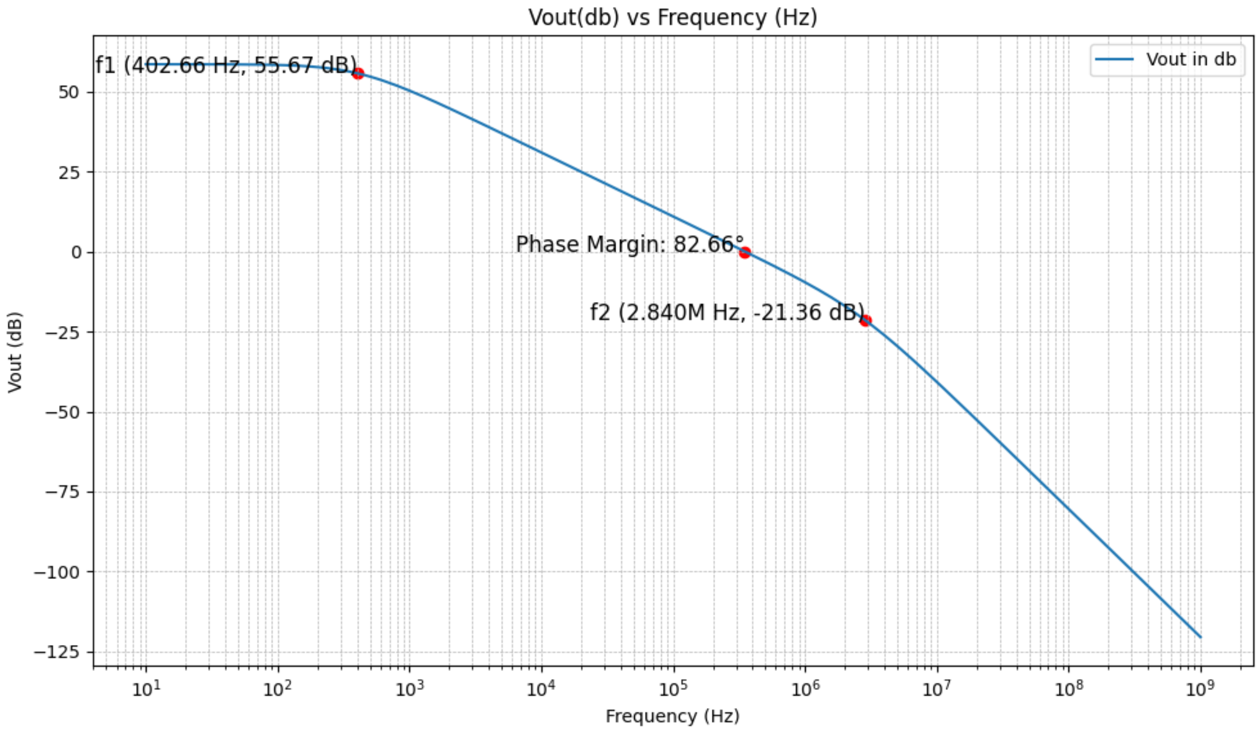


Figure 9: Pole location

For Light load we get the following curve

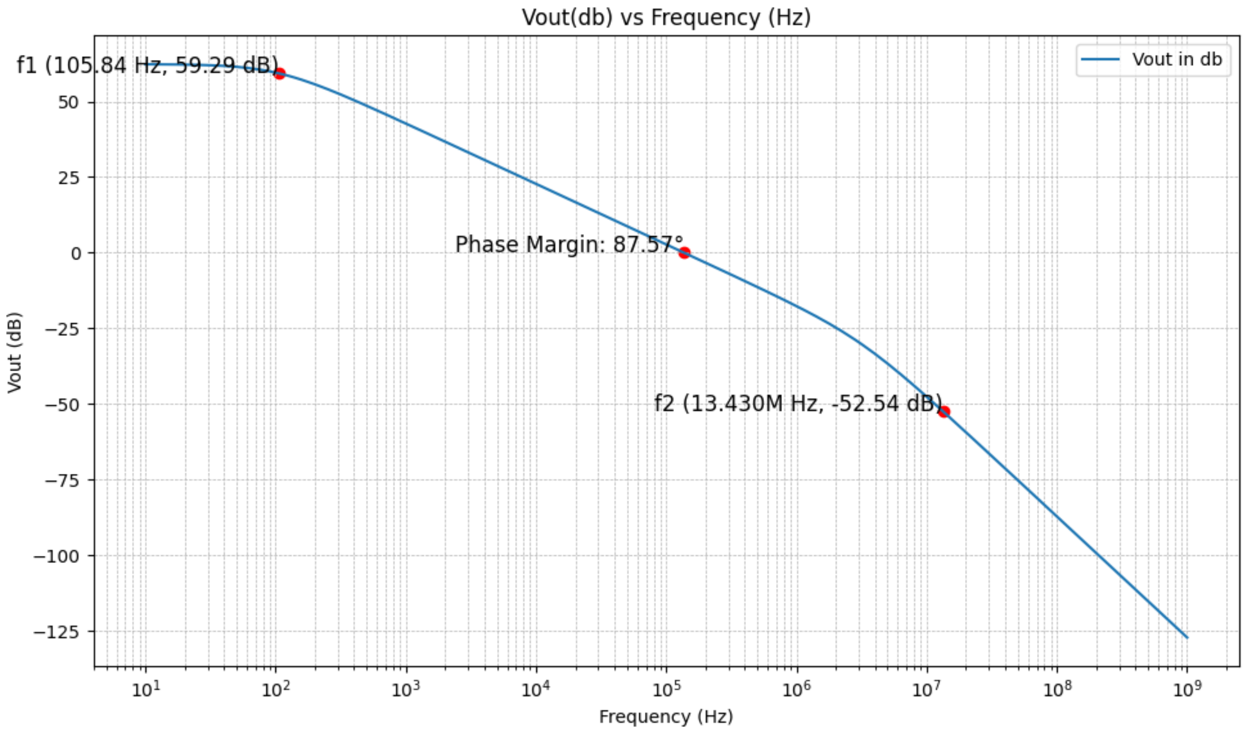


Figure 10: Pole location

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the heavy load case than the light load case. From the phase margin also we observe a smaller phase margin of 82.62 degrees for the heavy load case and 87.55 for light load case. From this analysis we can say that when we apply light load we get a more stable system.

Table 5: Key Metrics under Heavy and Light Load Conditions

Parameter	**Heavy Load**	**Light Load**
DC Loop Gain (dB)	58.52	62.30
Unity Gain Bandwidth (kHz)	402	105.8
Phase Margin (degrees)	82.62	87.55
Pole 1 (Hz)	402.6	105.8
Pole 2 (MHz)	2.84	13.43

6. PSRR Explanation

LDOs are essential components in the power supply of most ICs. They provide a ripple-free, stable fixed output voltage; isolating it from the input noise. An LDO has several important performance specifications and the power supply rejection ratio (PSRR) is one of them. PSRR is a quantitative measure of the attenuation of input ripples by the LDO at it's output. These ripples can originate from various parts of the circuit, like DC/DC converters or shared power supplies of other circuit blocks. PSRR is expressed as PSRR = 20log(vout/vin), where vout and vin refer to magnitudes of input and output ripples. In Figure 12, the PSRR of LDO is divided into two distinct regions (region 1 and region 2).Region 1 covers the low and mid frequency range till the regulator bandwidth frequency (reg), where PSRR primarily depends on the loop gain (LG) of the regulator. Region 2 starts after reg, where PSRR is independent of LG and is dominated by output parasitics, PCB impedance, etc.

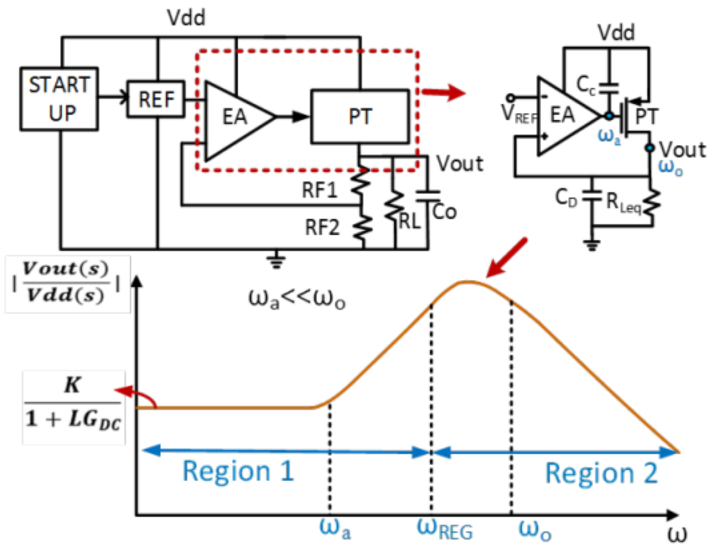
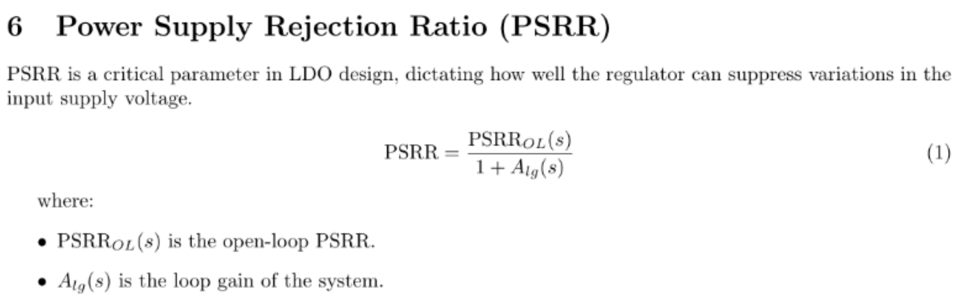


Figure 11: : Block diagram of a low drop-out (LDO) regulator and its associated PSRR curve (linear scale)



6 Power Supply Rejection Ratio (PSRR)

PSRR is a critical parameter in LDO design, dictating how well the regulator can suppress variations in the input supply voltage.

$$\text{PSRR} = \frac{\text{PSRR}_{OL}(s)}{1 + A_{lg}(s)} \quad (1)$$

where:

- $\text{PSRR}_{OL}(s)$ is the open-loop PSRR.
- $A_{lg}(s)$ is the loop gain of the system.

Figure 12: PSRR block diagram.

7. PSRR Simulation Results

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Heavy Load (10ma)

Schematic

Case 1:- Loop gain analysis:-

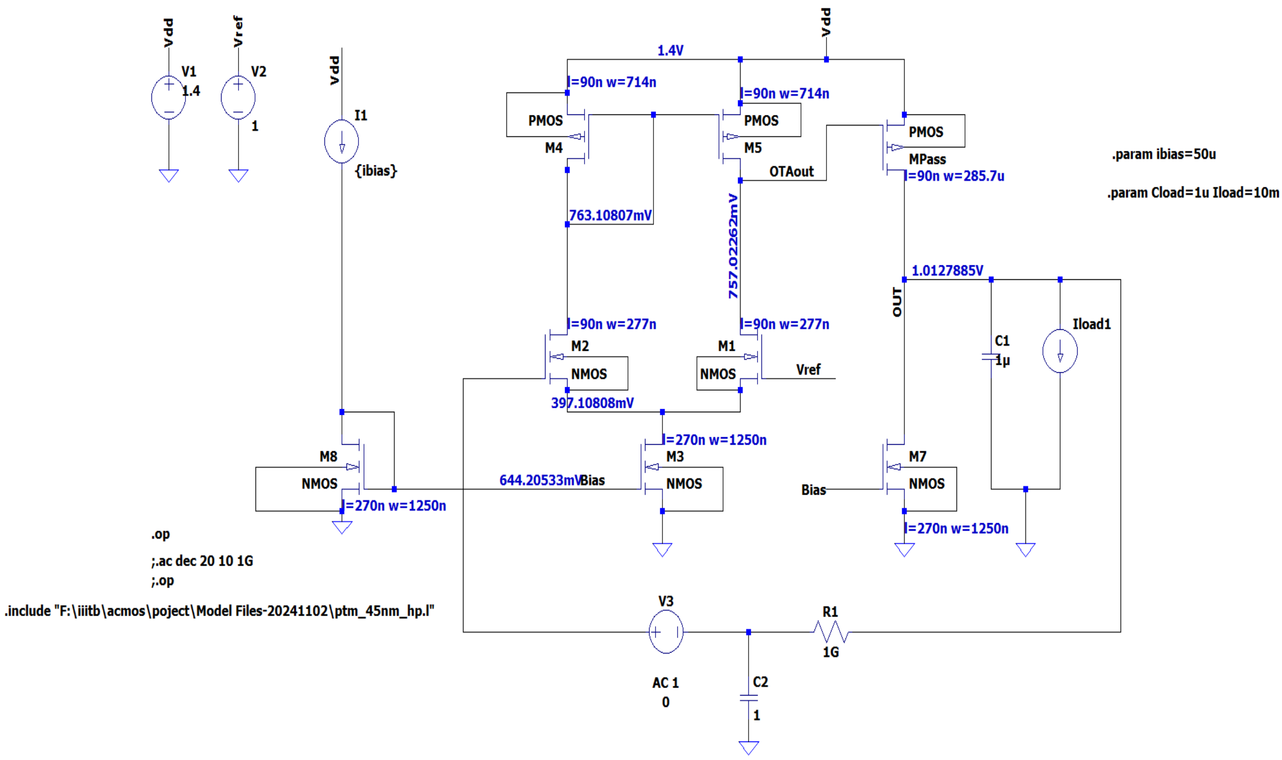
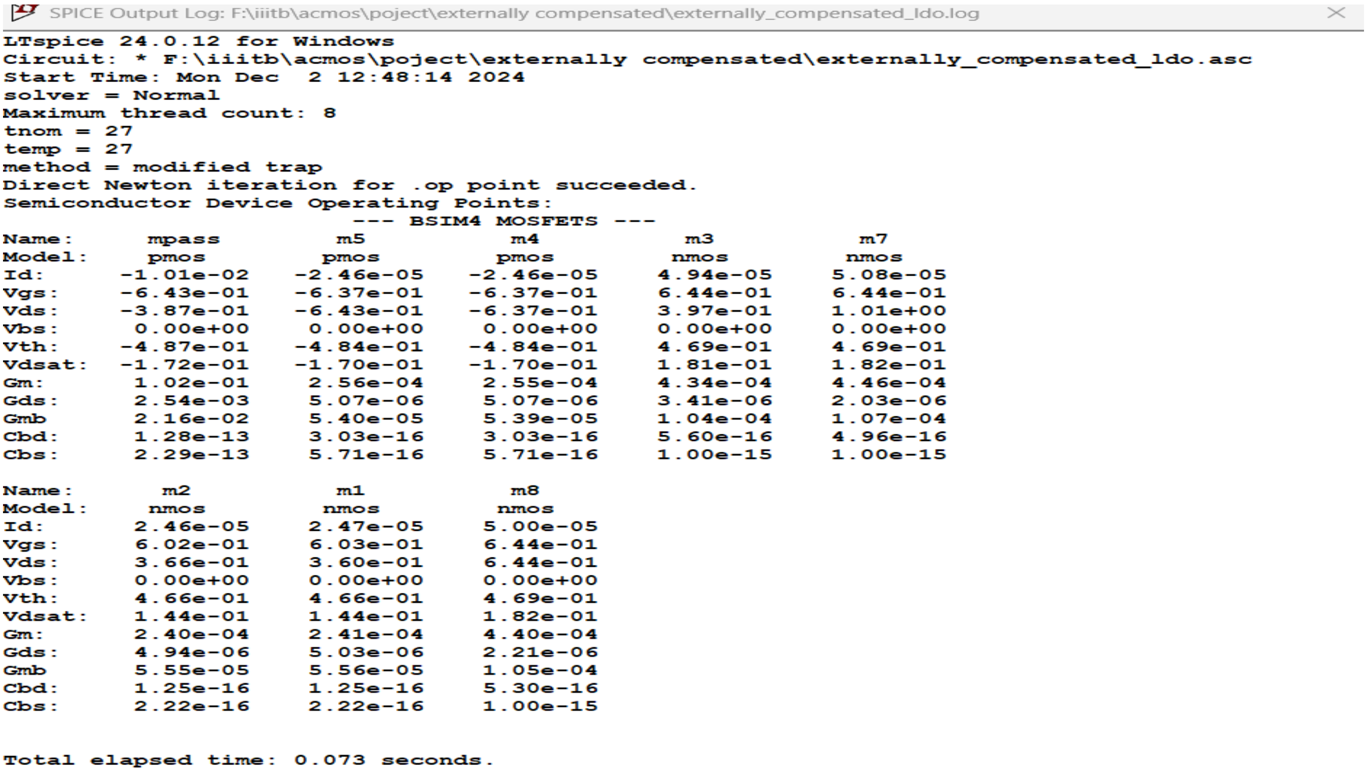


Figure 13: Schematic

Explanation of the artifact used:-

In order to calculate the loop gain we have given a RC circuit in the feedback loop alongwith a AC source with amplitude 1 (as we want to maintain an AC voltage of 1V) at the output. At the same time we also need to bias the circuit and provide a dc voltage to the gate of the nmos in the differential amplifier and for this we are giving the RC circuit which will prevent the flow of dc current to ground but will send any AC signal at the output to ground at high frequency. Also the drop across the resistor will be very less as we have given a very high resistance with very negligible current (since current going into the gate of the mosfet is zero). Thus we will bias the circuit and also calculate the loop gain.

Output Log File:-



```
SPICE Output Log: F:\iiitb\acmos\poject\externally compensated\externally_compensated_ldo.log
LTspice 24.0.12 for Windows
Circuit: * F:\iiitb\acmos\poject\externally compensated\externally_compensated_ldo.asc
Start Time: Mon Dec  2 12:48:14 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:      mpass        m5          m4          m3          m7
Model:      pmos        pmos        pmos        nmos        nmos
Id:     -1.01e-02   -2.46e-05   -2.46e-05   4.94e-05    5.08e-05
Vgs:    -6.43e-01   -6.37e-01   -6.37e-01   6.44e-01    6.44e-01
Vds:    -3.87e-01   -6.43e-01   -6.37e-01   3.97e-01    1.01e+00
Vbs:     0.00e+00    0.00e+00    0.00e+00   0.00e+00    0.00e+00
Vth:    -4.87e-01   -4.84e-01   -4.84e-01   4.69e-01    4.69e-01
Vdsat:  -1.72e-01   -1.70e-01   -1.70e-01   1.81e-01    1.82e-01
Gm:      1.02e-01    2.56e-04    2.55e-04   4.34e-04    4.46e-04
Gds:     2.54e-03    5.07e-06    5.07e-06   3.41e-06    2.03e-06
Gmb      2.16e-02    5.40e-05    5.39e-05   1.04e-04    1.07e-04
Cbd:     1.28e-13    3.03e-16    3.03e-16   5.60e-16    4.96e-16
Cbs:     2.29e-13    5.71e-16    5.71e-16   1.00e-15    1.00e-15

Name:      m2          m1          m8
Model:     nmos        nmos        nmos
Id:      2.46e-05    2.47e-05    5.00e-05
Vgs:     6.02e-01    6.03e-01    6.44e-01
Vds:     3.66e-01    3.60e-01    6.44e-01
Vbs:     0.00e+00    0.00e+00    0.00e+00
Vth:     4.66e-01    4.66e-01    4.69e-01
Vdsat:   1.44e-01    1.44e-01    1.82e-01
Gm:      2.40e-04    2.41e-04    4.40e-04
Gds:     4.94e-06    5.03e-06    2.21e-06
Gmb      5.55e-05    5.56e-05    1.05e-04
Cbd:     1.25e-16    1.25e-16    5.30e-16
Cbs:     2.22e-16    2.22e-16    1.00e-15

Total elapsed time: 0.073 seconds.
```

Figure 14: Output Log Details

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	**Type**	V_{ds} **(V)**	V_{gs}/V_{sg} **(V)**	V_t **(V)**	$V_{gs}/V_{sg} - V_t$ **(V)**	**Operating Region**
M1	NMOS	0.36	0.602	0.466	0.136	Saturation
M2	NMOS	0.366	0.602	0.466	0.163	Saturation
M3	NMOS	0.397	0.644	0.469	0.334	Saturation
M4	PMOS	0.637	0.637	0.469	0.168	Saturation
M5	PMOS	0.643	0.637	0.484	0.159	Saturation
Mpass	PMOS	0.387	0.643	0.487	0.156	Saturation
M7	NMOS	1.01	0.644	0.469	0.541	Saturation
M8	NMOS	0.644	0.644	0.489	0.155	Saturation

Table 6: Transistor Parameters and Operating Regions

Output loop gain:-

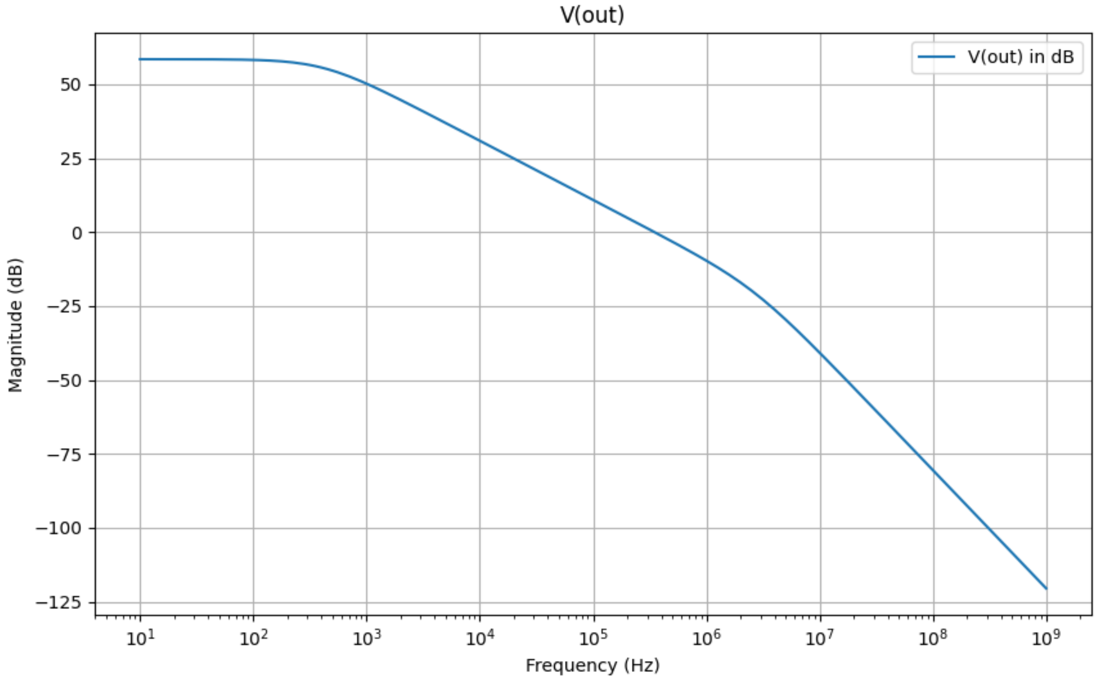


Figure 15: Output loop gain

OTA loop gain:-

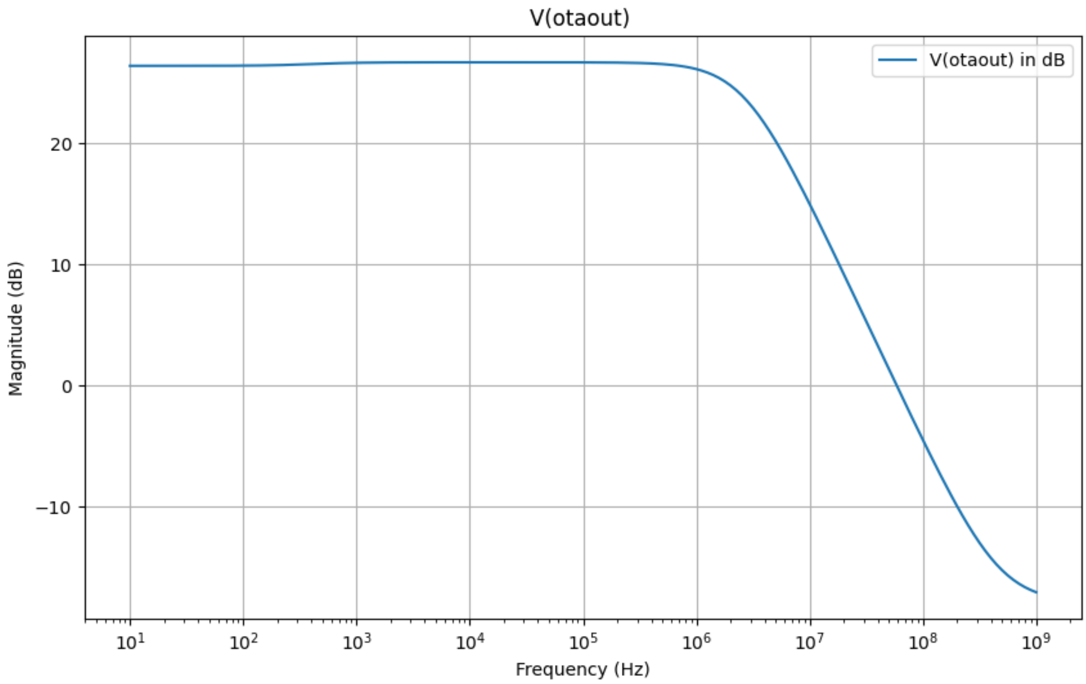


Figure 16: OTA loop gain

Phase margin

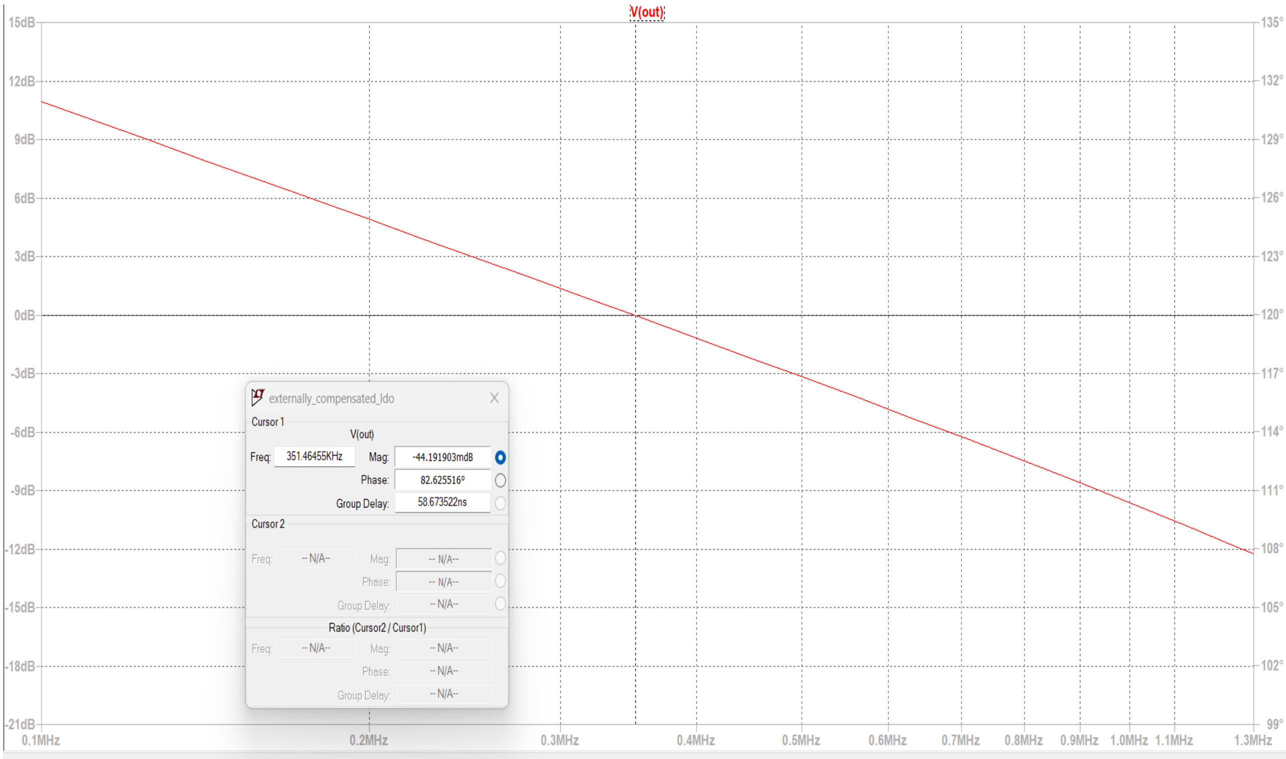


Figure 17: Phase Margin

The phase margin is 82.62

The output voltage (Loop gain) comes out to be close to 58.52db . The formula for loop gain is Adiff*Apass where Adiff is differential amplifier gain and Apass is the passfet gain.

Case 2:- Open Loop PSRR calculation

Schematic

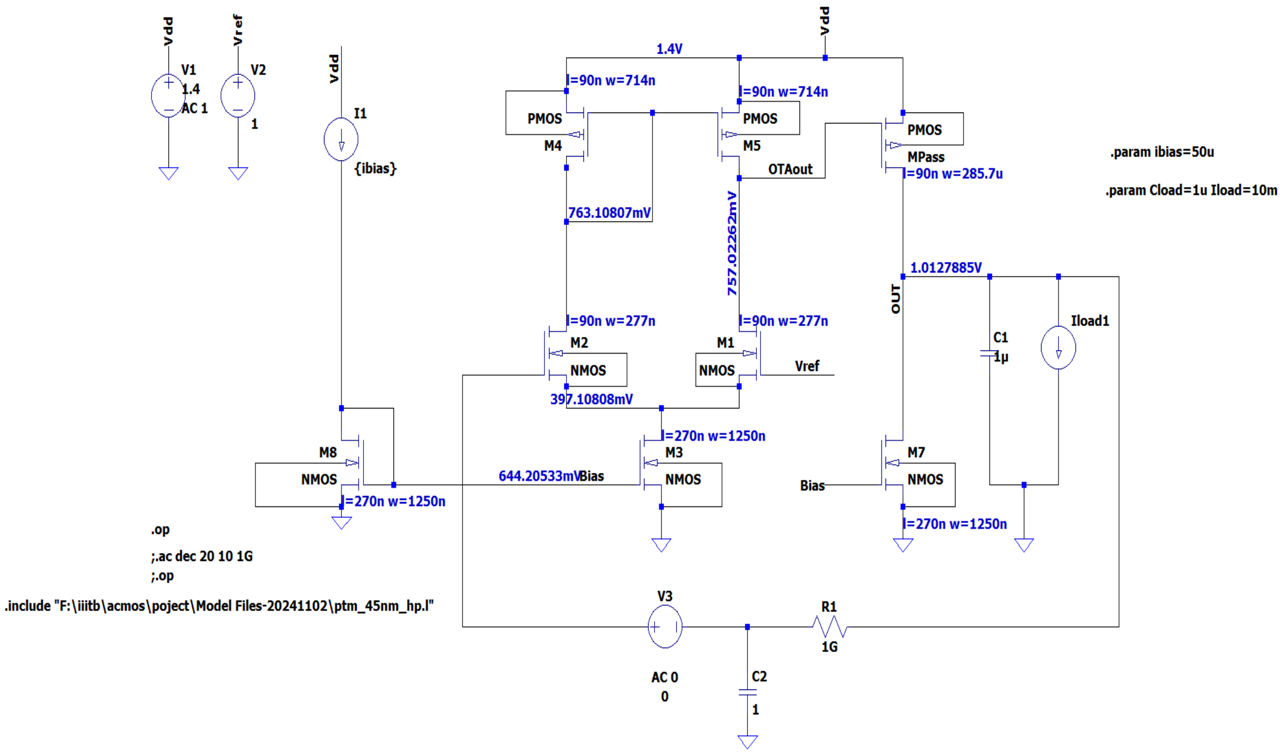


Figure 18: Schematic

Explanation of the artifact used:-

In order to calculate the open loop PSRR we need to send an AC signal from the source which in our case is VDD. Here we are giving an AC 1 signal in the source. This signal is given to the source of the passfet and the source of pmos in the diffamp. We will ideally want very bad PSRR in the diffamp as we want the OTA output to have all the AC noise such that Vsg of pmos = 0 (small signal analysis). Thus all the noise will get rejected and we will get a noise free dc voltage at the output of the LDO. Here in order to calculate the open loop PSRR we have a RC circuit to bias the differential amplifier. You can see AC 0 in the circuit indicating that there is an open loop in the circuit . From here we have calculated the open loop PSRR in the circuit. Since there is no feedback in the circuit we can thus say that there will be noise at the output and thus the rejection will be very poor.

Open loop psrr plots:-

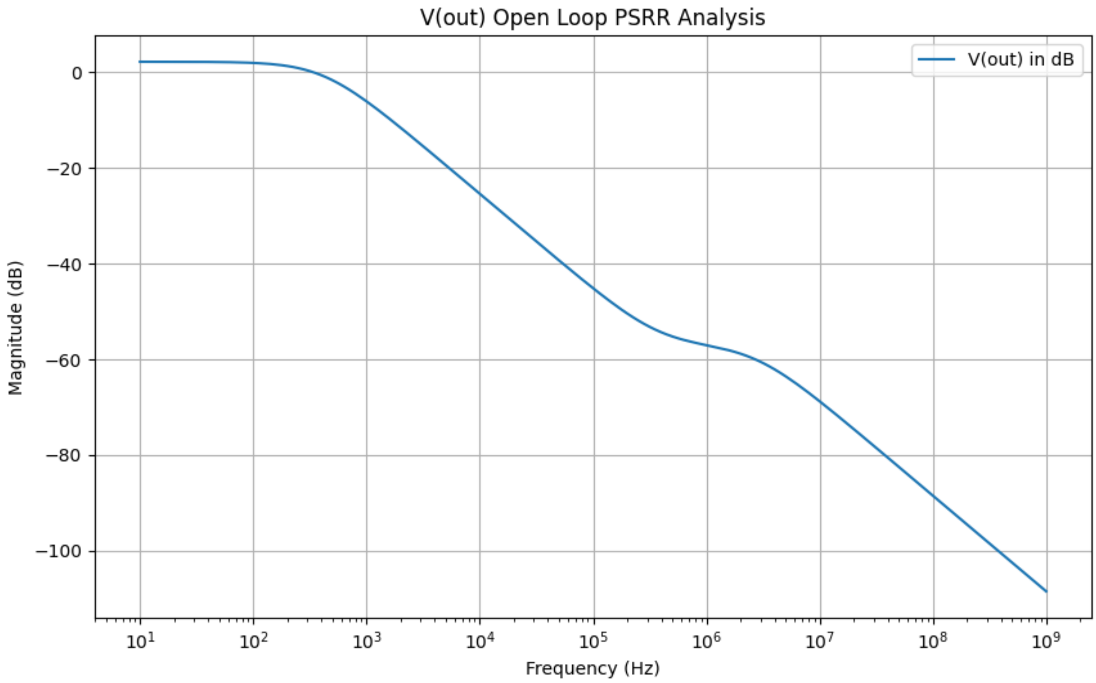


Figure 19: Open loop psrr for Output

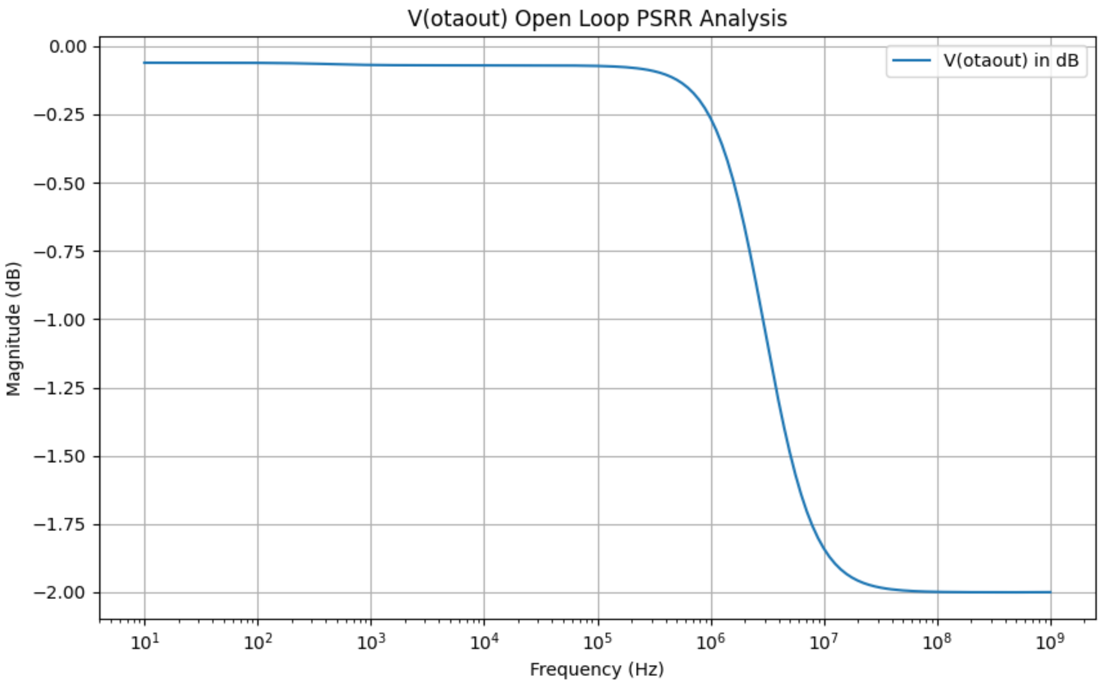


Figure 20: open loop psrr for OTA

Note:- Always observe the Vota output should be closer to 1v, the better it is for PSRR at the output as the Vsg value will be close to 0.

Case 3:- Closed Loop PSRR Calculation

Schematic

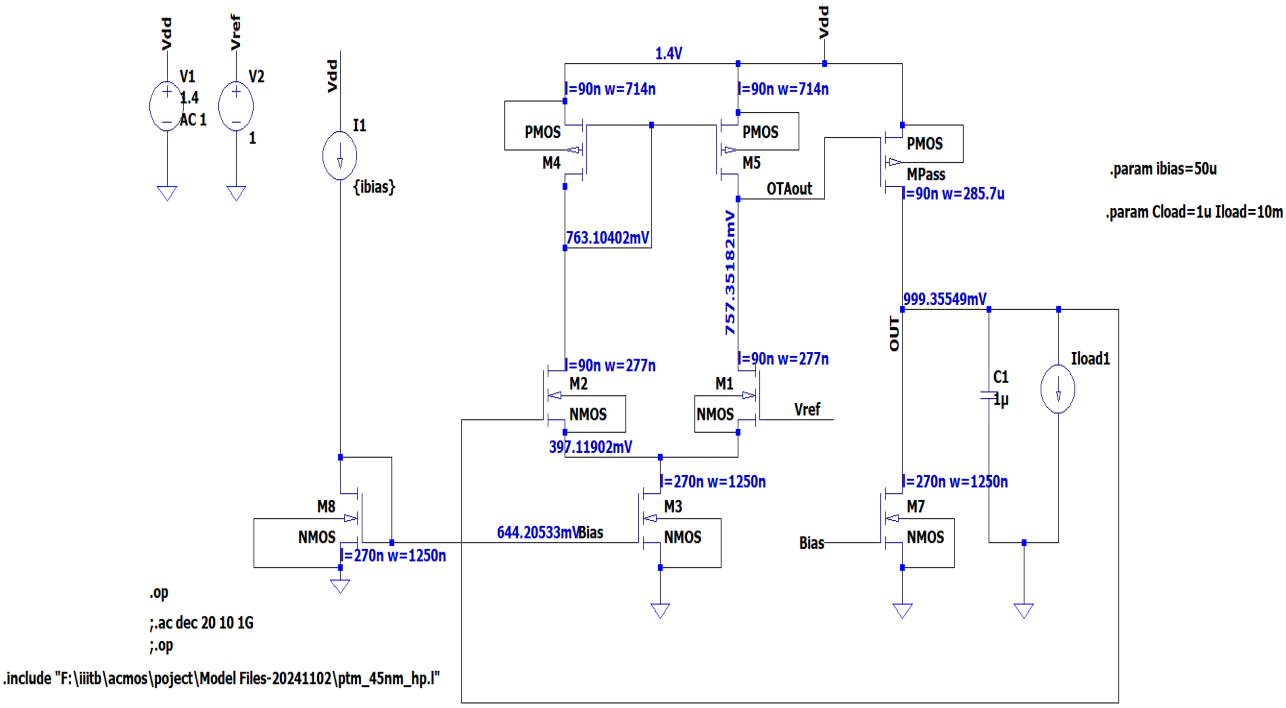


Figure 21: Schematic

Explanation of the artifact used:-

In this case we can see that we have given a AC source in the voltage source VDD. We want to see the negative feedback in the circuit due to which we will get the output voltage cancelled out (small signal analysis). Here we should observe a high PSRR according to our specifications (60db) which tells us that our sizing is perfect. For this circuit we have given a feedback from the output terminal to the input of the diffamp which indicates the feedback path.

Close loop PSRR:-

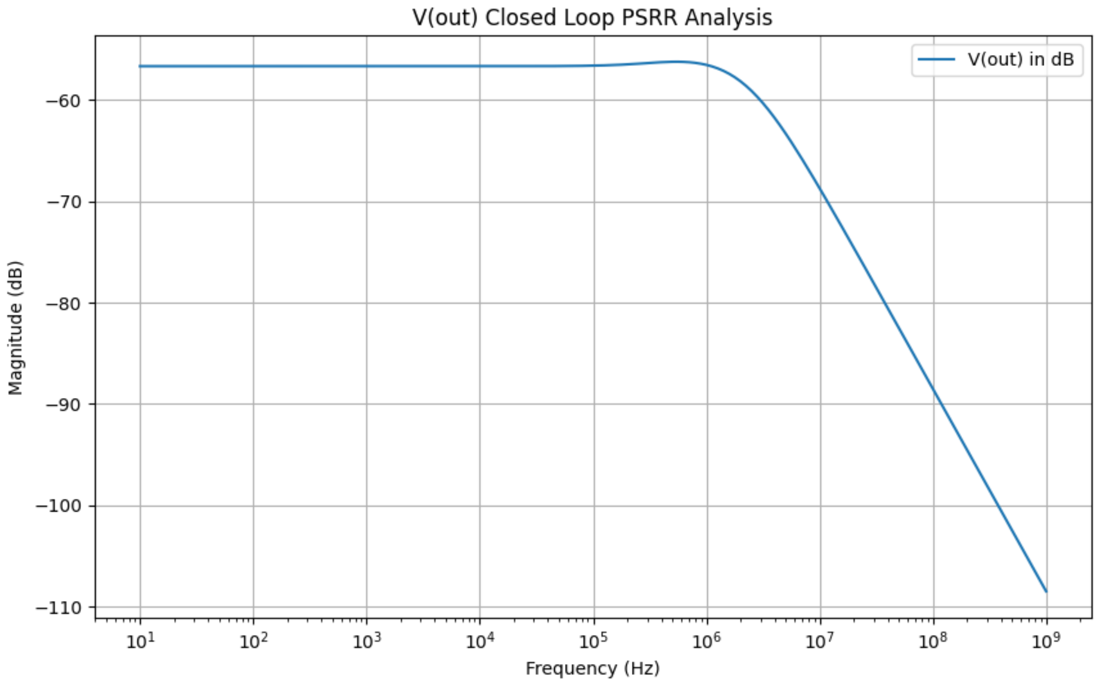


Figure 22: close loop psrr for output

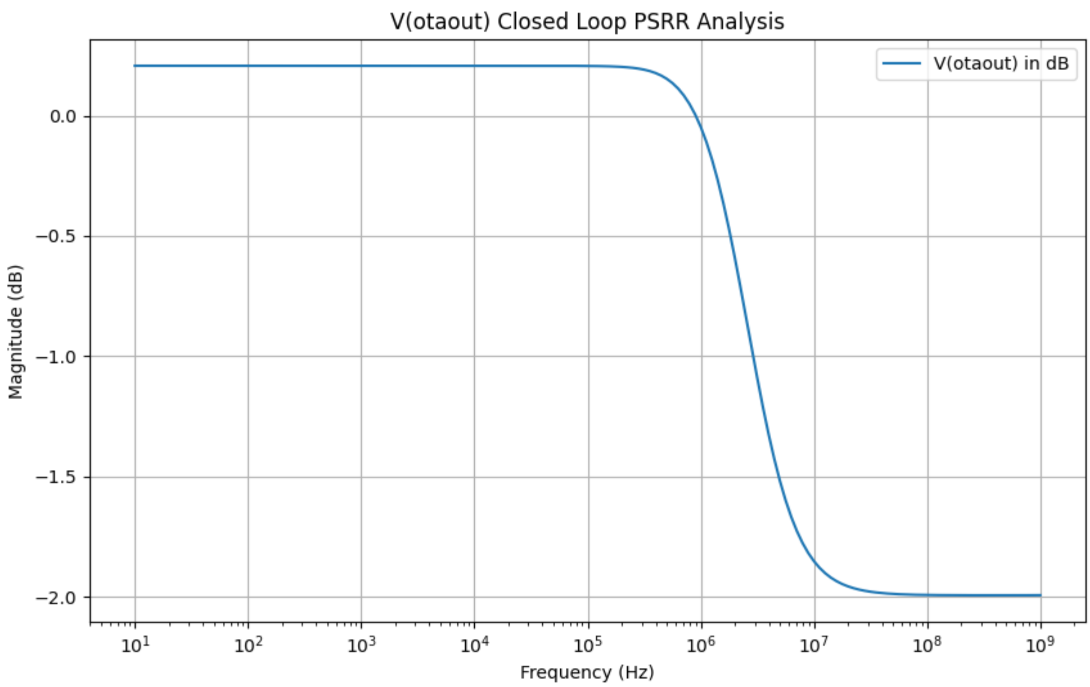


Figure 23: close loop psrr for OTA

Light Load (2ma)

Case 1:- Loop gain analysis

Schematic

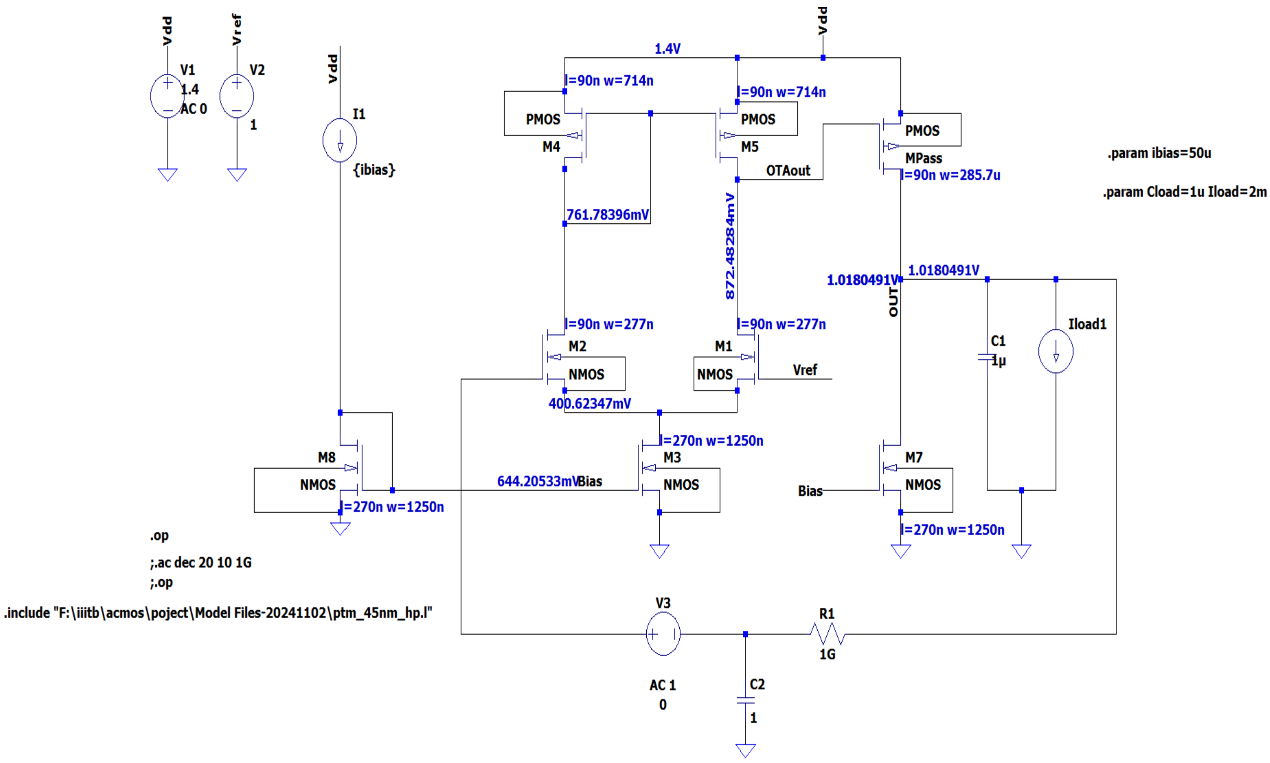


Figure 24: Schematic

Output Log File:-

```
SPICE Output Log: F:\iiitb\acmos\poject\externally compensated\externally_compensated_ldo.log
LTspice 24.0.12 for Windows
Circuit: * F:\iiitb\acmos\poject\externally compensated\externally_compensated_ldo.asc
Start Time: Mon Dec  2 16:20:41 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:      mpass       m5          m4          m3          m7
Model:     pmos        pmos        pmos        nmos        nmos
Id:       -2.05e-03   -2.44e-05   -2.50e-05    4.94e-05    5.08e-05
Vgs:      -5.28e-01   -6.38e-01   -6.38e-01    6.44e-01    6.44e-01
Vds:      -3.82e-01   -5.28e-01   -6.38e-01    4.01e-01    1.02e+00
Vbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      -4.87e-01   -4.86e-01   -4.84e-01    4.69e-01    4.69e-01
Vdsat:    -9.28e-02   -1.70e-01   -1.71e-01    1.81e-01    1.82e-01
Gm:        3.64e-02    2.53e-04    2.57e-04    4.34e-04    4.46e-04
Gds:       6.65e-04    5.30e-06    5.12e-06    3.36e-06    2.03e-06
Gmb        7.50e-03    5.34e-05    5.43e-05    1.04e-04    1.07e-04
Cbd:       1.28e-13    3.10e-16    3.03e-16    5.59e-16    4.96e-16
Cbs:       2.29e-13    5.71e-16    5.71e-16    1.00e-15    1.00e-15

Name:      m2          m1          m8
Model:     nmos        nmos        nmos
Id:        2.50e-05    2.44e-05    5.00e-05
Vgs:       6.04e-01    5.99e-01    6.44e-01
Vds:       3.61e-01    4.72e-01    6.44e-01
Vbs:       0.00e+00    0.00e+00    0.00e+00
Vth:       4.66e-01    4.65e-01    4.69e-01
Vdsat:     1.45e-01    1.43e-01    1.82e-01
Gm:        2.42e-04    2.41e-04    4.40e-04
Gds:       5.06e-06    4.27e-06    2.21e-06
Gmb        5.58e-05    5.56e-05    1.05e-04
Cbd:       1.25e-16    1.22e-16    5.30e-16
Cbs:       2.22e-16    2.22e-16    1.00e-15

Total elapsed time: 0.076 seconds.
```

Figure 25: Output Log Details

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	NMOS	0.47	0.59	0.46	0.13	Saturation
M2	NMOS	0.36	0.64	0.46	0.18	Saturation
M3	NMOS	0.40	0.64	0.46	0.18	Saturation
M4	PMOS	0.63	0.63	0.48	0.15	Saturation
M5	PMOS	0.52	0.63	0.48	0.15	Saturation
Mpass	PMOS	0.38	0.52	0.48	0.41	Saturation
M7	NMOS	1.02	0.64	0.468	0.15	Saturation
M8	NMOS	0.64	0.64	0.46	0.18	Saturation

Table 7: Transistor Data Table

Loop gain plot:-

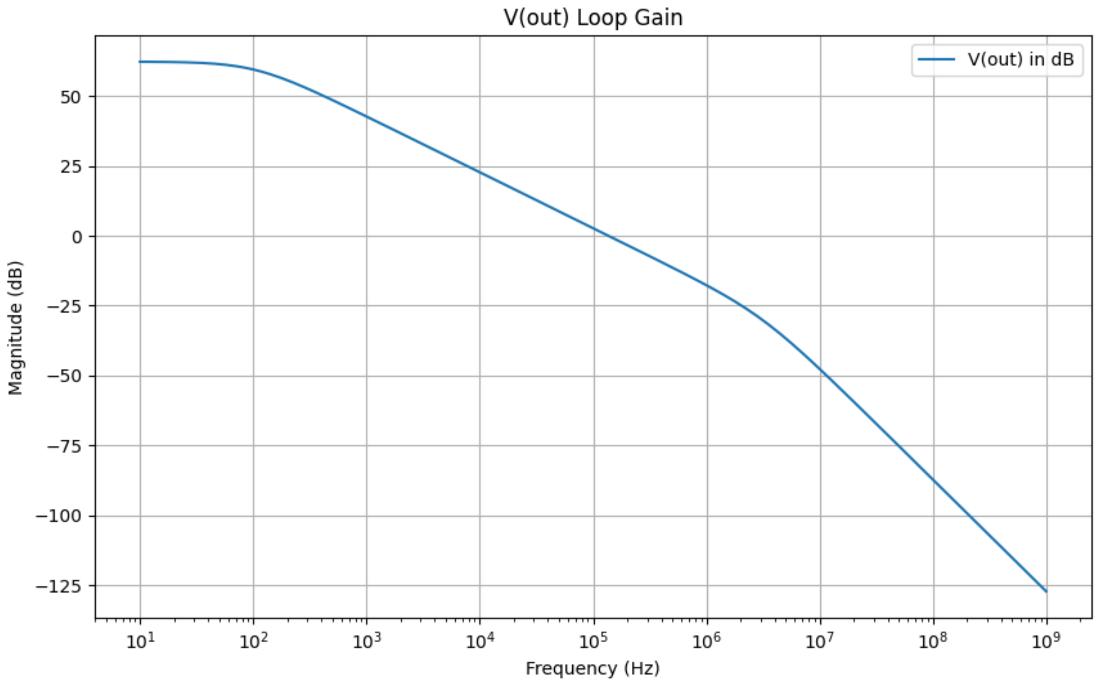


Figure 26: loop gain of output

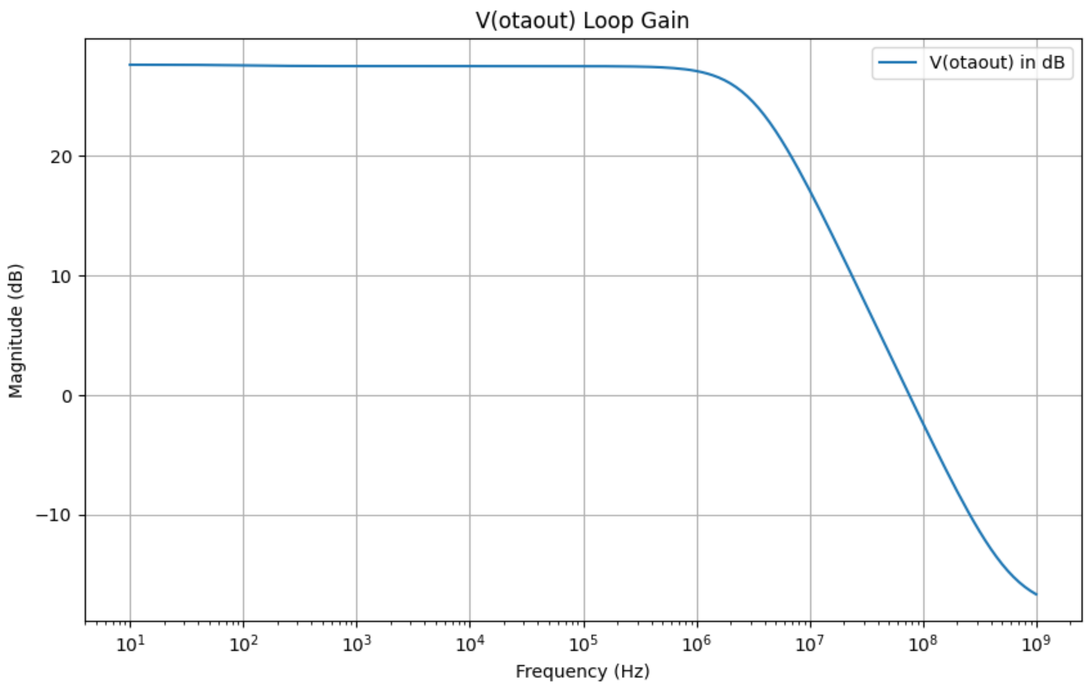


Figure 27: loop gain of OTA

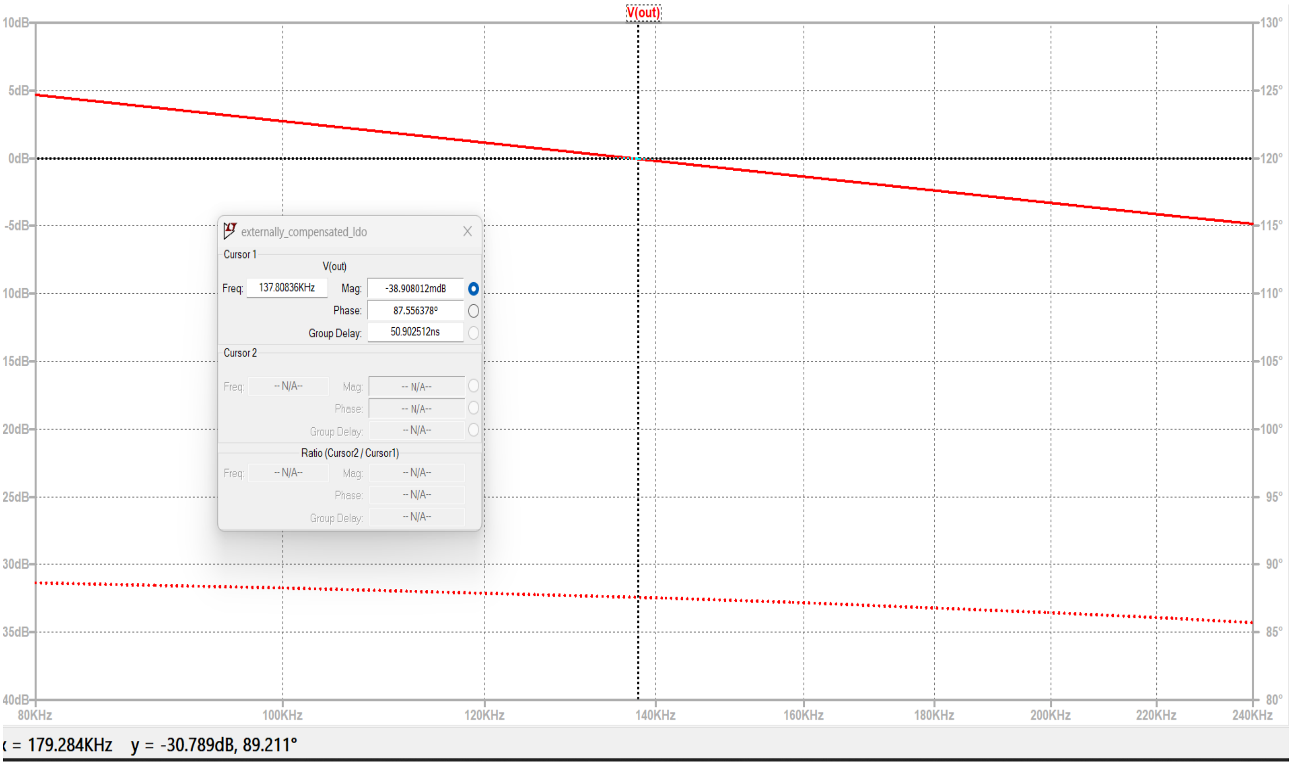


Figure 28: Phase Margin

The phase margin obtained is 87.55 degrees. This value is more than that of the value obtained for heavy load. Thus proving the point that for light load we get a better phase margin as the 1st pole and the 2nd pole are far apart.

Case 2:- Open Loop PSRR calculation

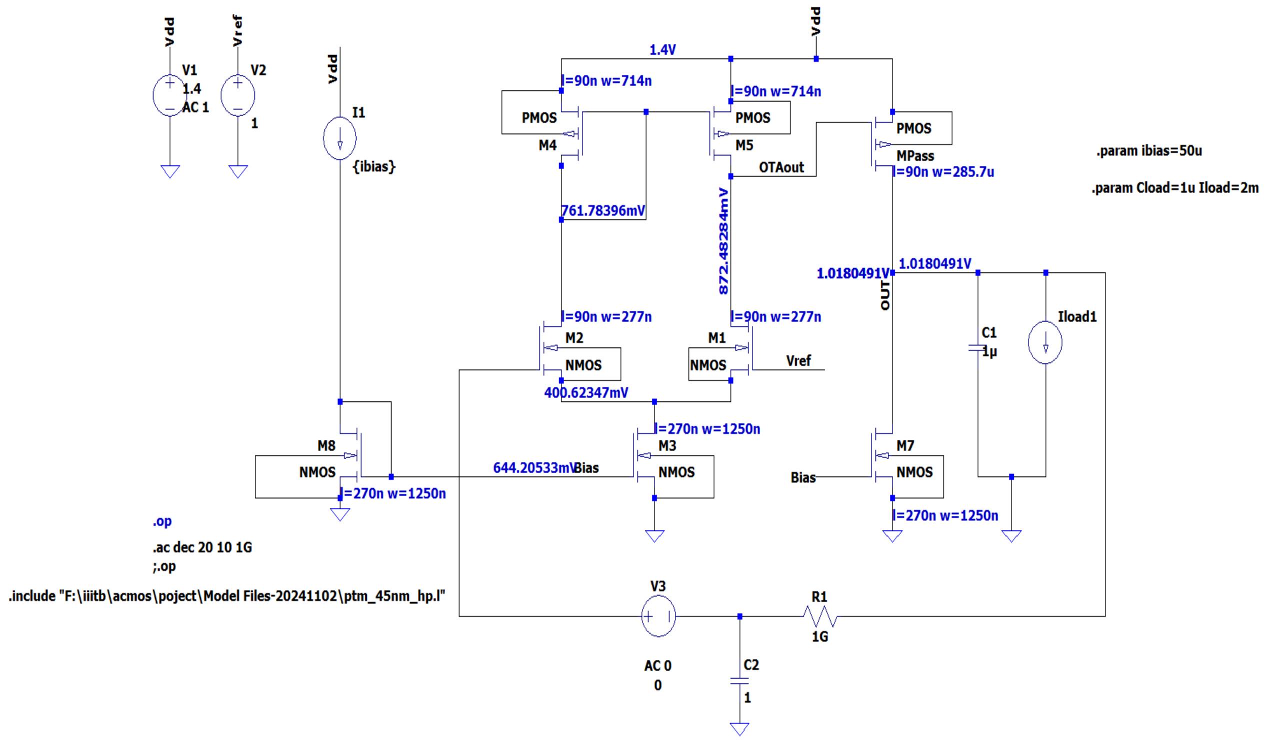


Figure 29: Schematic

Open loop PSRR plots:-

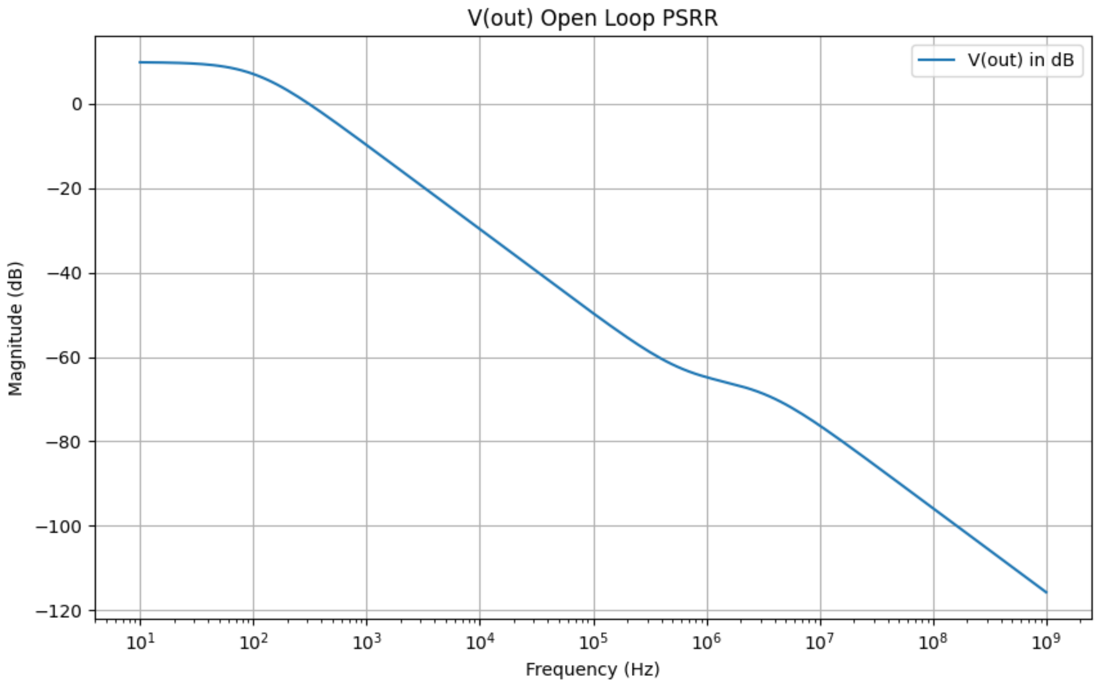


Figure 30: Open loop psrr of output

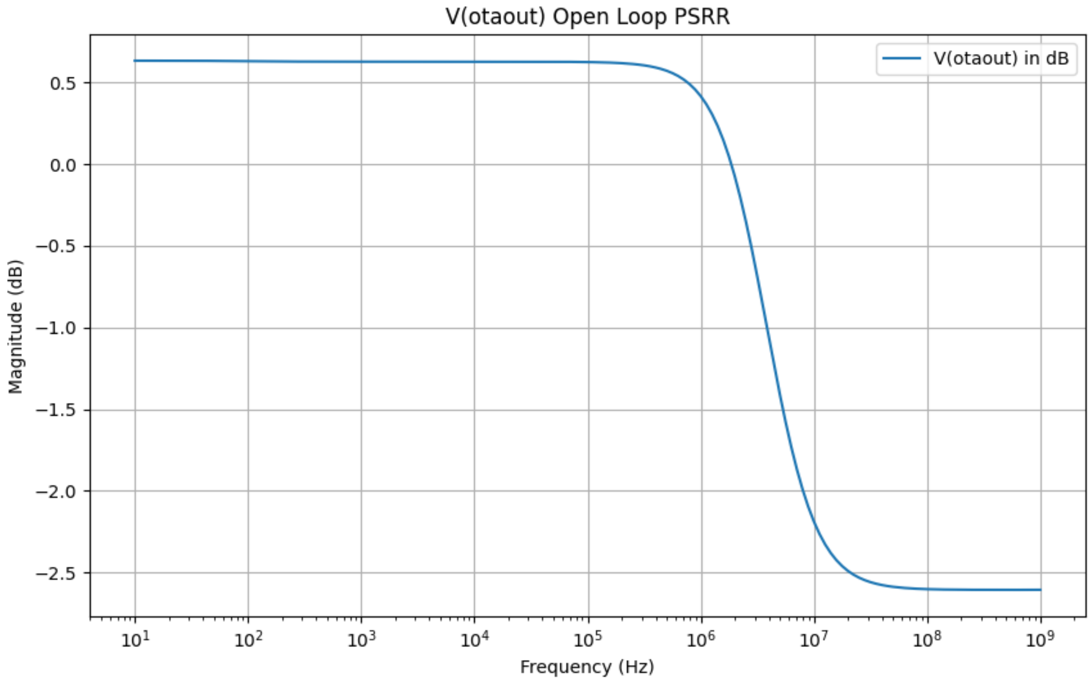


Figure 31: Open loop psrr of OTA

Case 3:- Closed loop PSRR calculation

Schematic

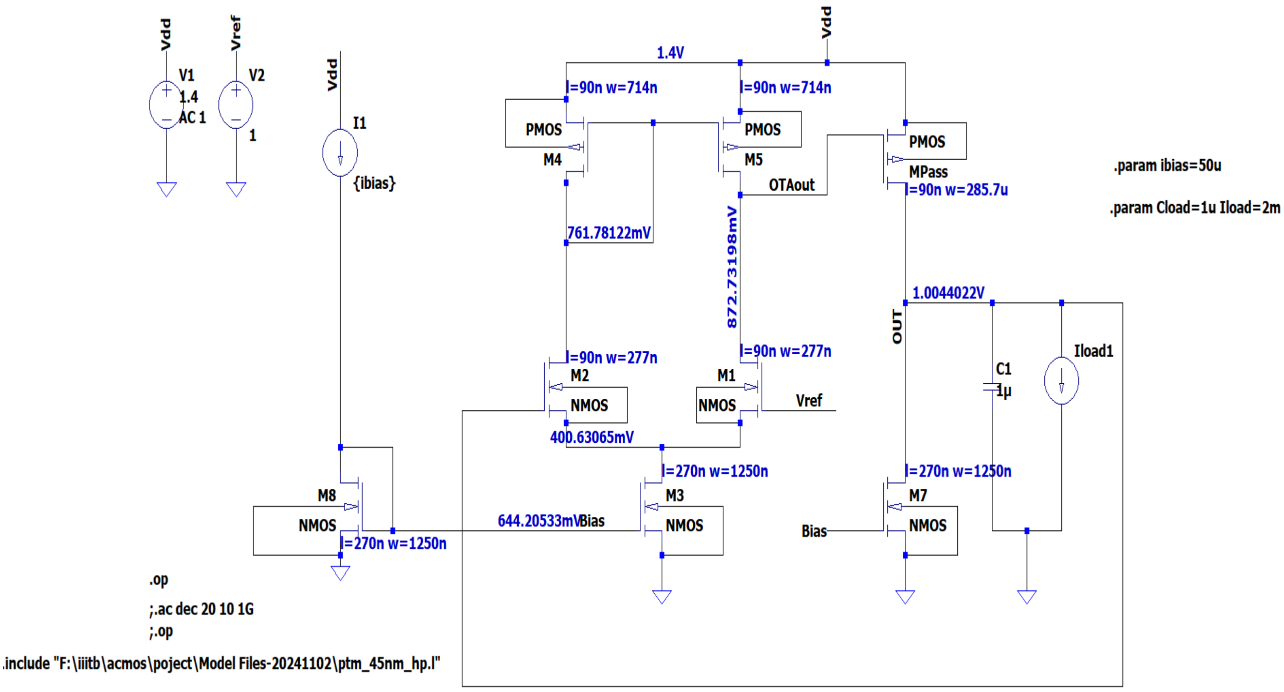


Figure 32: Schematic

Close loop PSRR plots:-

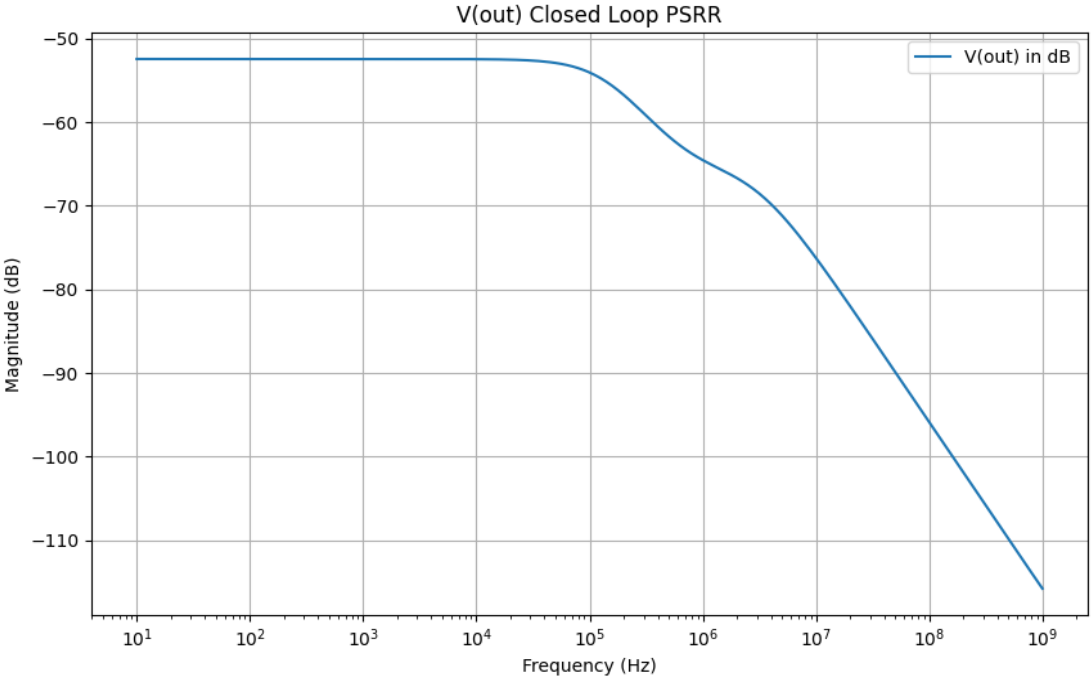


Figure 33: close loop psrr of output

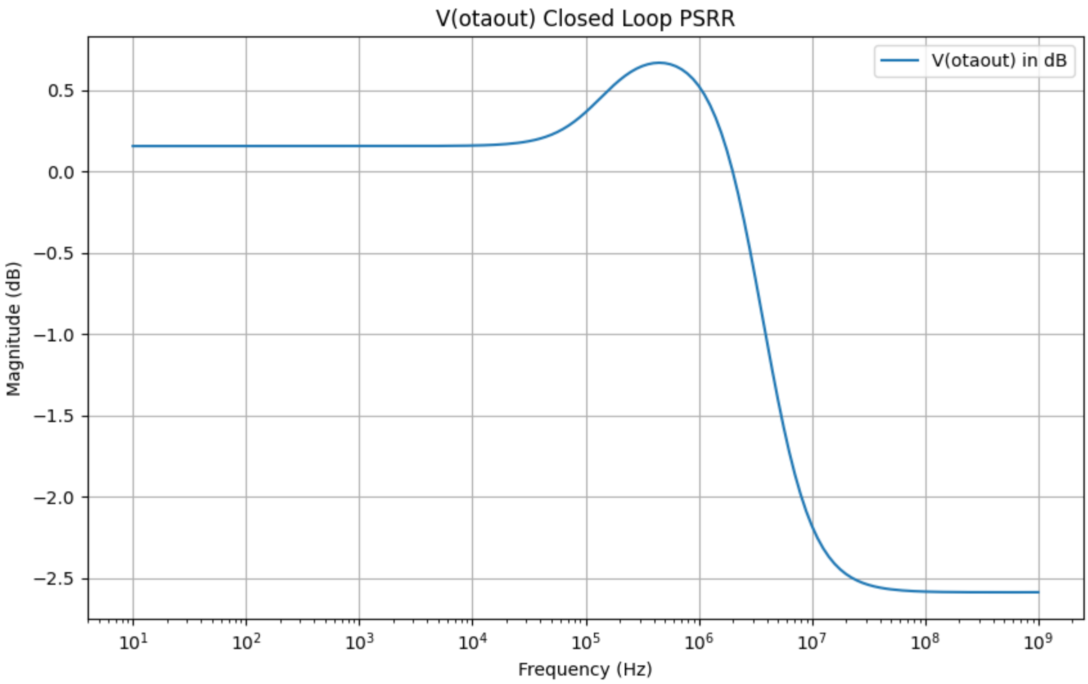


Figure 34: close loop psrr of OTA

8. Transient Simulation Results

We have given a pulse at the load with a rise time and fall time of 1u. Also the period of the pulse is 10m with a 50% duty cycle. From the below figure we can understand that the output is able to settle within the specified range of time. We are not able to observe any overshoot or undershoot in the output.

Schematic:-

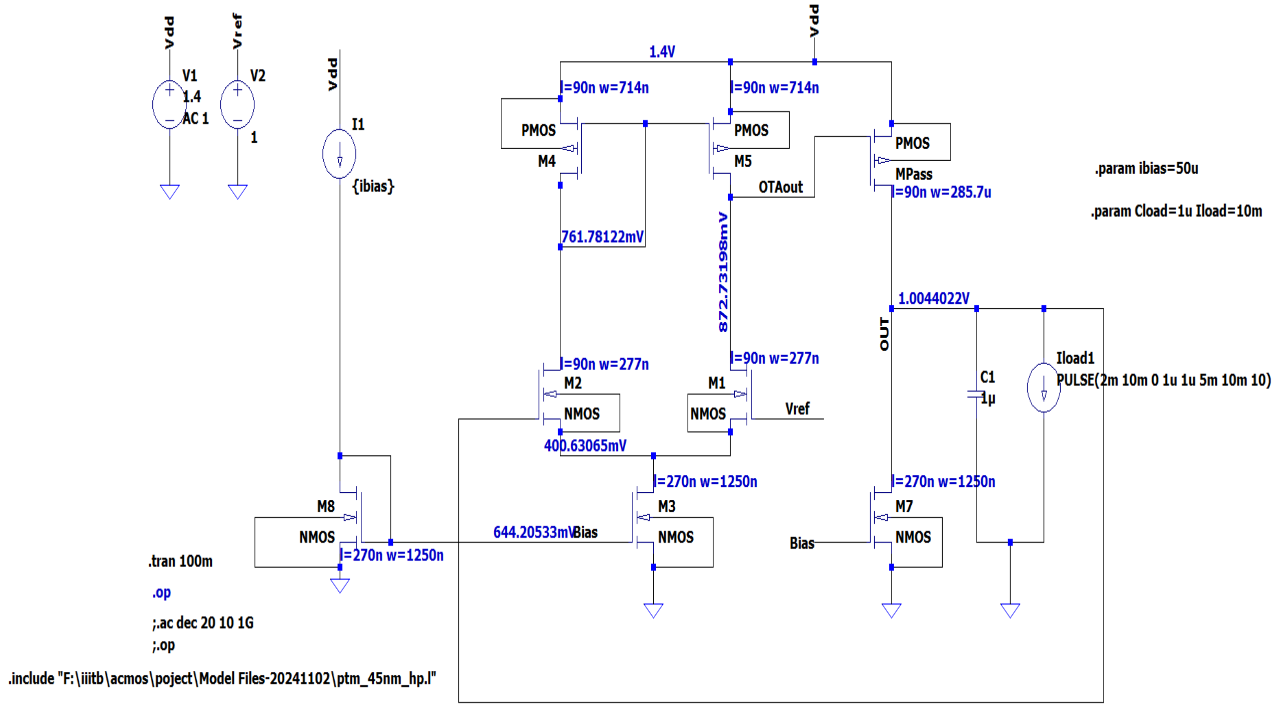


Figure 35: Schematic

Plots:-

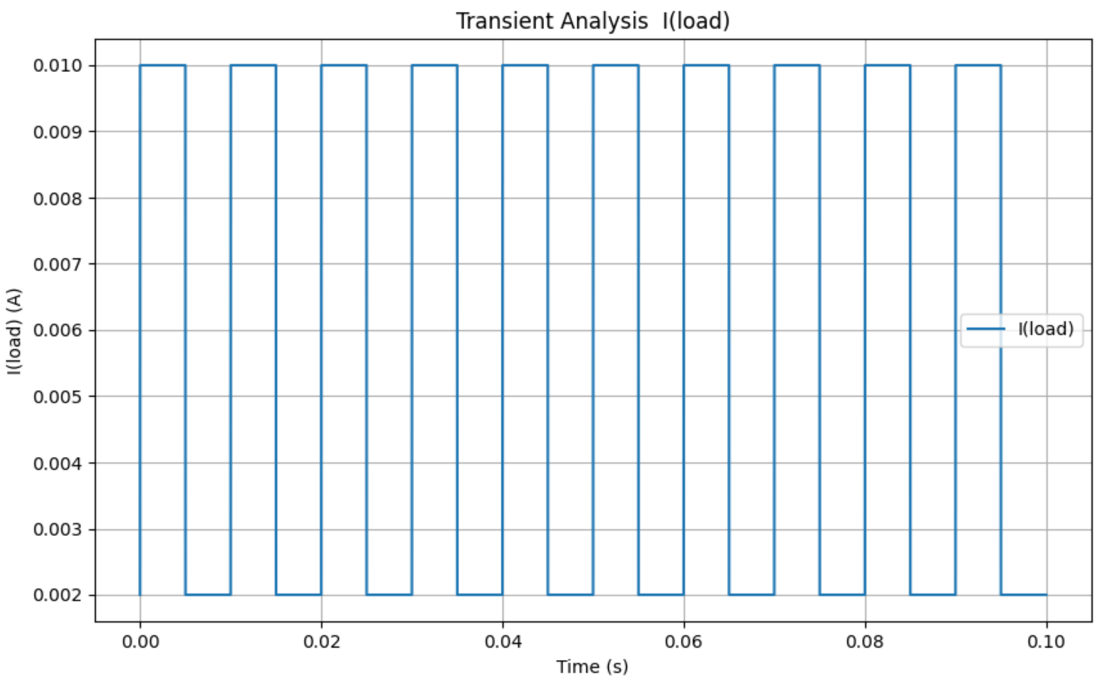


Figure 36: I_{load}

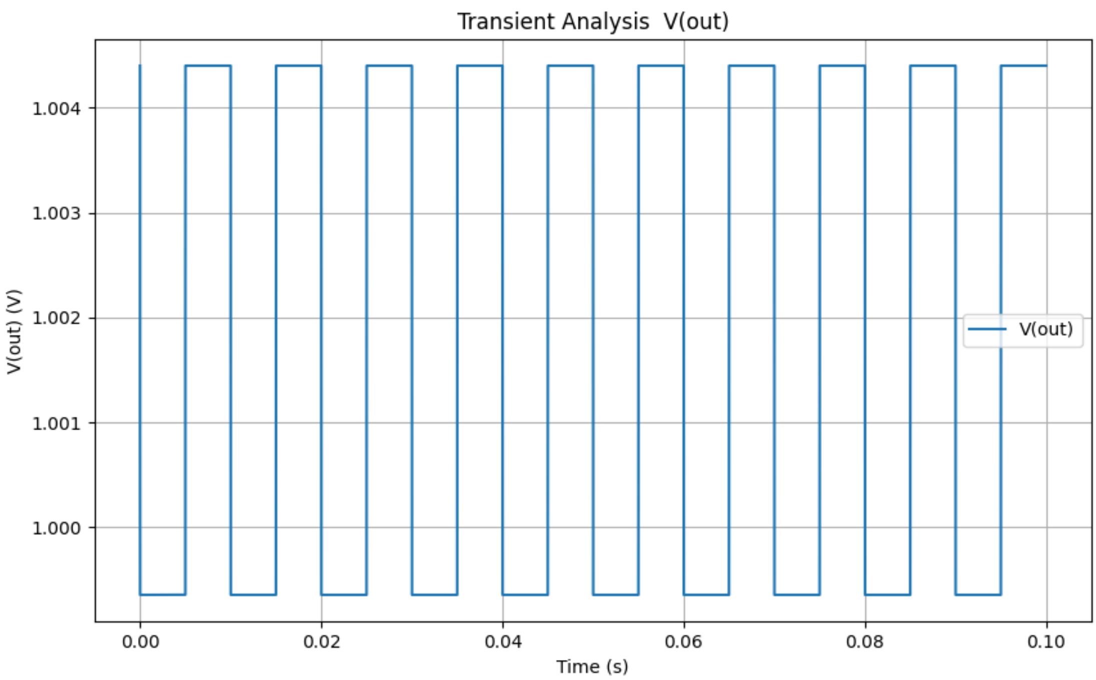


Figure 37: output voltage

9. Simulation vs. Hand Calculations

For Passfet HEAVY LOAD

Hand Calculation

- $r_o = 500\,\Omega$
- $g_m = 0.1\,\text{A/V}$
- W_{p1} (first pole location) = 2k
- $g_m r_o = 50$
- $C_L = 1u$
- $C_g g = 0.568p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 393\,\Omega$
- $g_m = 0.102\,\text{A/V}$
- W_{p1} (first pole location) = 2.54k
- $g_m r_o = 40.086$

Table 8: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	500.00	395.25	21.0%
g_m (A/V)	0.1	0.102	1.9%
$g_m * r_o$	50	40.316	19.36%
W_{p1} (Hz)	2k	2.53k	20.94%
W_{p2} (Hz)	22M	17.85M	18.86%
W_{ugb} (Hz)	2M	2.53M	20.94%
r_{odiff} (ohm)	80k	98.619k	18.87%
g_{mdiff} (A/V)	250u	255u	1.96%

max width=

Name	mpass	m5	m4	m3	m7	m2	m1	m8
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-1.01E-02	-2.46E-05	-2.46E-05	4.94E-05	5.08E-05	2.46E-05	2.47E-05	5.00E-05
Vgs	-6.43E-01	-6.37E-01	-6.37E-01	6.44E-01	6.44E-01	6.02E-01	6.03E-01	6.44E-01
Vds	-3.87E-01	-6.43E-01	-6.37E-01	3.97E-01	1.01E+00	3.66E-01	3.60E-01	6.44E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.84E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	4.69E-01
Vdsat	-1.72E-01	-1.70E-01	-1.70E-01	1.81E-01	1.82E-01	1.44E-01	1.44E-01	1.82E-01
Gm	1.02E-01	2.56E-04	2.55E-04	4.34E-04	4.46E-04	2.40E-04	2.41E-04	4.40E-04
Gds	2.54E-03	5.07E-06	5.07E-06	3.41E-06	2.03E-06	4.94E-06	5.03E-06	2.21E-06
Gmb	2.16E-02	5.40E-05	5.39E-05	1.04E-04	1.07E-04	5.55E-05	5.56E-05	1.05E-04
Cbd	1.28E-13	3.03E-16	3.03E-16	5.60E-16	4.96E-16	1.25E-16	1.25E-16	5.30E-16
Cbs	2.29E-13	5.71E-16	5.71E-16	1.00E-15	1.00E-15	2.22E-16	2.22E-16	1.00E-15
ro	3.94E+02	1.97E+05	1.97E+05	2.93E+05	4.93E+05	2.02E+05	1.99E+05	4.52E+05
gm*ro	4.02E+01	5.05E+01	5.03E+01	1.27E+02	2.20E+02	4.86E+01	4.79E+01	1.99E+02

Table 9: Updated Transistor Parameter Table

For Passfet LIGHT LOAD

Hand Calculation

- $r_o = 2500\,\Omega$
- $g_m = 0.02\,\text{A/V}$
- W_{p1} (first pole location) = 400
- $g_m r_o = 50$
- $C_L = 1u$
- $C_g g = 0.1136p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 1503.7\,\Omega$
- $g_m = 0.0364\,\text{A/V}$
- W_{p1} (first pole location) = 665.02
- $g_m r_o = 54.7$

Table 10: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	2500.00	1503.7	39.0%
g_m (A/V)	0.02	0.0364	45%
$g_m * r_o$	50	54.7	8.5%
W_{p1} (Hz)	400	665.02	39.8%
W_{p2} (Hz)	110M	84.4M	23.2%
W_{ugb} (Hz)	400k	665.02k	39.8%
r_{odiff} (ohm)	80k	104.2k	23.07%
g_{mdiff} (A/V)	250u	253u	1.185%

max width=

Name	mpass	m5	m4	m3	m7	m2	m1	m8
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-2.05E-03	-2.44E-05	-2.50E-05	4.94E-05	5.08E-05	2.50E-05	2.44E-05	5.00E-05
Vgs	-5.28E-01	-6.38E-01	-6.38E-01	6.44E-01	6.44E-01	6.04E-01	5.99E-01	6.44E-01
Vds	-3.82E-01	-5.28E-01	-6.38E-01	4.01E-01	1.02E+00	3.61E-01	4.72E-01	6.44E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.86E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	4.69E-01
Vdsat	-9.28E-02	-1.70E-01	-1.71E-01	1.81E-01	1.82E-01	1.45E-01	1.43E-01	1.82E-01
Gm	3.64E-02	2.53E-04	2.57E-04	4.34E-04	4.46E-04	2.42E-04	2.41E-04	4.40E-04
Gds	6.65E-04	5.30E-06	5.12E-06	3.36E-06	2.03E-06	5.06E-06	4.27E-06	2.21E-06
Gmb	7.50E-03	5.34E-05	5.43E-05	1.04E-04	1.07E-04	5.58E-05	5.56E-05	1.05E-04
Cbd	1.28E-13	3.10E-16	3.03E-16	5.59E-16	4.96E-16	1.25E-16	1.22E-16	5.30E-16
Cbs	2.29E-13	5.71E-16	5.71E-16	1.00E-15	1.00E-15	2.22E-16	2.22E-16	1.00E-15
ro	1.50E+03	1.89E+05	1.95E+05	2.98E+05	4.93E+05	1.98E+05	2.34E+05	4.52E+05
gm*ro	5.47E+01	4.77E+01	5.02E+01	1.29E+02	2.20E+02	4.78E+01	5.64E+01	1.99E+02

Table 11: Transistor Parameter Table

Internally Compensated LDO

1. Specifications

Table 12: Specifications Summary

Parameter	Value
Vin	1.4V
Vout	1V
PSRR	60dB
Iload (min)	2mA
Iload (max)	10mA
Cload	2nF
Iquiescent	50uA
Transient duration	1u

we have made three schematics in LTSpice to calculate the three conditions. We have made a simulation artifact for the same.

Case 1 : Loop Gain Analysis
Case 2 : Open Loop PSRR Calculation
Case 3 : Closed Loop PSRR Calculation

Light Load (2mA)

Schematic

Case 1:- Loop gain analysis:-

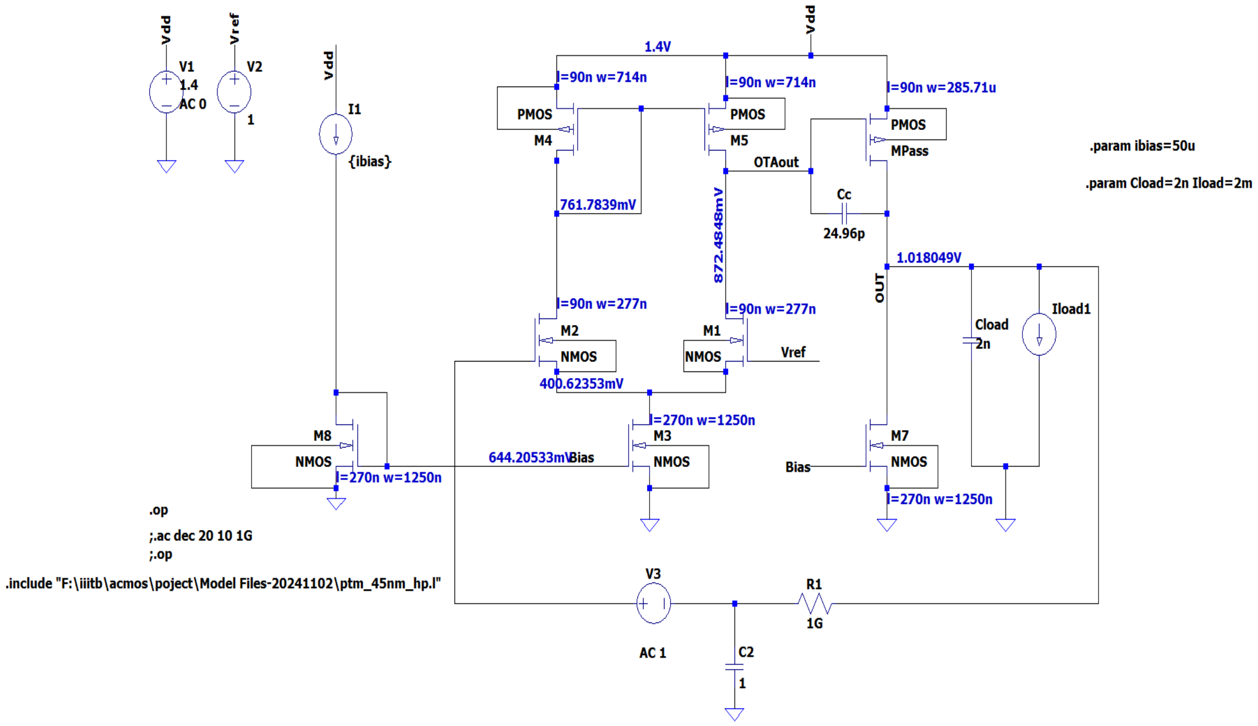


Figure 38: Schematic

Explanation of the artifact used:-

Output Log File:-

```
SPICE Output Log: F:\iiitb\acmos\poject\internally_compensated\internally_compensated_ldo.log
LTspice 24.0.12 for Windows
Circuit: * F:\iiitb\acmos\poject\internally_compensated\internally_compensated_ldo.a
Start Time: Wed Dec  4 12:00:07 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:      mpass       m5          m4          m3          m7
Model:      pmos        pmos        pmos        nmos        nmos
Id:      -2.05e-03   -2.44e-05   -2.50e-05    4.94e-05    5.08e-05
Vgs:     -5.28e-01   -6.38e-01   -6.38e-01    6.44e-01    6.44e-01
Vds:     -3.82e-01   -5.28e-01   -6.38e-01    4.01e-01    1.02e+00
Vbs:      0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:     -4.87e-01   -4.86e-01   -4.84e-01    4.69e-01    4.69e-01
Vdsat:   -9.28e-02   -1.70e-01   -1.71e-01    1.81e-01    1.82e-01
Gm:       3.64e-02    2.53e-04    2.57e-04    4.34e-04    4.46e-04
Gds:      6.65e-04    5.30e-06    5.12e-06    3.36e-06    2.03e-06
Gmb       7.50e-03    5.34e-05    5.43e-05    1.04e-04    1.07e-04
Cbd:      1.28e-13    3.10e-16    3.03e-16    5.59e-16    4.96e-16
Cbs:      2.29e-13    5.71e-16    5.71e-16    1.00e-15    1.00e-15

Name:      m2          m1          m8
Model:     nmos        nmos        nmos
Id:       2.50e-05    2.44e-05    5.00e-05
Vgs:      6.04e-01    5.99e-01    6.44e-01
Vds:      3.61e-01    4.72e-01    6.44e-01
Vbs:      0.00e+00    0.00e+00    0.00e+00
Vth:      4.66e-01    4.65e-01    4.69e-01
Vdsat:    1.45e-01    1.43e-01    1.82e-01
Gm:       2.42e-04    2.41e-04    4.40e-04
Gds:      5.06e-06    4.27e-06    2.21e-06
Gmb       5.58e-05    5.56e-05    1.05e-04
Cbd:      1.25e-16    1.22e-16    5.30e-16
Cbs:      2.22e-16    2.22e-16    1.00e-15

Total elapsed time: 0.178 seconds.
```

Figure 39: Output Log Detail

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	Type	V_{ds} (V)	V_{gs}/V_{sg} (V)	V_t (V)	$V_{gs}/V_{sg} - V_t$ (V)	Operating Region
M1	NMOS	0.472	0.599	0.465	0.134	Saturation
M2	NMOS	0.361	0.604	0.466	0.138	Saturation
M3	NMOS	0.401	0.644	0.469	0.175	Saturation
M4	PMOS	0.638	0.638	0.484	0.267	Saturation
M5	PMOS	0.528	0.638	0.487	0.151	Saturation
Mpass	PMOS	0.382	0.528	0.487	0.041	Saturation
M7	NMOS	1.02	0.644	0.469	0.175	Saturation
M8	NMOS	0.644	0.644	0.469	0.1.75	Saturation

Table 13: Transistor Parameters and Operating Regions

Loop gain plots:-

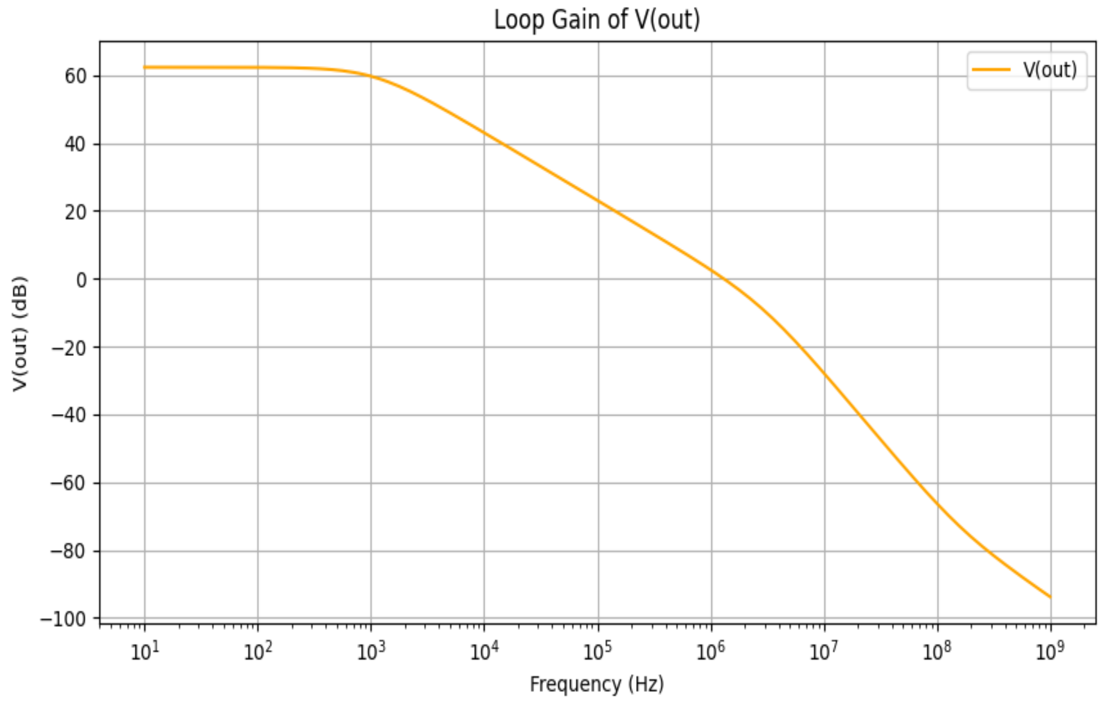


Figure 40: Loop gain of LDO

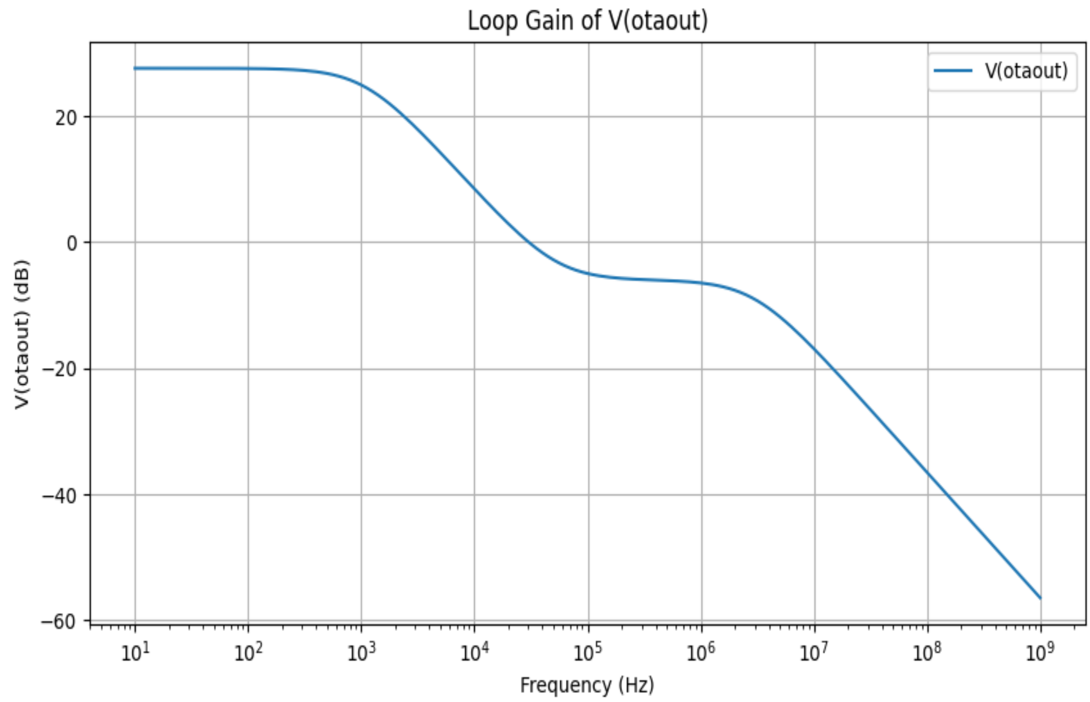


Figure 41: Loop gain of OTA

Phase margin

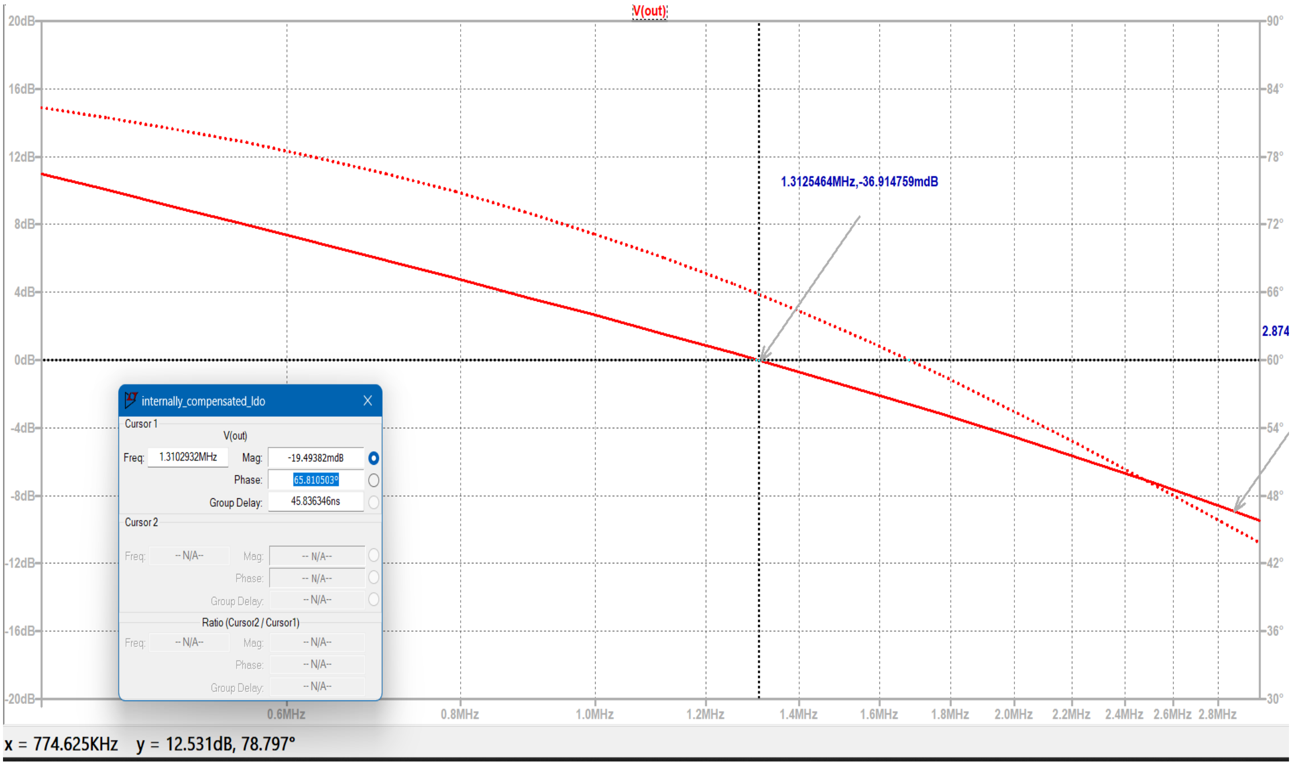


Figure 42: Phase Margin

Case 2:- Open Loop PSRR calculation

Schematic

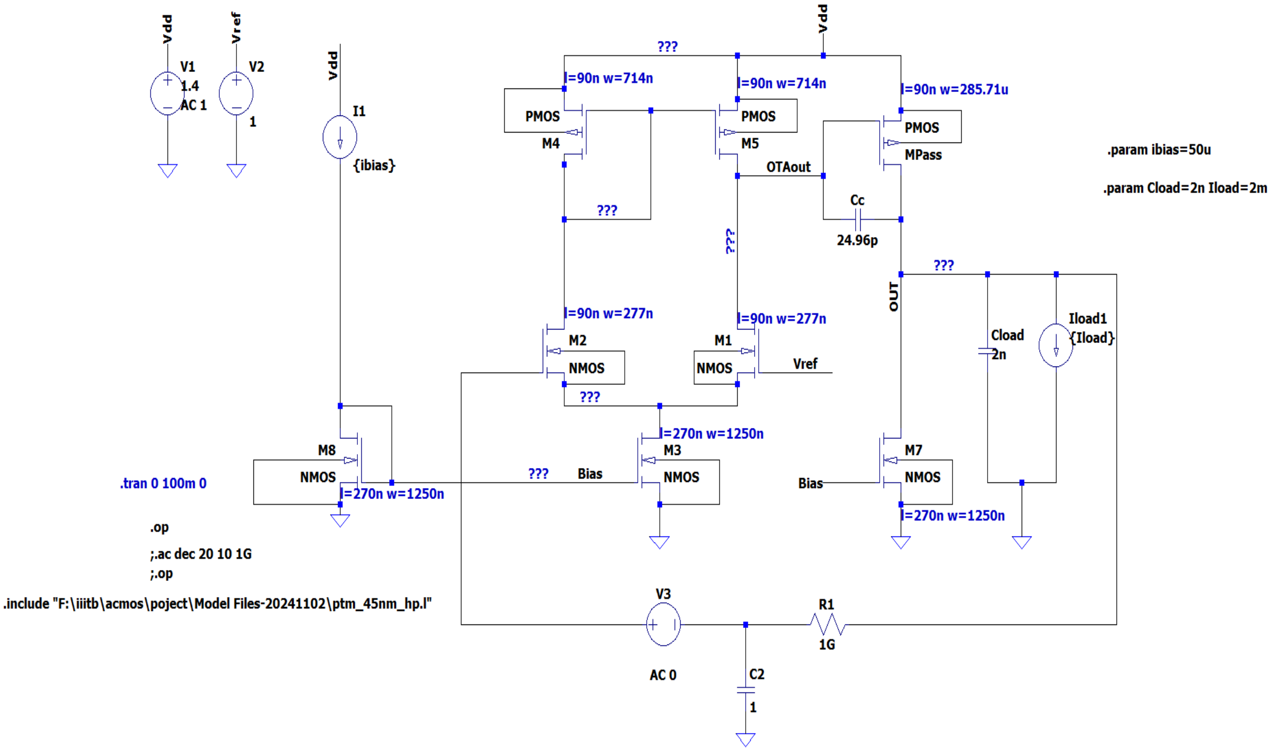


Figure 43: Schematic

Open loop PSRR plots:-

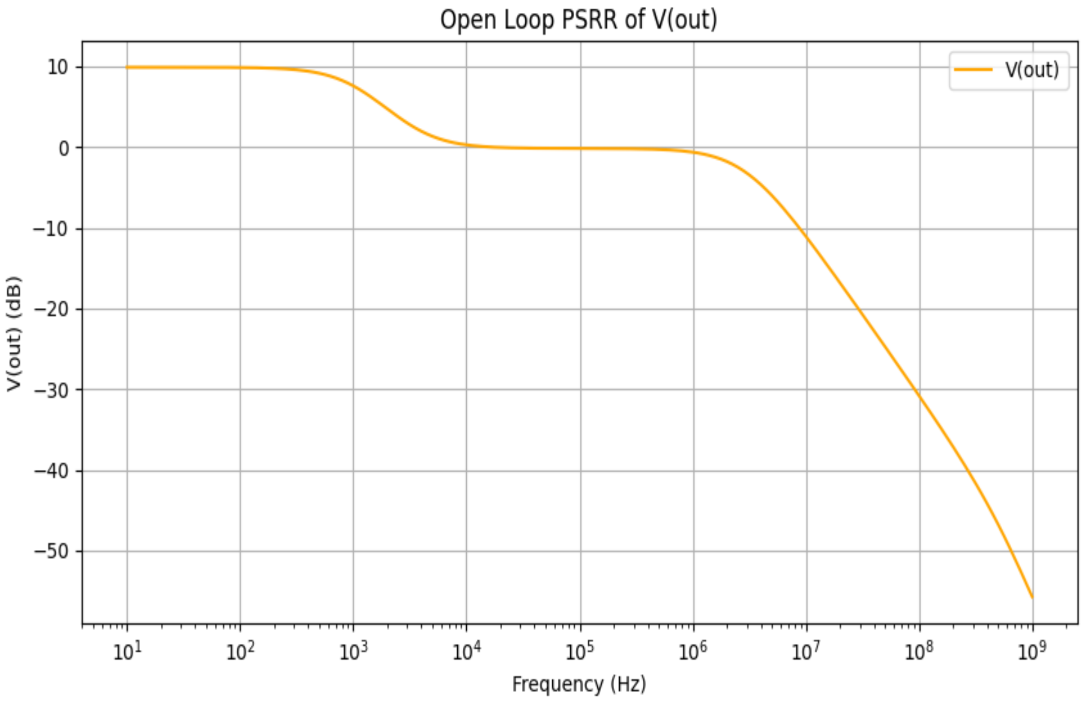


Figure 44: Open loop psrr of LDO

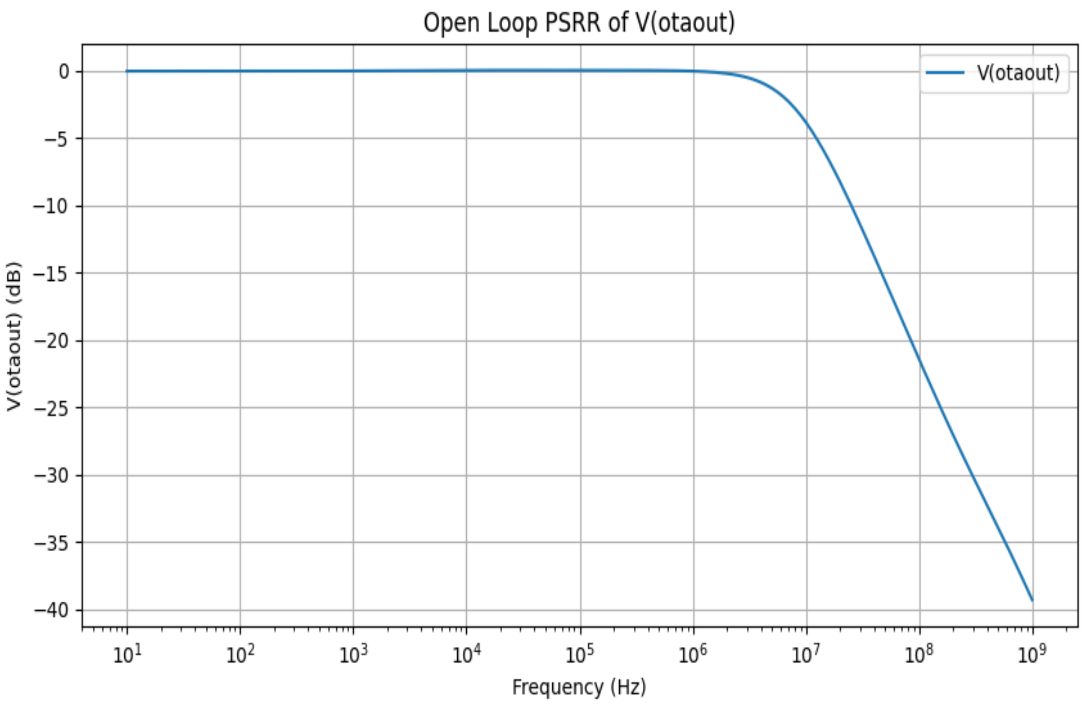


Figure 45: Open loop psrr of OTA

Case 3:- Closed loop PSRR calculation

Schematic

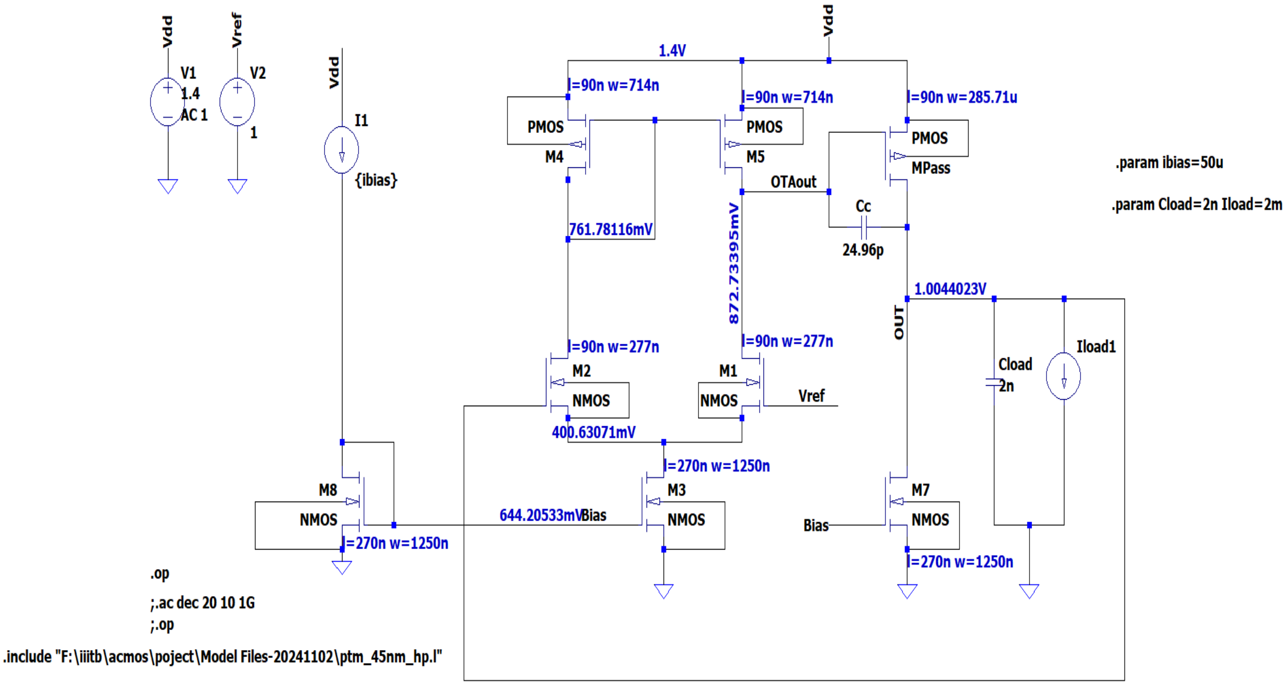


Figure 46: Schematic

Close loop psrr plots:-

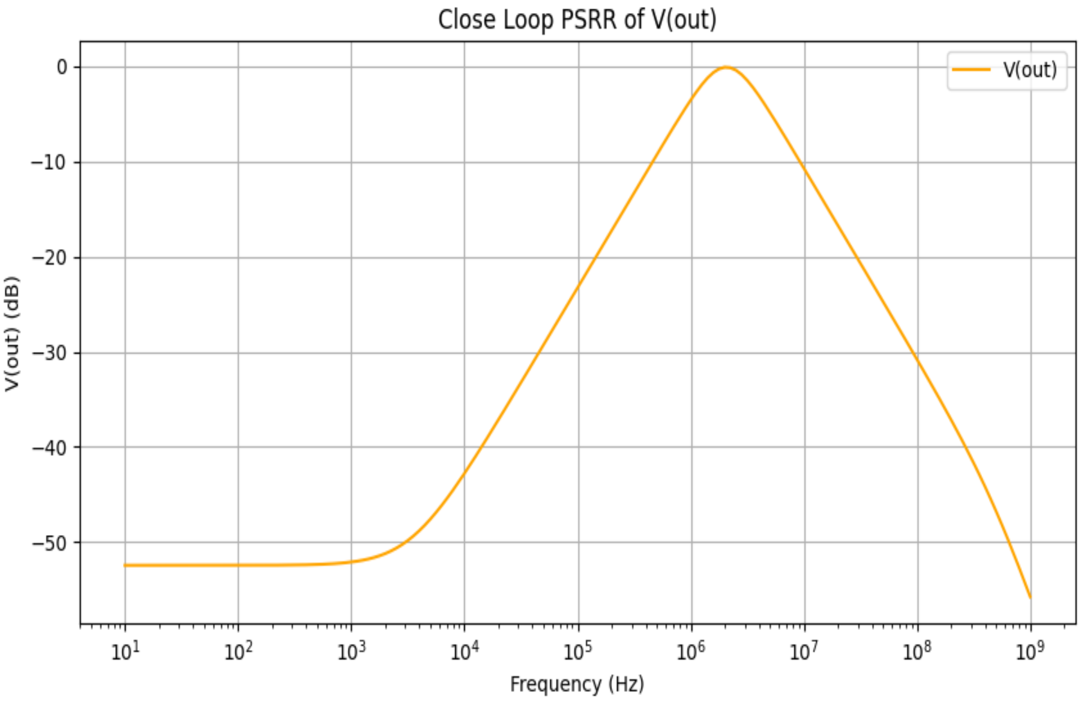


Figure 47: Close loop psrr of LDO

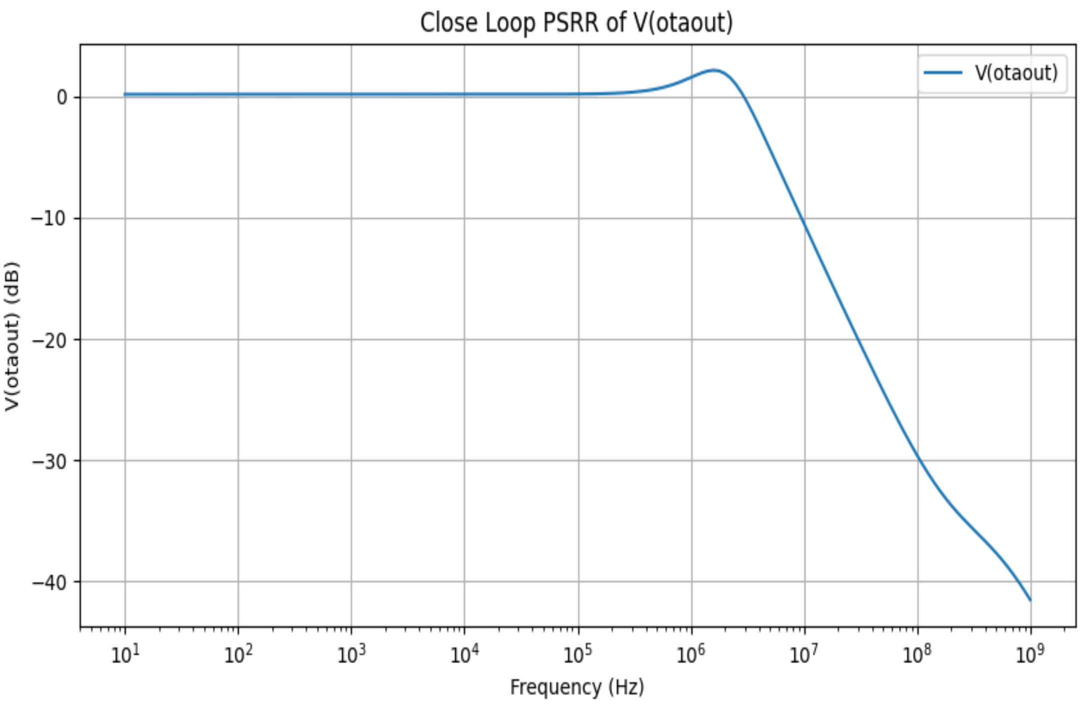


Figure 48: Close loop psrr of OTA

Heavy Load (10mA)

Schematic

Case 1:- Loop gain analysis:-

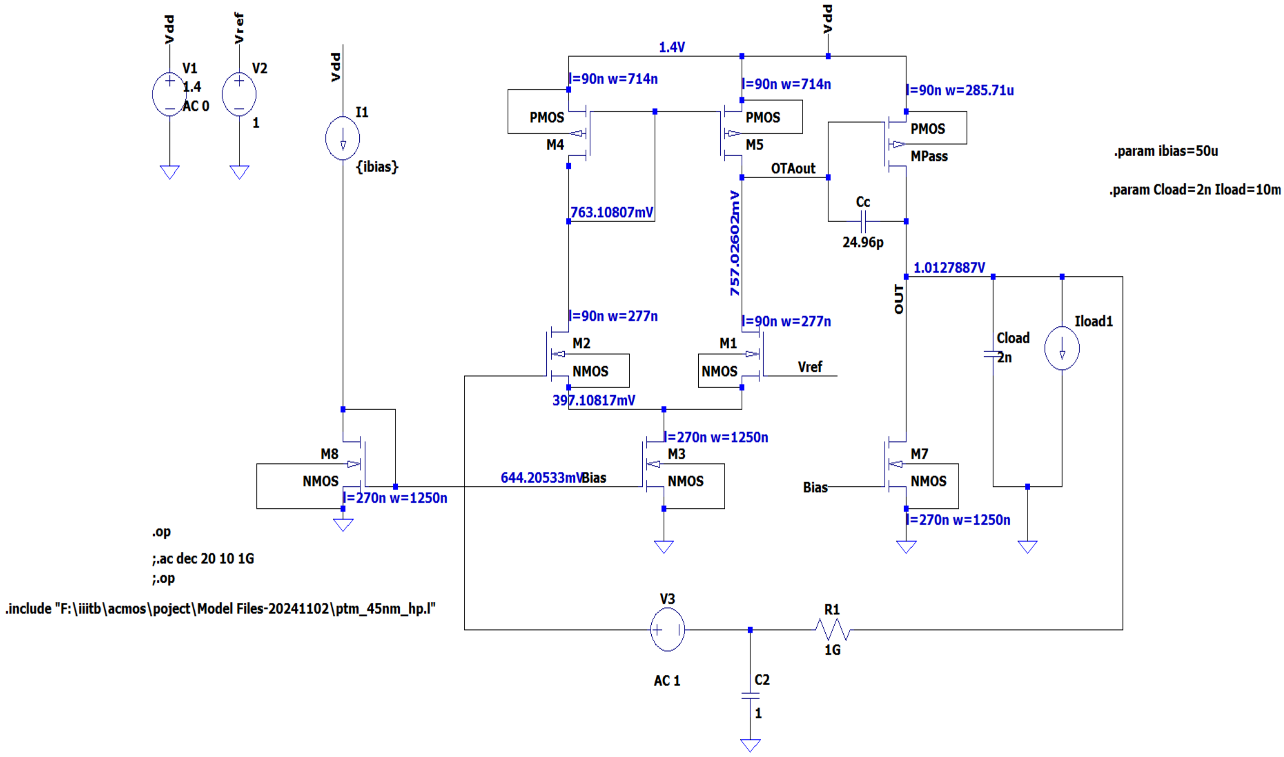


Figure 49: Schematic

Explanation of the artifact used:-

Output Log File:-

```
LTspice 24.0.12 for Windows
Circuit: * F:\iiitb\acmos\poject\internally_compensated\internally_compensated_ldo.a
Start Time: Wed Dec  4 11:22:29 2024
solver = Normal
Maximum thread count: 8
tnom = 27
temp = 27
method = modified trap
Direct Newton iteration for .op point succeeded.
Semiconductor Device Operating Points:
                        --- BSIM4 MOSFETS ---
Name:      mpass       m5          m4          m3          m7
Model:      pmos        pmos        pmos        nmos        nmos
Id:       -1.01e-02   -2.46e-05   -2.46e-05    4.94e-05    5.08e-05
Vgs:      -6.43e-01   -6.37e-01   -6.37e-01    6.44e-01    6.44e-01
Vds:      -3.87e-01   -6.43e-01   -6.37e-01    3.97e-01    1.01e+00
Vbs:       0.00e+00    0.00e+00    0.00e+00    0.00e+00    0.00e+00
Vth:      -4.87e-01   -4.84e-01   -4.84e-01    4.69e-01    4.69e-01
Vdsat:    -1.72e-01   -1.70e-01   -1.70e-01    1.81e-01    1.82e-01
Gm:        1.02e-01    2.56e-04    2.55e-04    4.34e-04    4.46e-04
Gds:       2.54e-03    5.07e-06    5.07e-06    3.41e-06    2.03e-06
Gmb        2.16e-02    5.40e-05    5.39e-05    1.04e-04    1.07e-04
Cbd:       1.28e-13    3.03e-16    3.03e-16    5.60e-16    4.96e-16
Cbs:       2.29e-13    5.71e-16    5.71e-16    1.00e-15    1.00e-15

Name:       m2          m1          m8
Model:      nmos        nmos        nmos
Id:        2.46e-05    2.47e-05    5.00e-05
Vgs:       6.02e-01    6.03e-01    6.44e-01
Vds:       3.66e-01    3.60e-01    6.44e-01
Vbs:       0.00e+00    0.00e+00    0.00e+00
Vth:       4.66e-01    4.66e-01    4.69e-01
Vdsat:     1.44e-01    1.44e-01    1.82e-01
Gm:        2.40e-04    2.41e-04    4.40e-04
Gds:       4.94e-06    5.03e-06    2.21e-06
Gmb        5.55e-05    5.56e-05    1.05e-04
Cbd:       1.25e-16    1.25e-16    5.30e-16
Cbs:       2.22e-16    2.22e-16    1.00e-15


Total elapsed time: 0.077 seconds.
```

Figure 50: Output$_{l}og_{d}etails$

From the above file we can verify that all the devices are in saturation as follows:

Transistor Operating Regions Table

This document provides a table summarizing the operating regions of several transistors based on their parameters.

Transistor	**Type**	V_{ds} **(V)**	V_{gs}/V_{sg} **(V)**	V_t **(V)**	$V_{gs}/V_{sg} - V_t$ **(V)**	**Operating Region**
M1	NMOS	0.360	0.603	0.466	0.137	Saturation
M2	NMOS	0.366	0.602	0.466	0.136	Saturation
M3	NMOS	0.397	0.644	0.469	0.175	Saturation
M4	PMOS	0.637	0.637	0.484	0.153	Saturation
M5	PMOS	0.643	0.637	0.484	0.153	Saturation
MPass	PMOS	0.387	0.643	0.487	0.156	Saturation
M7	NMOS	1.01	0.644	0.469	0.173	Saturation
M8	NMOS	0.644	0.644	0.469	0.175	Saturation

Table 14: Transistor Parameters and Operating Regions

Loop gain plots:-

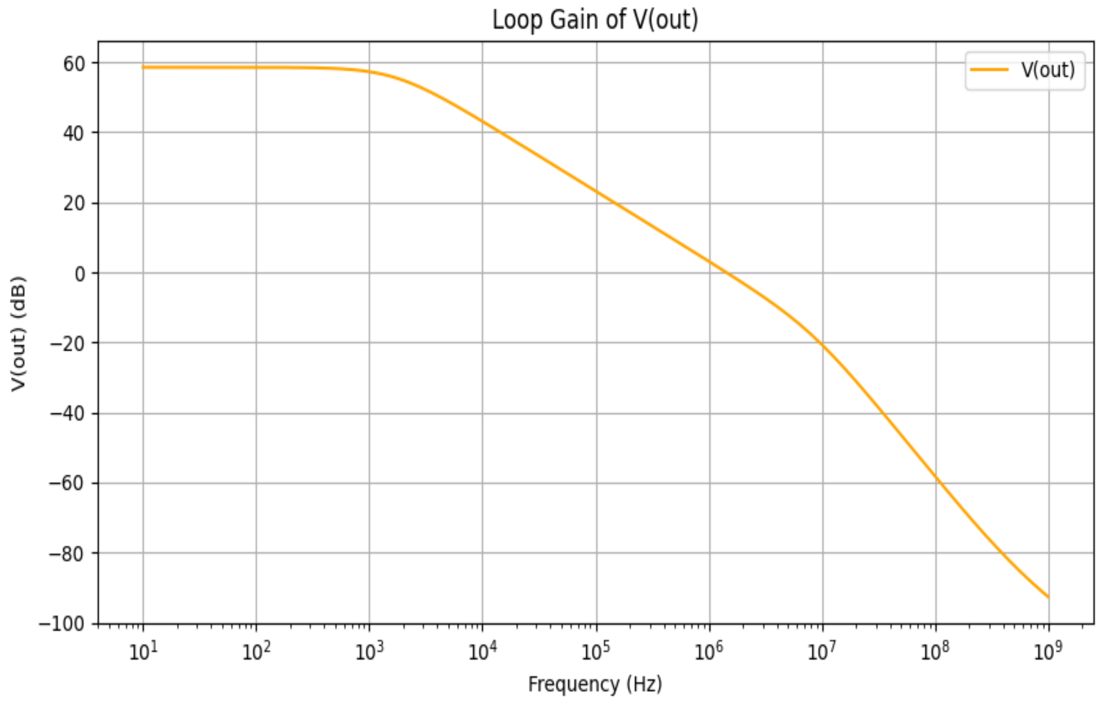


Figure 51: Loop gain of LDO

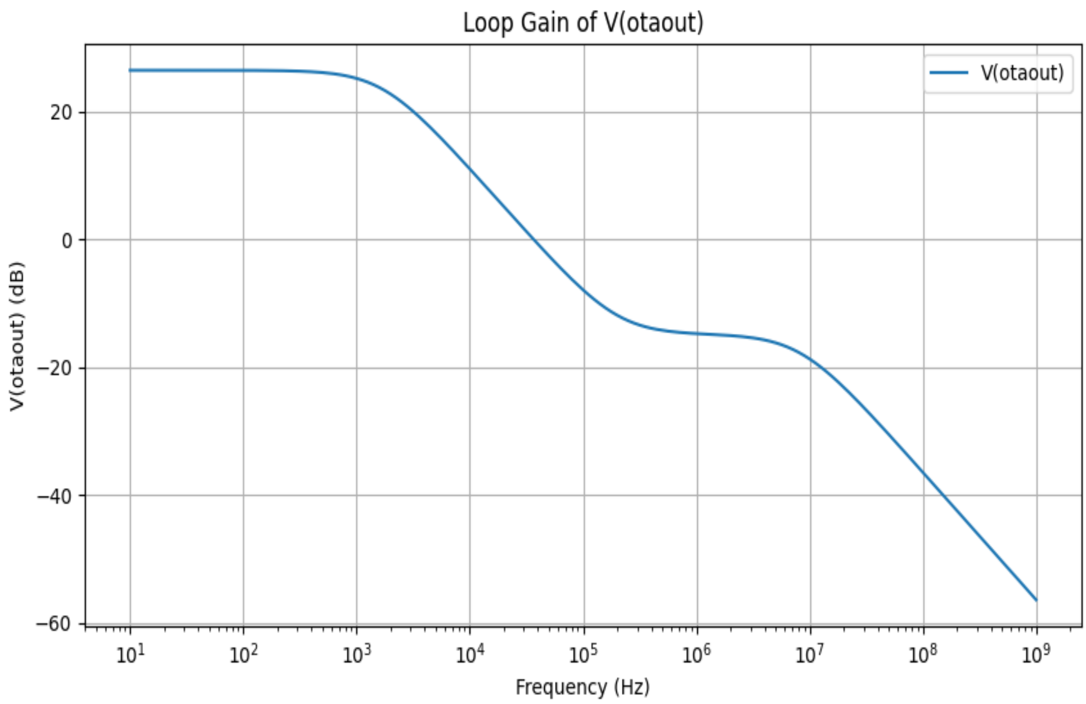


Figure 52: Loop gain of OTA

Phase margin

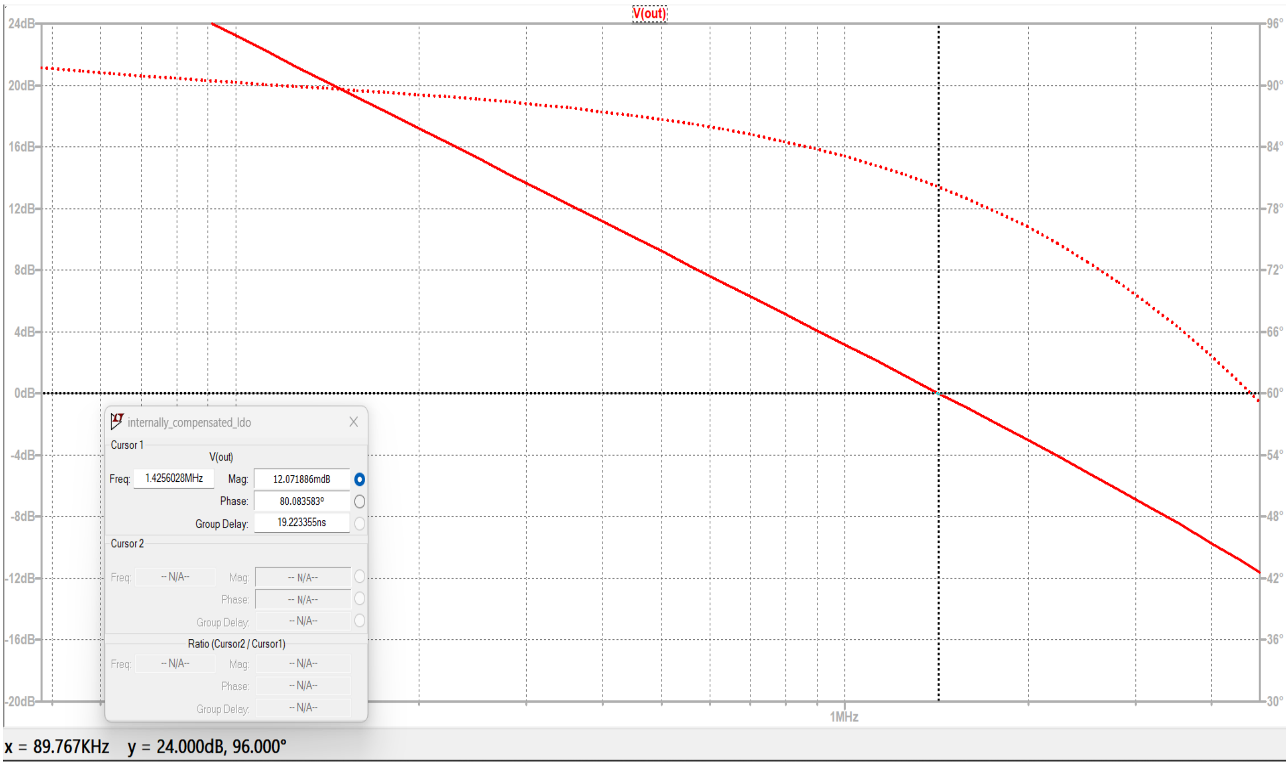


Figure 53: Phase Margin

Case 2:- Open Loop PSRR calculation

Schematic

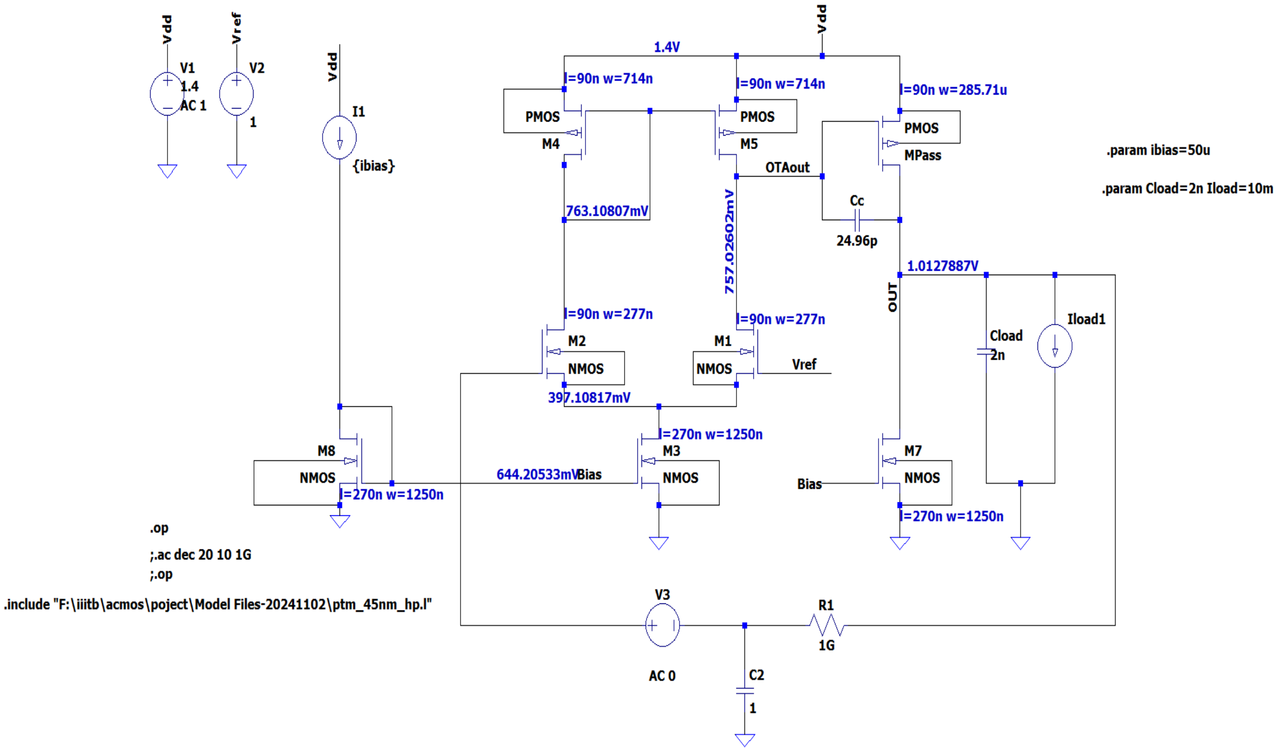


Figure 54: Schematic

Open loop psrr plots:-

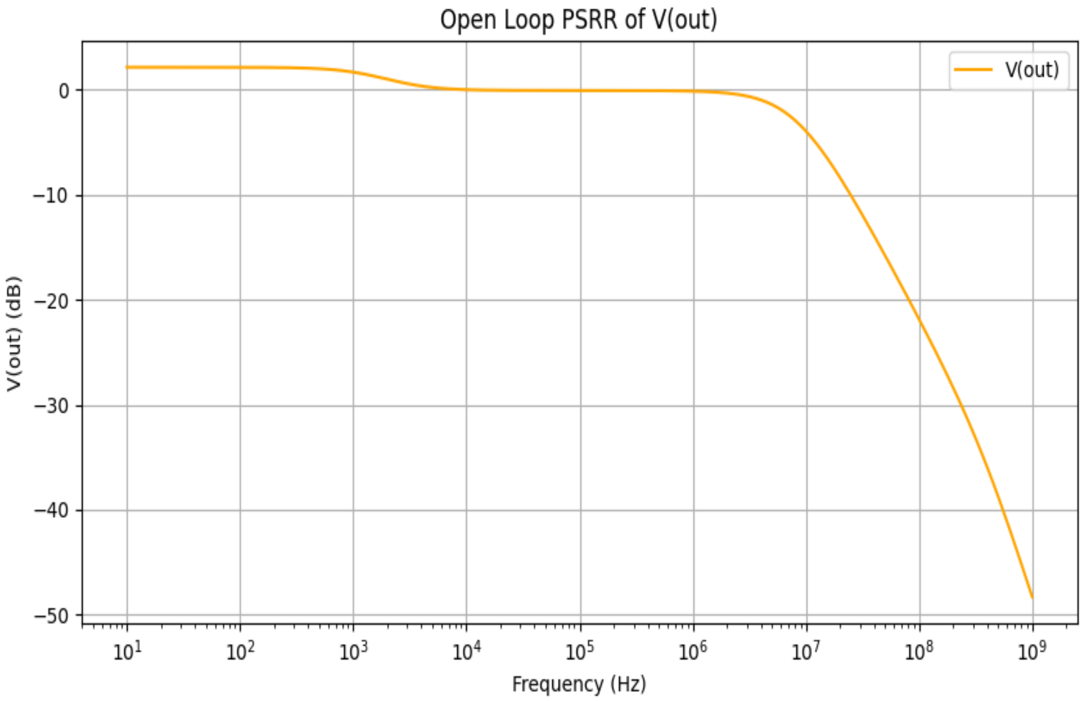


Figure 55: Open Loop PSRR of LDO

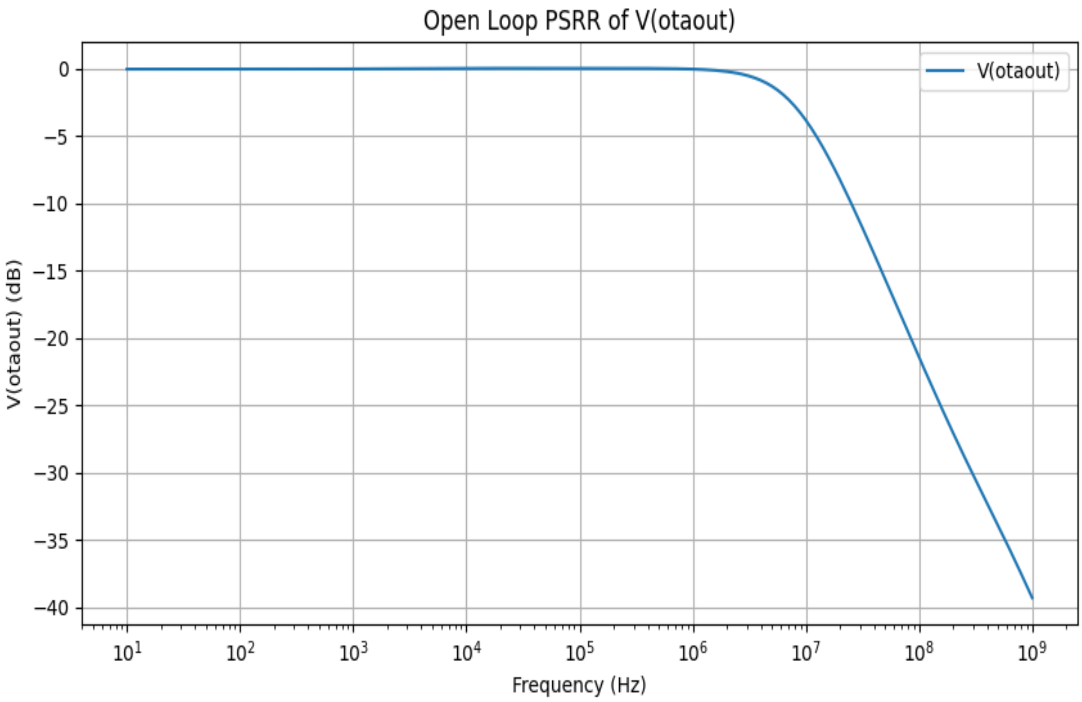


Figure 56: Open Loop PSRR of OTA

Case 3:- Closed loop PSRR calculation

Schematic

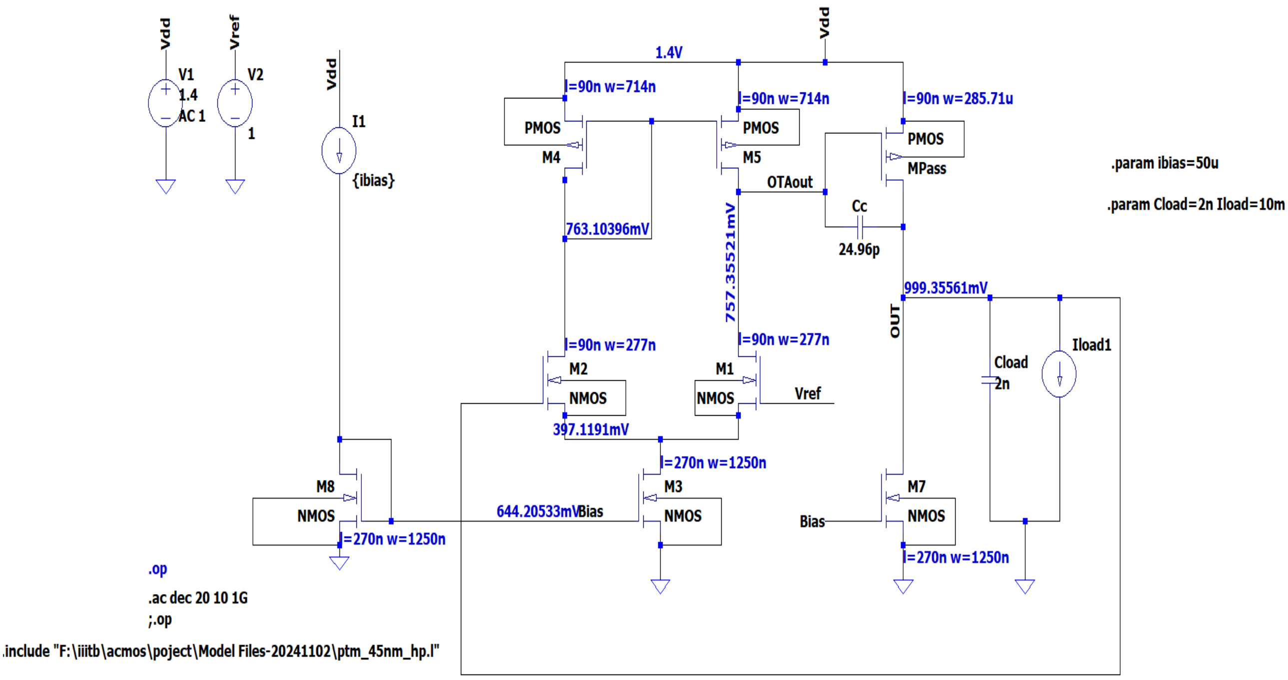


Figure 57: Schematic

C

lose loop psrr plots:-

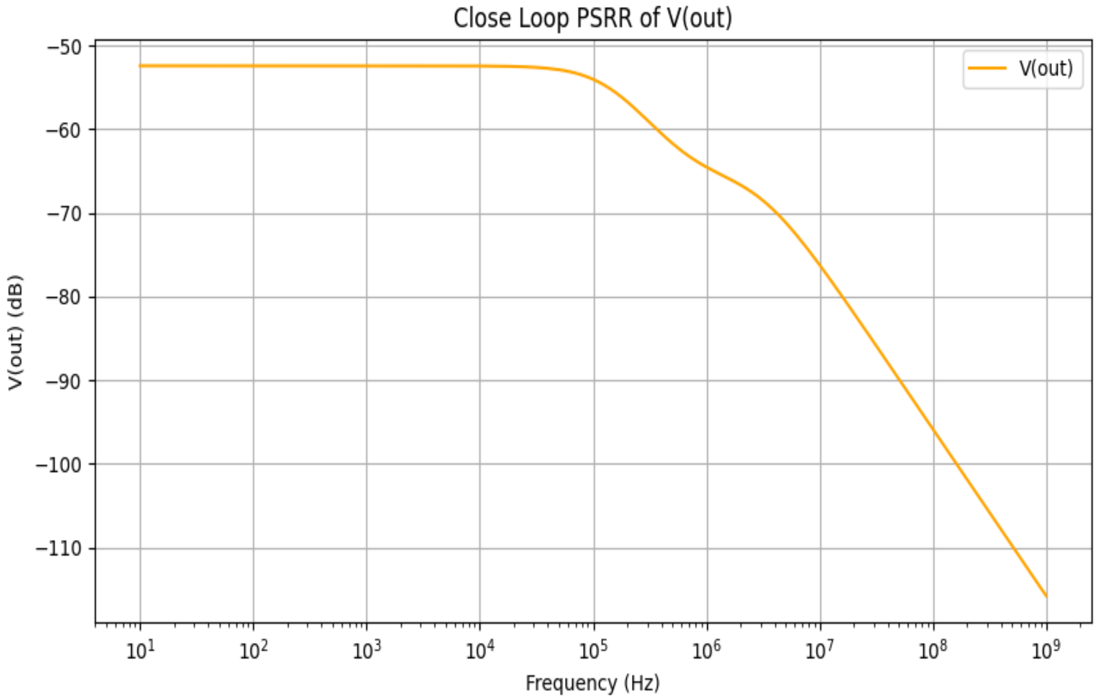


Figure 58: Close loop psrr of LDO

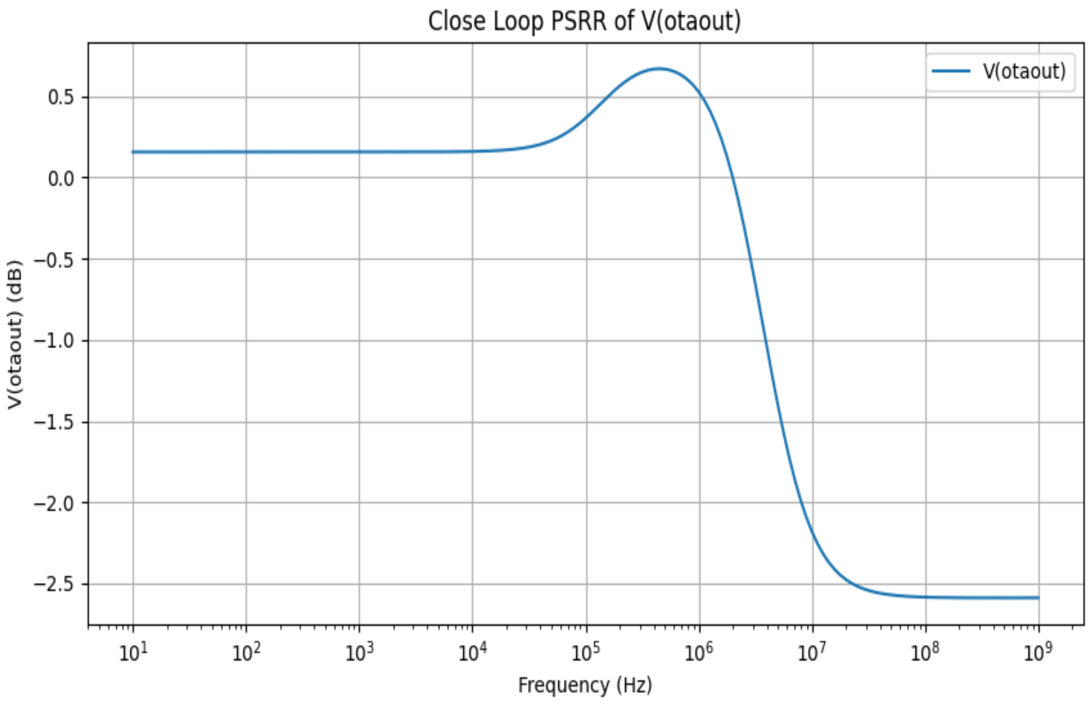


Figure 59: Close Loop PSRR of OTA

Transient Analysis

Schematic

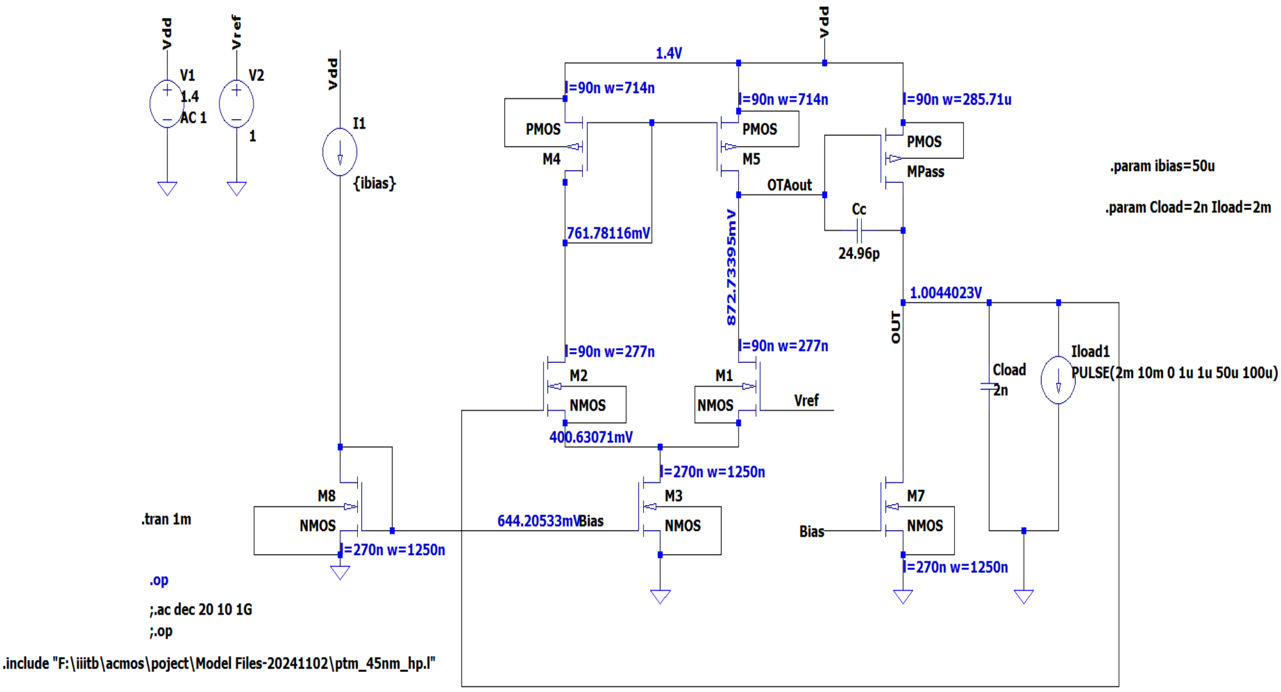


Figure 60: Schematic

Iload Vs Time

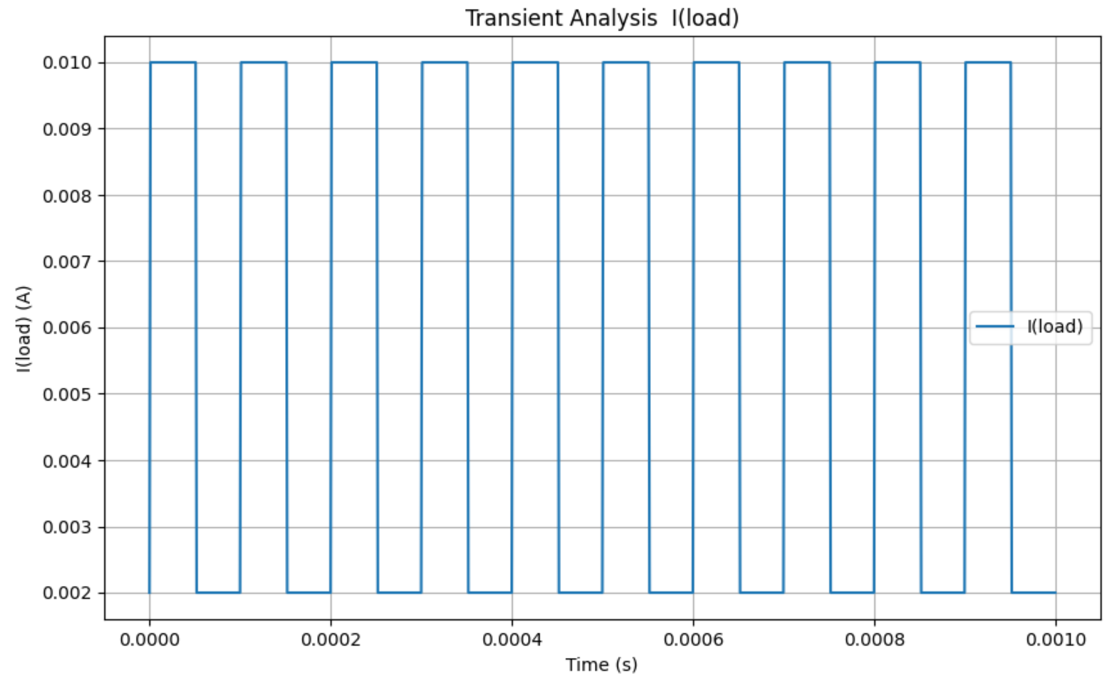


Figure 61: Iload Vs Time

Vout Vs Time

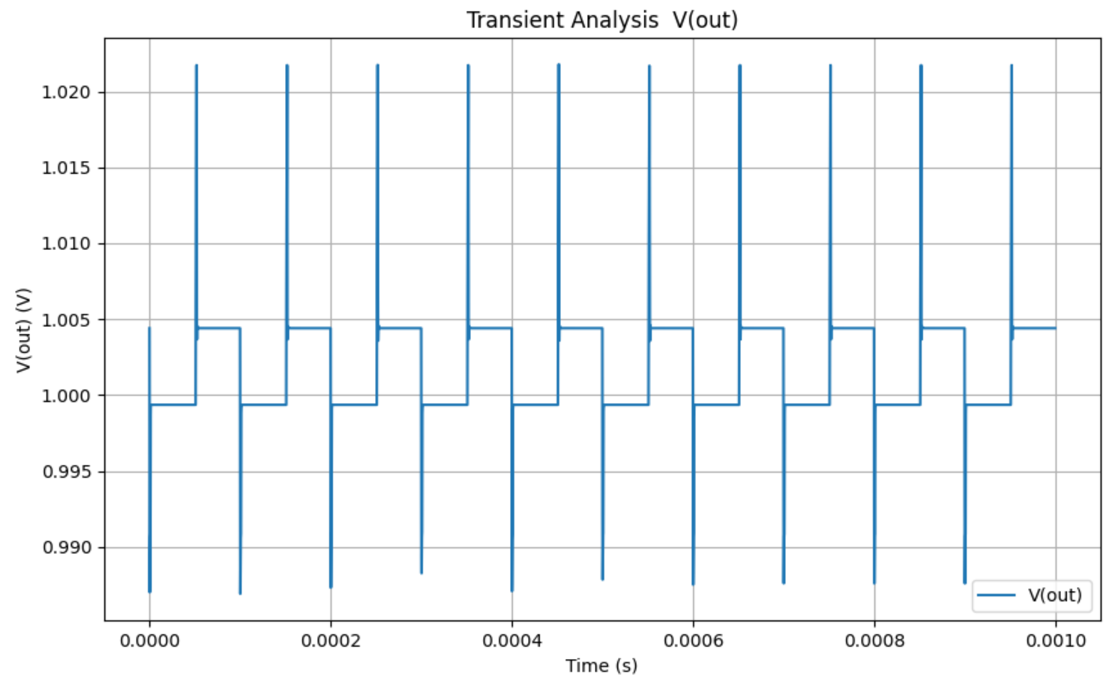


Figure 62: Vout Vs Time

Simulation vs. Hand Calculations

For Passfet HEAVY LOAD

Hand Calculation

- $r_o = 500\,\Omega$
- $g_m = 0.1\,\mathbf{A/V}$
- W_{p1} **(first pole location) = 9.94k**
- $g_m r_o = 50$
- $C_{gg} = 0.569p$
- $C_l = 2n$
- $C_c = 24.96p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 393\,\Omega$
- $g_m = 0.102\,\mathbf{A/V}$
- W_{p1} **(first pole location) = 10.04k**
- $g_m r_o = 40.086$

Table 15: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	500.00	390	22.0%
g_m (A/V)	0.1	0.102	1.9%
$g_m * r_o$	50	40.15	19.7%
W_{p1} (Hz)	9.94k	10.04k	1.01%
W_{p2} (Hz)	50M	51M	1.9%
W_{ugb} (Hz)	9.94M	10.04M	1.01%
r_{odiff} (ohm)	80k	98.619k	57.8%
g_{mdiff} (A/V)	250u	256u	2.4%

max width=

Name	mpass	m5	m4	m3	m7	m2	m1	m8
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-1.01E-02	-2.46E-05	-2.46E-05	4.94E-05	5.08E-05	2.46E-05	2.47E-05	5.00E-05
Vgs	-6.43E-01	-6.37E-01	-6.37E-01	6.44E-01	6.44E-01	6.02E-01	6.03E-01	6.44E-01
Vds	-3.87E-01	-6.43E-01	-6.37E-01	3.97E-01	1.01E+00	3.66E-01	3.60E-01	6.44E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.84E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.66E-01	4.69E-01
Vdsat	-1.72E-01	-1.70E-01	-1.70E-01	1.81E-01	1.82E-01	1.44E-01	1.44E-01	1.82E-01
Gm	1.02E-01	2.56E-04	2.55E-04	4.34E-04	4.46E-04	2.40E-04	2.41E-04	4.40E-04
Gds	2.54E-03	5.07E-06	5.07E-06	3.41E-06	2.03E-06	4.94E-06	5.03E-06	2.21E-06
Gmb	2.16E-02	5.40E-05	5.39E-05	1.04E-04	1.07E-04	5.55E-05	5.56E-05	1.05E-04
Cbd	1.28E-13	3.03E-16	3.03E-16	5.60E-16	4.96E-16	1.25E-16	1.25E-16	5.30E-16
Cbs	2.29E-13	5.71E-16	5.71E-16	1.00E-15	1.00E-15	2.22E-16	2.22E-16	1.00E-15
ro	3.94E+02	1.97E+05	1.97E+05	2.93E+05	4.93E+05	2.02E+05	1.99E+05	4.52E+05
gm*ro	4.02E+01	5.05E+01	5.03E+01	1.27E+02	2.20E+02	4.86E+01	4.79E+01	1.99E+02

Table 16: Transistor Parameter Table

For Passfet LIGHT LOAD

Hand Calculation

- $r_o = 2500\,\Omega$
- $g_m = 0.02\,\mathbf{A/V}$
- W_{p1} **(first pole location) = 10k**
- $g_m r_o = 50$
- $C_{gg} = 0.1136p$
- $C_l = 2n$
- $C_c = 24.96p$

Simulation Results from SPICE Error Log:

- $r_o = 1/g_{ds} = 1503.7\,\Omega$
- $g_m = 0.0364\,\mathbf{A/V}$
- W_{p1} **(first pole location) = 7.01k**
- $g_m r_o = 54.7$

Table 17: Hand Calculation vs Simulation Results

Parameter	Hand Calculation	Simulation Result	% Difference
r_o (ohm)	2500.00	1503.7	39.0%
g_m (A/V)	0.02	0.0364	45%
$g_m * r_o$	50	54.7	8.5%
W_{p1} (Hz)	10k	7.70k	23%
W_{p2} (Hz)	10M	18.2M	45.05%
W_{ugb} (Hz)	10M	7.70M	23 %
r_{odiff} (ohm)	80k	104.24k	23.07%
g_{mdiff} (A/V)	250u	253u	1.185%

max width=

Name	mpass	m5	m4	m3	m7	m2	m1	m8
Model	pmos	pmos	pmos	nmos	nmos	nmos	nmos	nmos
Id	-2.05E-03	-2.44E-05	-2.50E-05	4.94E-05	5.08E-05	2.50E-05	2.44E-05	5.00E-05
Vgs	-5.28E-01	-6.38E-01	-6.38E-01	6.44E-01	6.44E-01	6.04E-01	5.99E-01	6.44E-01
Vds	-3.82E-01	-5.28E-01	-6.38E-01	4.01E-01	1.02E+00	3.61E-01	4.72E-01	6.44E-01
Vbs	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00	0.00E+00
Vth	-4.87E-01	-4.86E-01	-4.84E-01	4.69E-01	4.69E-01	4.66E-01	4.65E-01	4.69E-01
Vdsat	-9.28E-02	-1.70E-01	-1.71E-01	1.81E-01	1.82E-01	1.45E-01	1.43E-01	1.82E-01
Gm	3.64E-02	2.53E-04	2.57E-04	4.34E-04	4.46E-04	2.42E-04	2.41E-04	4.40E-04
Gds	6.65E-04	5.30E-06	5.12E-06	3.36E-06	2.03E-06	5.06E-06	4.27E-06	2.21E-06
Gmb	7.50E-03	5.34E-05	5.43E-05	1.04E-04	1.07E-04	5.58E-05	5.56E-05	1.05E-04
Cbd	1.28E-13	3.10E-16	3.03E-16	5.59E-16	4.96E-16	1.25E-16	1.22E-16	5.30E-16
Cbs	2.29E-13	5.71E-16	5.71E-16	1.00E-15	1.00E-15	2.22E-16	2.22E-16	1.00E-15
ro	1.50E+03	1.89E+05	1.95E+05	2.98E+05	4.93E+05	1.98E+05	2.34E+05	4.52E+05
gm*ro	5.47E+01	4.77E+01	5.02E+01	1.29E+02	2.20E+02	4.78E+01	5.64E+01	1.99E+02

Table 18: Transistor Parameter Table

Stability Analysis

For Heavy load we get the following curve:

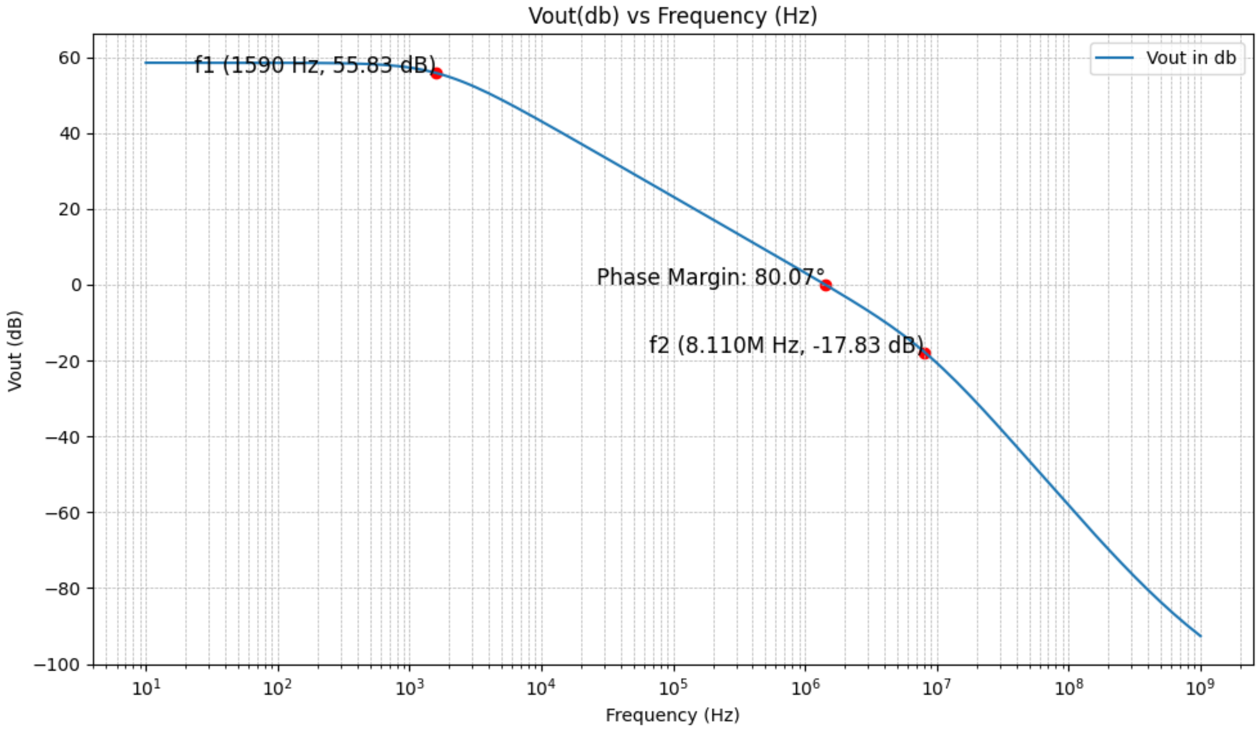


Figure 63: Pole representation

For Light load we get the following curve

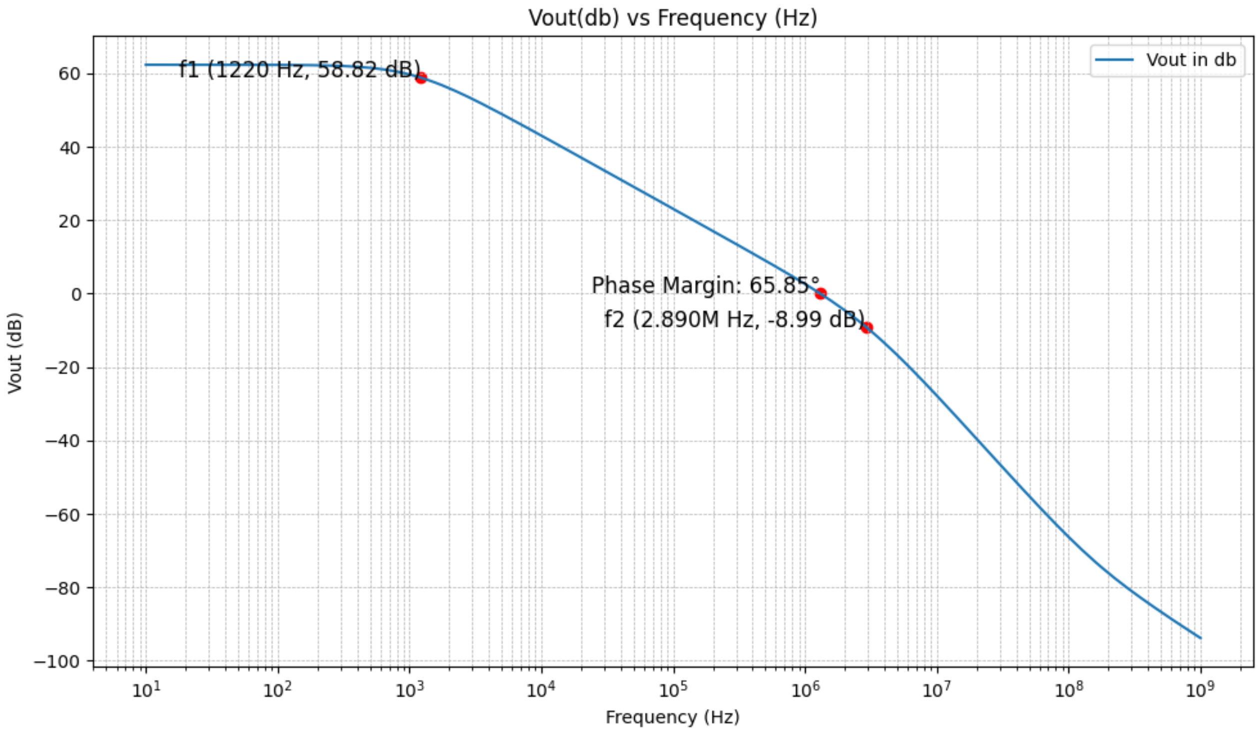


Figure 64: Pole representation

From the above analysis we can see that the unity gain bandwidth is closer to the second pole for the light load case than the heavy load case. From the phase margin also we we observe a better phase margin of 80.07 degrees for the heavy load case. From this analysis, we can say that we get a more stable system when we apply heavy load.