装 订 线

学号

姓名

专业班级

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西安邮电大学课程考试试题（B 卷）

（2022——2023 学年第一学期）

课程名称：《计算机组成与设计》
考试专业、年级：电子 20 级
考核方式：闭卷　　可使用计算器（否）

题号	一	二	三	四	五	六	七	八	九	总分
得分										
评卷人										

得分：_____　一、简答题（共 15 分）

得分：_____ 1. What are the three hazards of pipelined processors? How many data hazard(s) in the codes below (number only)? Please give the solutions respectively. **(10 points)**

```
ld x2, 20(x1)
and x4, x2, x5
or x8, x2, x6
add x9, x4, x2
sub x1, x6, x9
```

得分：_____ 2. Please briefly introduce *parallel processors*. **(5 points)**

得分：_____　二、选择题（每小题 4 分，共 20 分）

得分：_____ 1. The mapping of the main memory to Cache does not need to replace the strategy is（　　）.

A. Direct-mapped

B. Full associative

C. Set associative

D. The above three mapping methods

得分：_____ 2. Floating point number $(-8.25)_D$ is represented by IEEE754 single precision floating point format as （　　）.

A. $(C104\ 0000)_H$　　B. $(C242\ 0000)_H$　　C. $(C184\ 0000)_H$　　D. $(C1C2\ 0000)_H$

得分：_____ 3. Compared with the SRAM, the advantage of DRAM is （　　）.

A. The storage speed of dynamic RAM is fast.

B. Dynamic RAM is not easy to lose data.

C. In terms of technology, the storage density of static RAM is high.

D. Control is simpler than static RAM.

得分：_____ 4. The hierarchical structure of the computer system is （　） from the inside out.

A. Hardware system, system software, application software

B. System software, hardware system, application software

C. System software, application software, hardware system

D. Application software, hardware system, system software

得分：_____ 5. The largest number of the following number is （　　）.

A. $(243)_D$　　B. $(52)_O$　　C. $(10010101)_B$　　D. $(189)_H$

说明：1、除填空题、图解及特殊要求外，一般不留答题空间。 2、装订试卷、考生答卷时不得拆开或在框外留有任何标记，否则按零分计

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得分：_____ 三、计算题（共 35 分）

得分：_____ 1. In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies: （**15 points**）

IF	ID	EX	MEM	WB
250 ps	350 ps	150 ps	300 ps	200 ps

Also, assume that instructions executed by the processor are broken down as follows:

ALU/Logic	Jump/Branch	Load	Store
45%	20%	20%	15%

(1) What is the clock cycle time in a pipelined and non-pipelined processor?

(2) What is the total latency of an ***ld*** instruction in a pipelined and non-pipelined processor?

(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

(4) Assuming there are no stalls or hazards, what is the utilization of the data memory?

(5) Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

得分：_____ 2. Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 64-bit memory address references, given as **byte addresses.** （**20 points**）

0x00 0x04 0x10 0x84 0xE8 0xA0 0x400 0x1e 0x8c 0xc1c

(1) For each of these references, identify the binary byte address, the tag, the index and the offset given a direct-mapped cache with 32 blocks. The block size is 32B. Also list whether each reference is a hit or a miss, assuming the cache is initially empty. （**15 points**）

(2) Calculate the total number of bits required to implement this cache with write through. （**5 points**）

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得分：_____ 四、设计题（共 30 分）

得分：_____ 1. Please draw a single -cycle CPU datapath that can achieve the following seven instructions ***add***, ***sub***, ***and***, ***or***, ***ld***, ***sd***, ***beq***, and gives the value of control signals when performing ***sd*** instructions. **（24 points）**

得分：_____ 2. What additional logic blocks, if any, are needed to add ***bne*** instruction to the above datapath? Add any necessary logic blocks to the datapth and explain their purpose. **（6 points）**

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