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姓名

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# 西安邮电大学课程考试试题（A 卷）

## （2022——2023 学年第一学期）

**课程名称：《计算机组成与设计》**
**考试专业、年级：电子 20 级**
**考核方式：闭卷　　可使用计算器（否）**

| 题号 | 一 | 二 | 三 | 四 | 五 | 六 | 七 | 八 | 九 | 总分 |
|---|---|---|---|---|---|---|---|---|---|---|
| 得分 | | | | | | | | | | |
| 评卷人 | | | | | | | | | | |

**得分：_____　一、简答题（共 15 分）**

**得分：_____** 1. Please briefly introduce *parallel processors*. **(5 points)**

**得分：_____** 2. What are the three hazards of pipelined processors? How many data hazard(s) in the codes below (number only)? Please give the solutions respectively. **(10 points)**

```
ld x2, 20(x1)
and x4, x2, x5
or x8, x2, x6
add x9, x4, x2
sub x1, x6, x9
```

**得分：_____ 二、选择题（每小题 4 分，共 20 分）**

**得分：_____** 1. The smallest number of the following number is （　　）.

A. $(101001)_B$　　B. $(52)_O$　　C. $(29)_D$　　D. $(233)_H$

**得分：_____** 2. Floating point number $(-8.25)_D$ is represented by IEEE754 single precision floating point format as （　　）.

A. $(C104\ 0000)_H$　　B. $(C242\ 0000)_H$　　C. $(C184\ 0000)_H$　　D. $(C1C2\ 0000)_H$

**得分：_____** 3. The purpose of adding Cache between the main memory and the CPU is（　　）.

A. Increase memory capacity

B. Improve the reliability of memory

C. Solve the problem of speed matching between CPU and memory

D. Increase memory capacity and speed up the access speed

**得分：_____** 4. Among the following external storage, the sequential access memory is（　　）.

A. USB flash disk

B. hard disk

C. Tape

D. CD

**得分：_____** 5. The only language that computer hardware can execute is only （　　）.

A. High -level language

B. Machine language

C. Assembly language

D. Machine language and assembly language

说明：1、除填空题、图解及特殊要求外，一般不留答题空间。 2、装订试卷、考生答卷时不得拆开或在框外留有任何标记，否则按零分计

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得分：_____ 三、计算题（共 35 分）

得分：_____ 1. In this exercise, we examine how pipelining affects the clock cycle time of the processor. Problems in this exercise assume that individual stages of the datapath have the following latencies: （**15 points**）

| IF | ID | EX | MEM | WB |
|---|---|---|---|---|
| 250 ps | 350 ps | 150 ps | 300 ps | 200 ps |

Also, assume that instructions executed by the processor are broken down as follows:

| ALU/Logic | Jump/Branch | Load | Store |
|---|---|---|---|
| 45% | 20% | 20% | 15% |

(1) What is the clock cycle time in a pipelined and non-pipelined processor?

(2) What is the total latency of an ***ld*** instruction in a pipelined and non-pipelined processor?

(3) If we can split one stage of the pipelined datapath into two new stages, each with half the latency of the original stage, which stage would you split and what is the new clock cycle time of the processor?

(4) Assuming there are no stalls or hazards, what is the utilization of the data memory?

(5) Assuming there are no stalls or hazards, what is the utilization of the write-register port of the "Registers" unit?

得分：_____ 2. Caches are important to providing a high-performance memory hierarchy to processors. Below is a list of 64-bit memory address references, given as word addresses. （**20 points**）

**0x03, 0xb4, 0x2b, 0x02, 0xbf, 0x58, 0xbe, 0x0e, 0xb5, 0x2c, 0xba, 0xfd**

(1) For each of these references, identify the binary word address, the tag, and the index given a direct-mapped cache with 16 one-word blocks. Also list whether each reference is a hit or a miss, assuming the cache is initially empty.

(2) For each of these references, identify the binary word address, the tag, the index, and the offset given a direct-mapped cache with two-word blocks and a total size of eight blocks. Also list if each reference is a hit or a miss, assuming the cache is initially empty.

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**得分：_____ 四、设计题（共 30 分）**

**得分：_____** 1. Please draw a single -cycle CPU datapath that can achieve the following seven instructions ***add***, ***sub***, ***and***, ***or***, ***ld***, ***sd***, ***beq***, and gives the value of control signals when performing ***ld*** instructions. **（24 points）**

**得分：_____** 2. What additional logic blocks, if any, are needed to add ***bne*** instruction to the above datapath? Add any necessary logic blocks to the datapth and explain their purpose. **（6 points）**

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