装 订 线

学号

姓名

专业班级

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西安邮电大学课程考试试题（C 卷）

（2022——2023 学年第一学期）

课程名称：《计算机组成与设计》
考试专业、年级：电子 20 级
考核方式：闭卷　　可使用计算器（否）

题号	一	二	三	四	五	六	七	八	九	总分
得分										
评卷人										

得分：_____　一、简答题（共 15 分）

得分：_____ 1. Please briefly introduce *parallel processors*. **(5 points)**

得分：_____ 2. What is the minimum number of cycles needed to completely execute n instructions on a CPU with a k stage pipeline? Justify your formula. **(5 points)**

得分：_____ 3. Assuming that your friends do not understand the computer well, please explain to your friends how the computer works. **(5 points)**

得分：_____ 二、选择题（每小题 4 分，共 20 分）

得分：_____ 1. The smallest number of the following number is （　）

A. $(101001)_B$　　B. $(52)_O$　　C. $(29)_D$　　D. $(233)_H$

得分：_____ 2. Floating point number $(-0.5)_D$ is represented by IEEE754 single precision floating point format as （　）

A. $(CE00\ 0000)_H$　　B. $(CF00\ 0000)_H$　　C. $(CF10\ 0000)_H$　　D. $(CE10\ 0000)_H$

得分：_____ 3. In the address mapping of the cache, if any piece in the main memory can be mapped to any fast position in cache, this method is called （　）.

A. Full associative　　B. Direct-mapped

C. Set associative　　D. Mixed mapping

得分：_____ 4. The advantages of hardware in functional implementation are（　）.

A. Fast speed　　B. Low cost

C. Strong flexibility　　D. Easy to achieve

得分：_____ 5. The main purpose of different addressing methods in the instruction system is （　　）.

A. Increase the capacity of memory

B. Short in the length of the instruction and expand the address of the address

C. Improve the speed of access memory

D. Simplify instruction decoding circuit

说明：1、除填空题、图解及特殊要求外，一般不留答题空间。 2、装订试卷、考生答卷时不得拆开或在框外留有任何标记，否则按零分计

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得分：_____ 三、计算题（共 35 分）

得分：_____ 1. Problems in this exercise refer to the following sequence of instructions, and assume that it is executed on a five-stage pipelined datapath. **(15 points)**

```
add x15, x12, x11
ld x13, 4(x15)
ld x12, 0(x2)
or x13, x15, x13
sd x13, 0(x15)
```

(1) If there is no forwarding or hazard detection, insert NOPs to ensure correct execution. **(5 points)**

(2) If there is forwarding, for the first seven cycles during the execution of this code, specify which signals are asserted in each cycle by hazard detection and forwarding units. **(10 points)**

得分：_____ 2. For a direct-mapped cache with four-word blocks. Below is a list of 64-bit memory address references, given as byte addresses. (Attention: 1 word = 64 bits) **(20 points)**

address	**0x02**	**0x06**	**0xe1c**	**0x416**	**0x28**	**0x34**	**0x64**	**0x148**	**0xf14**	**0x41c**	**0xc30**	**0x62**

(1) Calculate the total number of bits required to implement a 1KiB cache; **(5 points)**

(2) For each reference, list ①its tag, index, and offset; ②whether each reference is a hit or a miss, assuming the cache is initially empty; and③what is the hit ratio? **(15 points)**

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得分：_____ 四、设计题（共 30 分）

得分：_____ 1. Please draw a single -cycle CPU datapath that can achieve the following seven instructions ***add***, ***sub***, ***and***, ***or***, ***ld***, ***sd***, ***beq***, and gives the value of control signals when performing ***add*** instructions. **（24 points）**

得分：_____ 2. What additional logic blocks, if any, are needed to add ***bne*** instruction to the above datapath? Add any necessary logic blocks to the datapth and explain their purpose. **（6 points）**

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