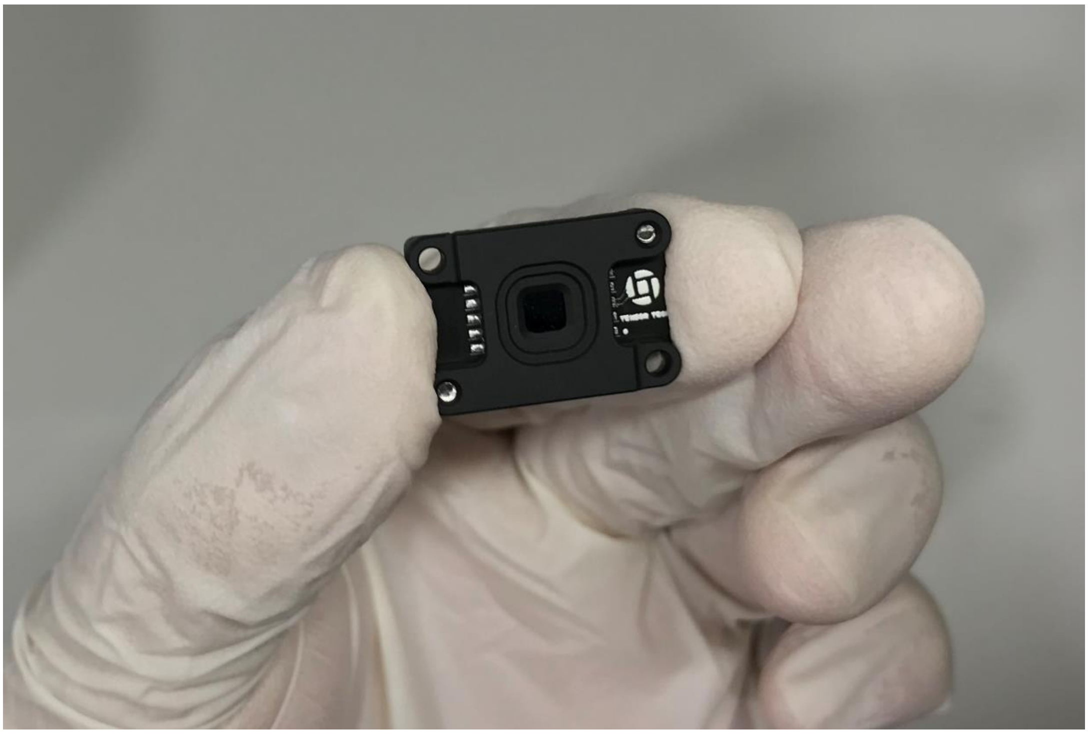
User Manual for

FSS100 – Nano Fine Sun Sensor



V2.2

2021.12.14

Tensor Tech CO., LTD.

P: +886 229319383 W: tensortech.com.tw E: info@tensortech.com.tw
A: 3F.-1, No. 211, Sec. 2, Anhe Rd., Da'an Dist., Taipei City 106056, Taiwan (R.O.C.)

Table of Contents

Abbreviation List

ESD	Electrostatic Discharge
PCBA	Printed Circuit Board Assembly
SMT	Surface Mount Technology for manufacturing of a PCBA
OBC	Onboard Computer on a satellite
ADCS	Satellite Attitude Determination and Control System
PC	Personal Computer
ICD	Interface Control Document
TID	Total Ionizing Dose radiation test
FM	Flight model. The product is used for integrating into the user's satellite that is planned to be launched into space. Therefore, disruptive environmental tests won't be performed by Tensor Tech before the shipment of the product
EM	Engineering Model. The product is used for conducting functional tests, destructive tests, or experiments in the user's laboratory.
DUT	Device Under Test. Herein refers to the product under functional or environmental tests.
NVM	Non-Volatile Memory
LSB	Least Significant Bit
RAM	Random Access Memory

Document Revisions

Date	Author	Revision	Descriptions
2020.12.11	Thomas Yen	V1.0	Establishing initial parameters and definitions
2021.08.30	Thomas Yen	V2.0	Updating critical specifications and drawings
2021.11.09	Sam Lee and Thomas Yen	V2.1	Add in the section of interface control document (ICD)
2021.12.14	Thomas Yen	V2.2	Update the mechanical drawing of the FSS100 and add in the section of mounting error control.

A. Unpacking and Handling

1. Control the electrostatic discharge (ESD) in the environment

FSS100 is an ESD-sensitive device. Please un-packaging and integrate it with proper equipment and procedures.

2. Control the contamination in the environment

FSS100 is assembled in a cleanroom environment certified with ISO 14644-1 ISO5 standard. This preparation is majorly set up to prevent dust from getting into FSS100. To conduct a proper integration of Tensor Tech's FSS100 into your CubeSat, we suggest having a cleanroom environment of ISO7 standard or at least having an air shower of ISO7 standard to wash out the dust on the lens before sending it to space.

3. Remove the Kapton Tape before launch

A Kapton tape covers the top of the lens before shipping. After the users finish their satellite integration and are ready for launch, please remove that Kapton tape to keep the FSS100 properly functioning. If users plan to conduct a functional test on the FSS100 under a solar simulator, remove the Kapton tape temporarily during the Test, then put it back after the Test.

4. Do not remove any electrical or mechanical components on the FSS100

The primary cause of the system errors on FSS100 is the imperfection of manufacturing the aperture and its mounting. Tensor Tech performs in-factory calibration on every shipped FSS100 to keep the sensor's error in the guaranteed range. This calibration includes biasing the center of the light spot on the photodiode and correcting the error tabulated via the error table. This error table will be input into the FSS100 before the shipment. To keep the calibration result valid, Tensor Tech glues up the aperture with space-grade epoxy. Therefore, do not remove any mechanical parts on the FSS100. Otherwise, the sun vector determination accuracy may vary.

Every surface-mount-technology (SMT) electrical component will be glued with space-grade epoxy before the shipment to prevent possible fall off during the launch or users' vibration test. However, if users find any electrical or mechanical components fall off via visual inspection during proper environmental testings that this user manual allows, please contact Tensor Tech's team to ship you a new one.

B. Storage

In Tensor Tech, we storge our standard FSS100 in a dry environment with relative humility that is 2% or lower. To store this FSS100, we recommend having a moisture-proof box with relative humility 20% or lower. Moreover, the recommended storing temperature is listed in Table C-1.

C. Product Specifications

Table C-1. Mechanical Specifications

1	Weight	2.5 grams
2	Size	22 mm * 15 mm * 5.16 mm (Length*Width*Height)
3	Maximum Flock of View (FOV)	+/- 60 deg
4	Recommended Operation FOV	+/- 45 deg
5	Pointing Knowledge	less than +/- 0.5 deg in recommended FOV (3-sigma) without albedo
6	Operating Temperature Range	Absolute Maximum: -40~85 deg C[1] Recommend: -20~50 deg C
7	Storing Temperature Range	Absolute Maximum: -40~85 deg C Recommend: 10~30 deg C
8	PCB Production Standard	Following IPC-6012C Class 3
9	PCB Assembly Standard	Following IPC-A-610 Class 3

Table C-2. Electrical Specifications

1	Current Consumption	sampling: 2.4mA not sampling: 1.4mA
2	Supplied Voltage Range	Absolute Maximum: 2.3~5.5V Recommend: 3.2V~3.4V
3	Interface	I2C and UART
4	Connectors	There are two Molex Pico- Ez Mate 0781710004 connectors, one for the UART and the other for the I2C communication. Customization on the connector is available; please get in touch with Tensor Tech's team.

[1] If the product is operate or storing in absolute maximum rages, its performane and reliability may degrade. The product may still function, but its out of Tensor Tech's warranty.

5	Pinout Definition	GND, VDD, SCL, and SDA for the I2C connector; GND, RX, TX, and VDD for the UART connector. Figure C-1 depicts such a pinout diagram. Please glue up the cable and connector before sending the satellite to space. Such a procedure prevents the cables from falling off. Only one of the connectors should be connected to the user's onboard computer (OBC) or Attitude Determination and Control System (ADCS) computer. Both provide the functionalities of supplying power, commanding, and outputting information from the product. To connect the product to the user's personal computer (PC) for calibration and functional tests, use the UART connector and a TTL to USB converter. (ship with the delivered product) Select the correct Com port on the user's PC with Tensor Tech's customer support software. Detailed instructions are provided in the interface control document (ICD).

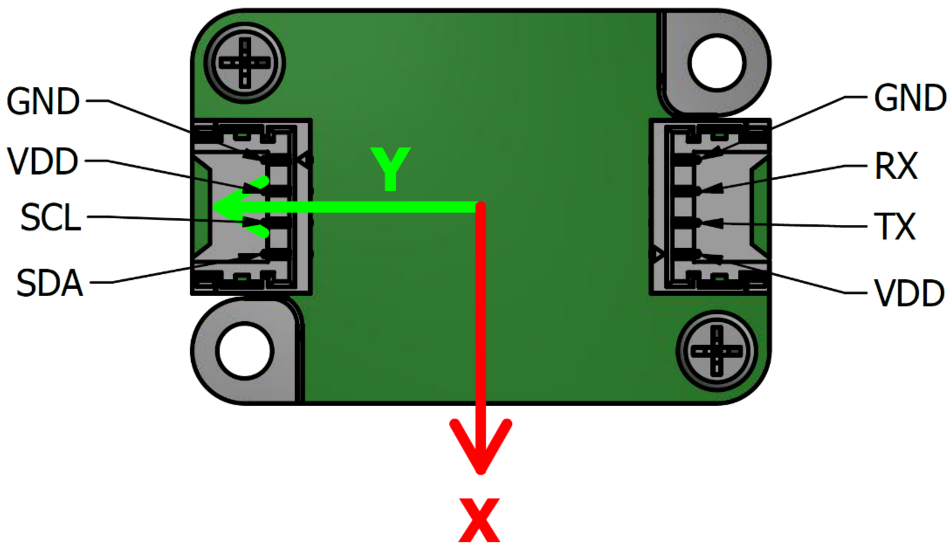


Figure C-1. Pinout Definition of the FSS100 (seen from the backside of the product)

D. Environmental Test Standards[2]

Tensor Tech's FSS100 thermal vacuum and vibration tests follow the ESA QB50 standard. For the total ionizing dose (TID) radiation test, we follow ESCC Basic Specification No. 22900- "TOTAL DOSE STEADY-STATE IRRADIATION TEST METHOD." For the single event effect radiation test, we follow ECSS Basic Specification No. 25100- "SINGLE EVENT EFFECTS TEST METHOD AND GUIDELINES." Our testing specifications are listed in Table D-1.

Table D-1. Environmental Test Standard for FSS100

1	Thermal Vacuum Baked-out Test	3 hours, 50 deg C, 10^{-5} mBar
2	Thermal Vacuum Cycling Test	4 cycles, the temperature varies from -20 to 50 degrees Celsius, 60 hours of testing time in total. The degree of vacuum is kept under 10^{-5} mbar for the whole process.
3	Random Vibration Test	20~2000Hz, 14 Grms for 120 seconds. Perform sine sweep vibration tests from 5 to 500Hz before and after the random vibration test. The acceptance requires a pass on QB50-SYS-2.6.1.
4	Total Ionizing Test[3]	10 krad using Co-60 radiation source
5	Single Event Effect Test	10^8 particles per cm^2 per second, with a 230 MeV proton beam, Lasting for 1000 seconds.

A self-communication check, an embedded function built in the customer support software, is executed after each environmental Test. This self-communication check inspects the survival of FSS100, including the ability to communicate to the user's OBC and the proper functioning of the circuitry. However, the performance spec like sun vector determination accuracy cannot be verified by this function.

Since the environmental tests may influence the product's performance, Tensor Tech calibrates the product and conducts the functional Test after the environmental tests. The detailed specs are listed in section E.

[2] Executed on every delivered flight model (FM). Self-communication check will be made after each environmental tests.

[3] Radiation tests including total ionizing test and single event effect test are disruptive tests. Tensor Tech only excuted these two tests on several finished samples. Therefore, the shipped FM or Engineering Model (EM) will not be excuted with radiation tests unless required by the user.

E. Functional Test Standards[4]

The in-factory calibration carried out by Tensor Tech's team is set up in an ISO7 clean room. An AM0 grade solar simulator and a two-axis rotational table that has accuracies up to arc-minute level are used for the calibration. A power supply is used for checking if the current consumption of the Device Under Test (DUT) is out of our guaranteed level. Moreover, the sun vector determination acracy will be post-validated and recorded in a test report with measured current consumption and environmental testing results. This test report will be shipped with the product, and the user may trace it back to that specific product with a unique serial number. Tensor Tech's customer support software can access that serial number. It helps Tensor Tech's team and the users to identify the differences between every shipped product.

Suppose the current consumption of the DUT or the sun vector determination error of the DUT exceeds the guaranteed specs listed in this user manual, that DUT will be deemed as a defective part. The shipped EMs are required to pass the functional tests. For the shipped FMs, they have to pass both the environmental and functional tests. Here are the conditions that we conduct such functional tests.

1. **Testing Light source: ASTM AM0, Class AAA**
2. **Two angle errors will be measured in each testing condition, one in Phi and the other in Theta, defined in Figure E-1. Totally 108 testing conditions for completing the error table, exampled in Table E-1.**

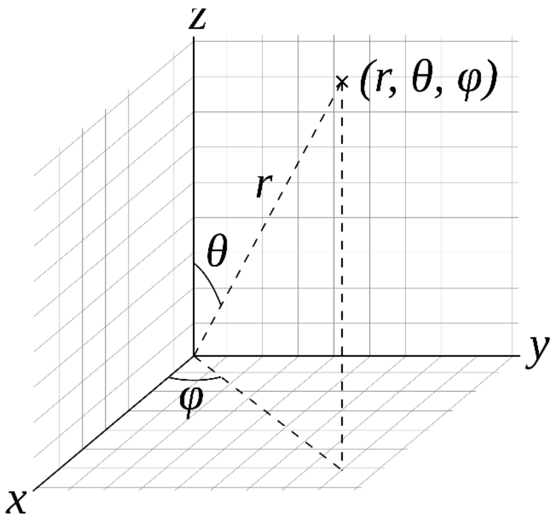


Figure E-1. Definition of the spherical coordinate that is being used for sun vector outputted and the construction of error table [2]

[4] Executed on every delivered EM and FM. For the FMs, functional tests will be executed after the environmental tests.

Table E-1. Example Error table that will be provided to the user and written into the shipped product. It contains the theta and phi angle error information of the DUT.

Phi\ Theta	Range	-60~ -50	-50~ -40	-40~ -30	-30~ -20	-20~ -10	-10~ 0	0~ 10	10~ 20	20~ 30	30~ 40	40~ 50	50~ 60
Range	Displayed value[5]	-55	-45	-35	-25	-15	-5	5	15	25	35	45	55
-90~ -70	-80	\	\	\	\	\	\	\	\	\	\	\	\
-70~ -50	-60	\	\	\	\	\	\	\	\	\	\	\	\
-50~ -30	-40	\	\	\	\	\	\	\	\	\	\	\	\
-30~ -10	-20	\	\	\	\	\	\	\	\	\	\	\	\
-10~ 10	0	\	\	\	\	\	\	\	\	\	\	\	\
10~ 30	20	\	\	\	\	\	\	\	\	\	\	\	\
30~ 50	40	\	\	\	\	\	\	\	\	\	\	\	\
50~ 70	60	\	\	\	\	\	\	\	\	\	\	\	\
70~ 90	80	\	\	\	\	\	\	\	\	\	\	\	\

F. Frame Definition and Sun Vector Calculations

The microcontroller (MCU) in FSS100 will automatically calculate the sun vector measured using the following algorithms. Firstly, we define the coordinate in figure F-1, calculation parameters in table F-1. The relative position of photodiode cells is shown in figure F-2. Secondly, the position of the light spot is calculated via equation F-1. Then, the Theta and Phi angle is calculated via equation F-2. [3]

[5] Customer support software has the function for users to conduct error table-cased calibration by themselves. The white-colored blanks show that the angle ranges that will use this error information for correction; the gray-colored blanks show that the displayed angle in the customer support software's screen, as well as the angle that should be used for obtaining that error information; the green-colored blanks show the two error angles, one for Phi, and the other for Theta

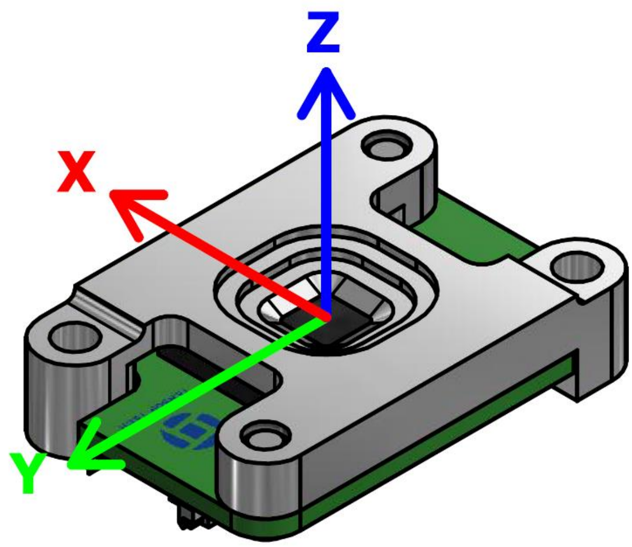


Figure F-1. Fine Sun Sensor frame definition

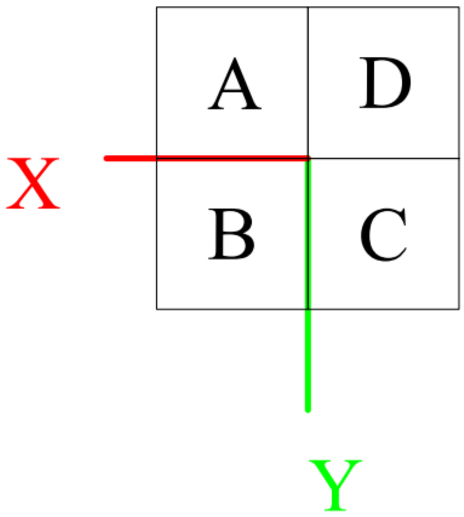


Figure F-2. quad-segmented photodiode cell position definition

Table F-1. Definition of the parameters

v_a	Voltage measurement of cell A defined in Figure F-2	p_x	Center of the light spot in X-axis
v_b	Voltage measurement of cell B defined in Figure F-2	p_y	Center of the light spot in Y-axis
v_c	Voltage measurement of cell C defined in Figure F-2	e_{theta}	Measured error for Theta angle in Table E-1. (According to the tilting range)
v_d	Voltage measurement of cell D	e_{phi}	Measured error for Phi angle in

	defined in Figure F-2		Table E-1. (According to the tilting range)
e_x	Error for biasing the light spot position in the X and Y-axis. Such error is caused by the imperfection of the mounting of the aperture. Tensor Tech's team measures these errors and input them into FSS100 before shipping. Do not adjust these two values using customer support software unless consulting with Tensor Tech's team.		
e_y			

Finally, use equation F-3 to change the output theta and phi angle to be compatible with the defined fine sun sensor coordinate. The coefficient k_1 to k_4 are constant parameters relating to the FSS100 aperture structure.

$$\begin{pmatrix} p_x \\ p_y \end{pmatrix} = \begin{pmatrix} k_1 \cdot \dfrac{v_a + v_b - v_c - v_d}{v_a + v_b + v_c + v_d} - e_x \\ k_2 \cdot \dfrac{v_b + v_c - v_a - v_d}{v_a + v_b + v_c + v_d} - e_y \end{pmatrix} \quad \text{Equation F-1}$$

$$\begin{pmatrix} \theta \\ \varphi \end{pmatrix} = \begin{pmatrix} k_3 \cdot \arcsin\left(1.41 \cdot \sin\left(\dfrac{\sqrt{{p_x}^2 + {p_y}^2}}{\sqrt{{p_x}^2 + {p_y}^2 + 0.46^2}}\right)\right) + e_{theta} \\ k_4 \cdot \arcsin\left(\sin\left(\dfrac{{p_y}^2}{\sqrt{{p_x}^2 + {p_y}^2}}\right)\right) + e_{phi} \end{pmatrix} \quad \text{Equation F-2}$$

$$\text{if } p_x \geq 0, \theta = -\theta; \text{else: } \varphi = -\varphi \quad \text{Equation F-3}$$

G. Interface Control Document

1. FSS100 Operation Overview

1) When powered up, FSS100 initializes all its registers with default values. CONF and ADDR default values are loaded from the Non-Volatile Memory (NVM). This configuration means the default values and the I^2C address can be modified.
2) FSS100 enters Idle mode after initialization. At Idle mode, FSS100 responses to UART and I^2C read/write requests. If the FSS100 is set into the continuous mode, the timer will wake up FSS100 then set the SAMP bit at a fixed rate.
3) After being woke up, FSS100 will check if CONF or ADDR is modified. If so, FSS100 updates its setting. According to SAMP bit in CONF, FSS100 performs sampling and filtering. The results are stored in the registers.

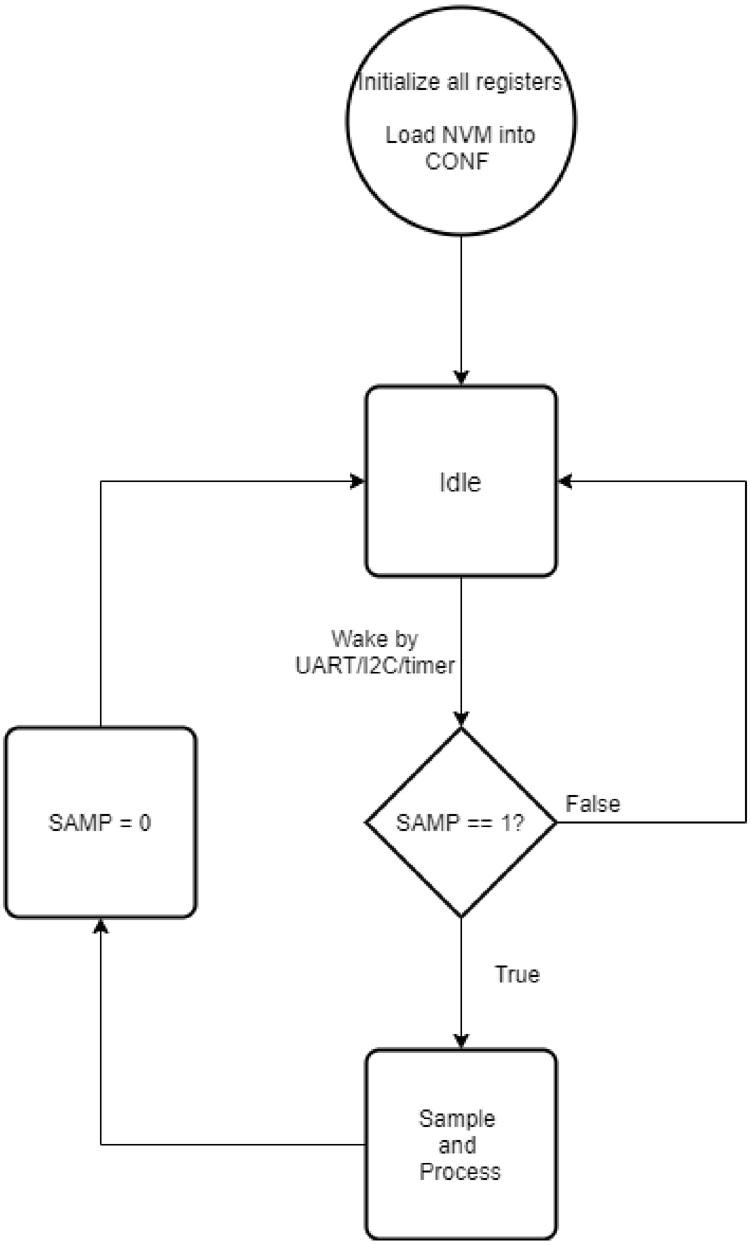


Figure G-1. Primary Function Flow Chart

2. I²C Interface

FSS100 serves as a slave device on the I²C bus [5]. The data sent to FSS100 are stored in a buffer (the "buf" blank in Figure G-2) and handled according to Figure G-2. Three events trigger the I²C interface, "Address Event," "Read Event," and "Write Event."

- Address Event: If the first byte after the start condition of the I²C bus matches the ADDR, the address event will be triggered. The Least

Significant Bit (LSB) of the first byte is the RW bit.

- Write Event: FSS100 transmits messages to the master. This event happens when RW=1 and the master starts sending the clock.
- Read Event: Master transmits messages to the FSS100. This event happens when RW=0 and the master starts sending the clock.

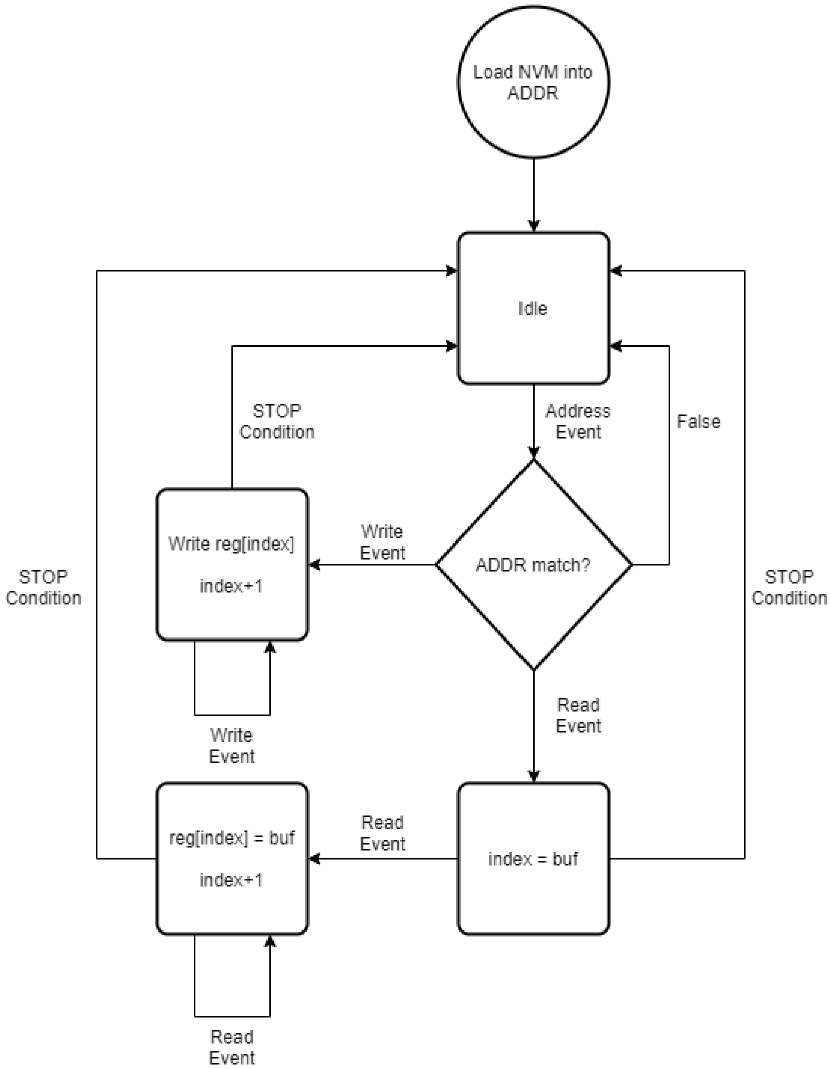


Figure G-2. I^2C Interface Operation

3. I²C Interface Operation Details

1) When powered up, FSS100 loads the I^2C address from NVM into ADDR. Then FSS100 enters the Idle mode, waiting for the address event.
2) If a “Write Event” happens, FSS100 will send the byte stored in the indexed register. The index increments automatically. The index resets to 0 when it reaches the end of the register map.
3) If a “Read Event” happens right after the Address Event, FSS100 will assign

the byte to the index. The following "Read Event" stores the byte into the register pointed by the index. The index increments by 1 at the end of the "Read Event." It will be reset to 0 when it reaches the end of the register map.

4) STOP condition on I^2C bus resets FSS100 back to Idle.

4. UART Interface

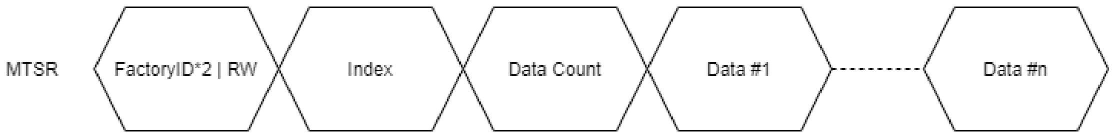


Figure G-3. Writing Register Message

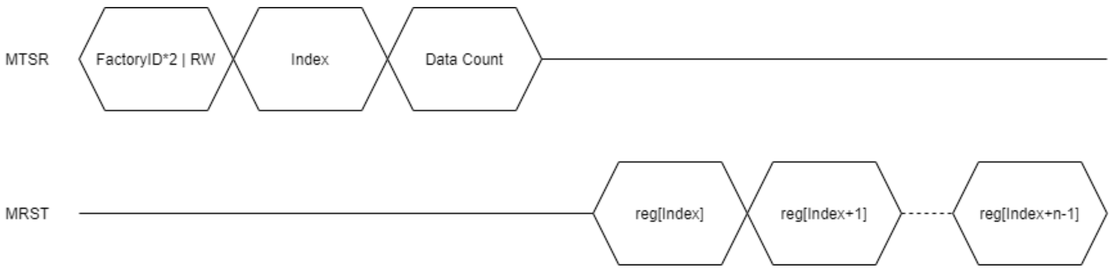


Figure G-4. Reading Register Message

- FSS100 can be accessed via UART-8N1, using a 115200 baud rate. Every block in Figure G-3 and Figure G-4 represents a byte.
- The FactoryID is 0x57. To start a message, the first byte, HEAD, must be FactoryID left shifting 1 bit. The LSB of HEAD represents read(1) message or write(0) message.
- The second byte is an index, indicating which register to start from.
- Data Count tells FSS100 how much data byte to read/write.
- A "write" message should follow with n Data byte equal to Data Count.
- A read message ends with a Data Count byte. Then FSS100 replies with n Data bytes.

5. Register Map

The register map is the interface for FSS100 to exchange data and set the FSS100. The data is stored in the Little-Endian pattern.

Table G-1. Register Map

Index	Alias	Type	Default Value
0	THETA	int 16	0x0000

2	PHI	int 16	0x0000
4	TEMP	int 16	0x0000
6	CNT	uint 16	0x0000
8	CONL	uint 8	0x00
9	CONH	uint 8	0x57
10	VER	uint 16	—
12	SER	uint 16	—

THETA

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
THETA_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
THETA_H							
R							

THETA_L: Lower byte of THETA

THETA_H: Higher byte of THETA

$$\theta = \frac{1}{3}\pi * \mathrm{THETA}/32767.0 \qquad \text{Equation G-1}$$

PHI

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
PHI_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PHI_H							
R							

PHI_L: Lower byte of PHI

PHI_H: Higher byte of PHI

$$\phi = \frac{1}{2}\pi * \mathrm{PHI}/32767.0 \qquad \text{Equation G-2}$$

TEMP

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
TEMP_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TEMP_H							
R							

TEMP_L: Lower byte of TEMP

TEMP_H: Higher byte of TEMP

$$T = TEMP/128.0 \qquad \text{Equation G-3}$$

CNT

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
CNT_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CNT_H							
R							

CNT_L: Lower byte of CNT

CNT_H: Higher byte of CNT

CNT records how many samples are being made after powered up. It will automatically be reset when it is overflowed.

CONL

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAMP	MODE	CMT	SR		LOCK	—	—
RW	RW	RW	RW		RW	—	—

SAMP: Sample Request bit

1 = Request FSS100 to sample the sun vector and temperature. If the process is not finished yet, read as 1.

0 = Sample done. Results are stored in THETA, PHI, and TEMP.

MODE: FSS100 Operation Mode

1 = Continuous mode, FSS100 update the sample result at the rate describe in SR

0 = One-Shot mode, FSS100 sample once when SAMP=1

CMT: Commit Setting

1 = FSS100 stores CONL and CONH into NVM. Read as 1 when the commit has not been handled.

0 = Setting remain in Random Access Memory (RAM)

SR: Sample Rate

0b11 = 32Hz

0b10 = 16Hz

0b01 = 8Hz

0b00 = 4Hz

LOCK: Extend Register Lock

1 = Unlock the extend registers. Extend register contain factory calibration data, please consult Tensor Tech before modify them.

0 = Extend registers locked.

CONH

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
—	ADDR						

ADDR: 7-bit I²C address. After writing ADDR, CMT must be set to 1. Then FSS100 will update its I²C address[6].

VER

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
VER_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
VER_H							
R							

VER: Firmware Version of FSS100.

SER

[6] User can change FSS100's I²C default address via UART or even I²C interface. This feature provides the capability to attach much more I²C devices on the bus. However, modifying the I²C address is strongly not recommend on orbit.

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
SER_L							
R							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SER_H							
R							

SER: Unique serial number[7] for the FSS100.

H. Mounting Error control

The pointing performance of the FSS100 is solely designated in Table C-1. However, the user often uses it with their ADCS system. Therefore, another system error exists between the ADCS reference frame and the FSS reference frame. The mounting error frequently causes it. If the material of the mounting plane of the FSS100 is different from the material used on the FSS100 (aluminum alloy 6061-T6), the thermal variation on the orbit will furtherly cause a time-varying system error between the ADCS reference frame and the FSS100 reference frame.

For minimizing mounting errors in the X/Y axis of the FSS100, the parallelism of the contacting surface is manufactured under 0.01mm. Please make sure the surface of the mounting plane is well-processed as well. Furthermore, a reamer bolt will be preferred to control the Z-axis mounting error, as attachment 1 shows.

References and Attachments

[1] FSS100 Mechanical Drawing

[2] International Standard Organization (ISO). (2019, August). ISO 80000-2:2019 Quantities and units. https://www.iso.org/standard/64973.html

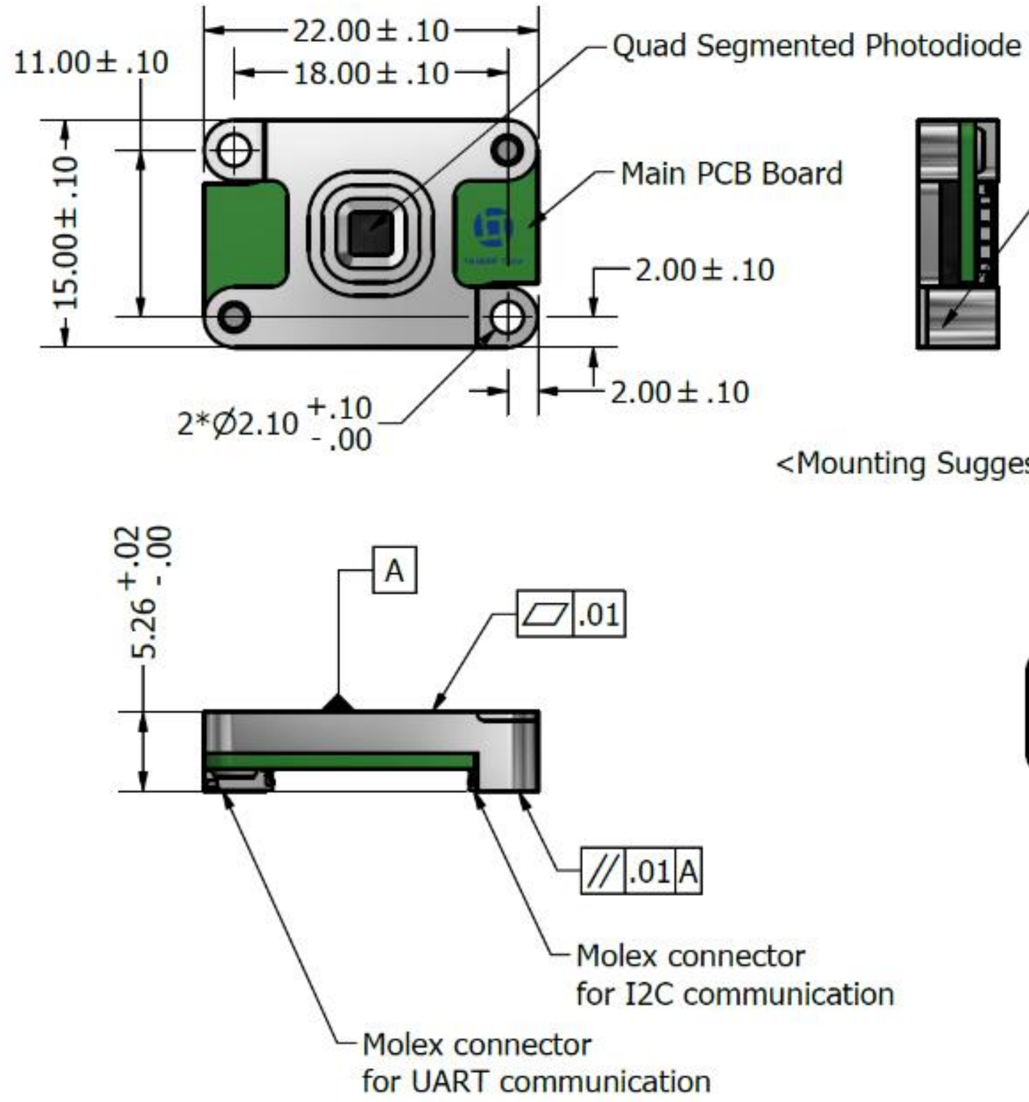
[3] E. Boslooper, N. Heiden, D. Naron, R. Schmits, J. Velde, and J. Wakeren. (2012). BepiColombo fine sun sensor. International Conference on Space Optics. https://www.spiedigitallibrary.org/conference-proceedings-of-spie/10564/105641P/BepiColombo-fine-sun-sensor/10.1117/12.2309172.full?SSO=1

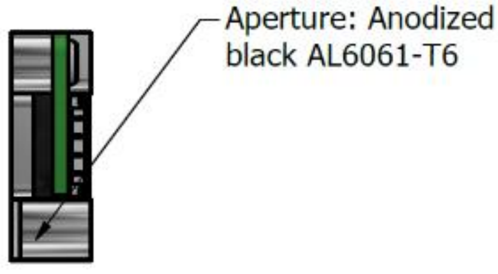
[4] TENSOR TECH. (2021, June 12). An introduction to fine sun sensors –. https://tensortech.com.tw/an-introduction-to-fine-sun-sensors/

[5] NXP. (2003, March 24). Application Note: AN10216-01 I^2C MANUAL. https://www.nxp.com/docs/en/application-note/AN10216.pdf

7 The serial number will not be repeated in the same batch

<FSS100 Mechanical Dimension>





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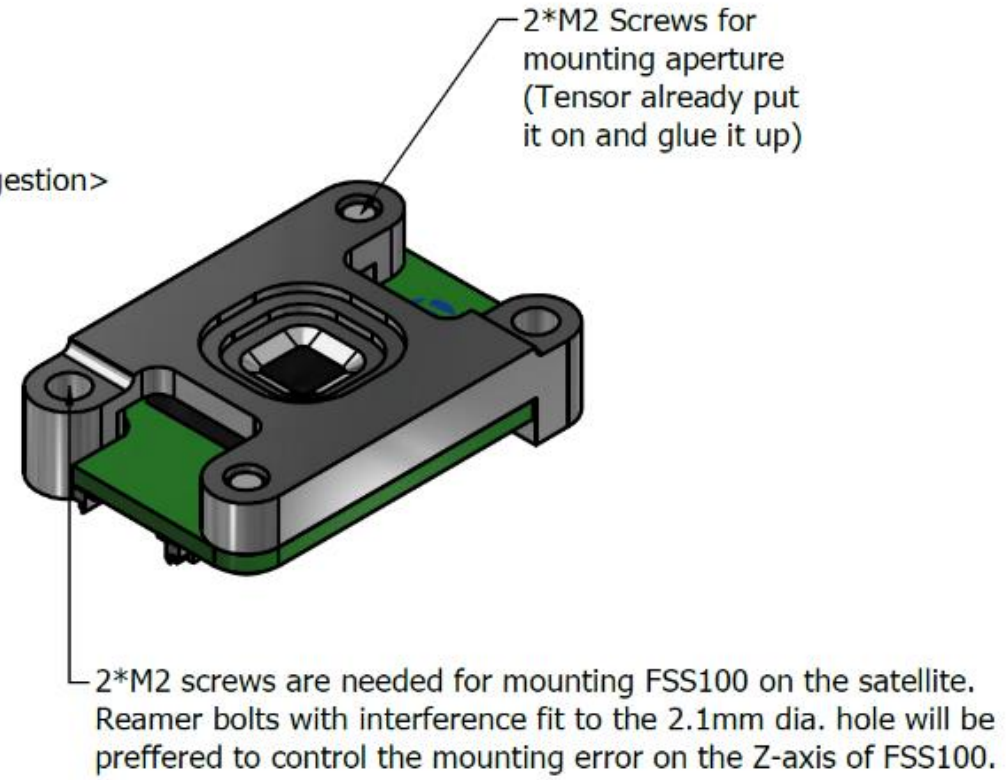

Updated Time	2021.12.14 (Tue.)	TENSOR TECH
FSS100 V2	Attachment 1. FSS100 Dimensions	