

# ENGR3426: Miniproject 3

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## Schematic Capture and Simulation

For MP3, we were tasked to design and lay out a 7-bit DAC using a MOSFET ladder network. We needed to meet several performance and operation requirements - the DAC needed to function for a range of supply and output voltages while maintaining good linearity.

To start the design process, we chose to work with the ladder network outlined in the assignment document. This ladder doesn't have particularly strict output voltage requirements, as the output transistor just needs to be held in saturation for proper operation. This is useful because mirroring the output current does require some voltage on that node below VDD.

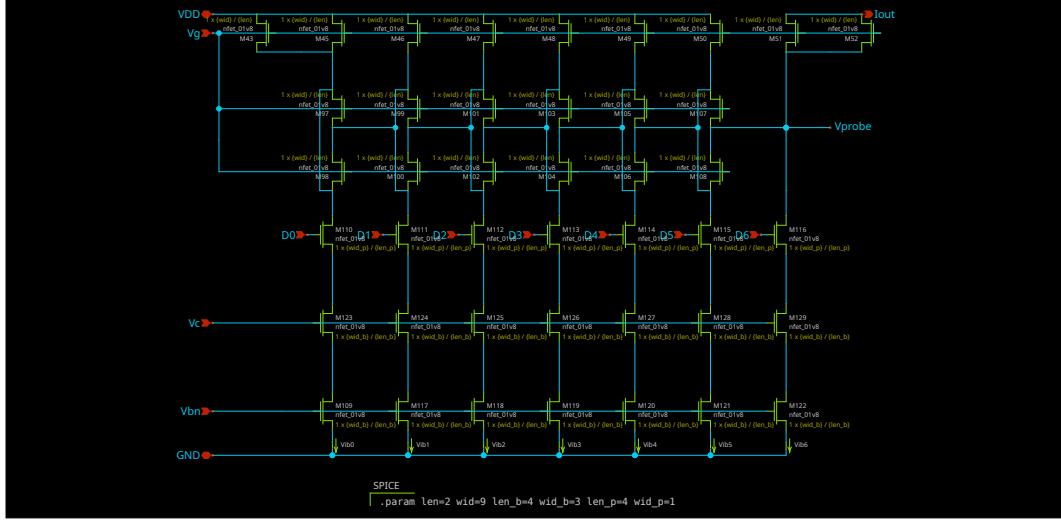


Figure 1: Transistor Level Schematic of MOSFET Ladder.

To make the switched current sinks, we added pass transistors which connect to the DACs digital inputs in series with cascoded bias transistors. An unforeseen consequence of this implementation is that because the cascaded bias transistors also have to remain above saturation to properly sink our bias current, our input voltage requirement for the next stage becomes stricter.

Despite this, we decided to cascode the bias transistors because it helped mitigate the Early effect, improving matching. To generate the cascode bias voltage ( $V_c$ ), we used a cascode bias circuit.

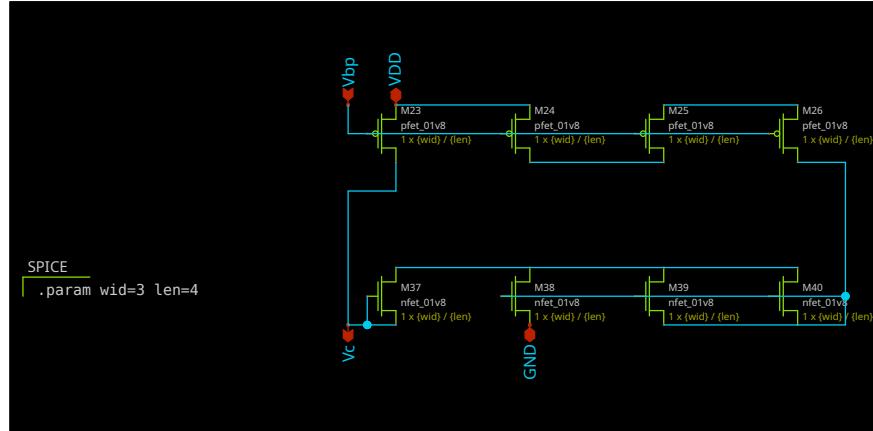


Figure 2: Transistor Level Schematic of Cascode Bias Circuit.

One requirement of our DAC is that it has to have less than a  $0.5\%/V$  change in  $I_{out}$  as  $V_{out}$  is swept over at least 80% of the power supply range. In order to do this, we needed to mirror the output current from the ladder. We chose to implement a PMOS version of the Cong and Geiger Mirror. This Mirror features an extremely flat output characteristic and a low input voltage requirement (around  $V_{dssat}$ ), making it a reasonable choice. This design generates its own PMOS cascode bias voltage.

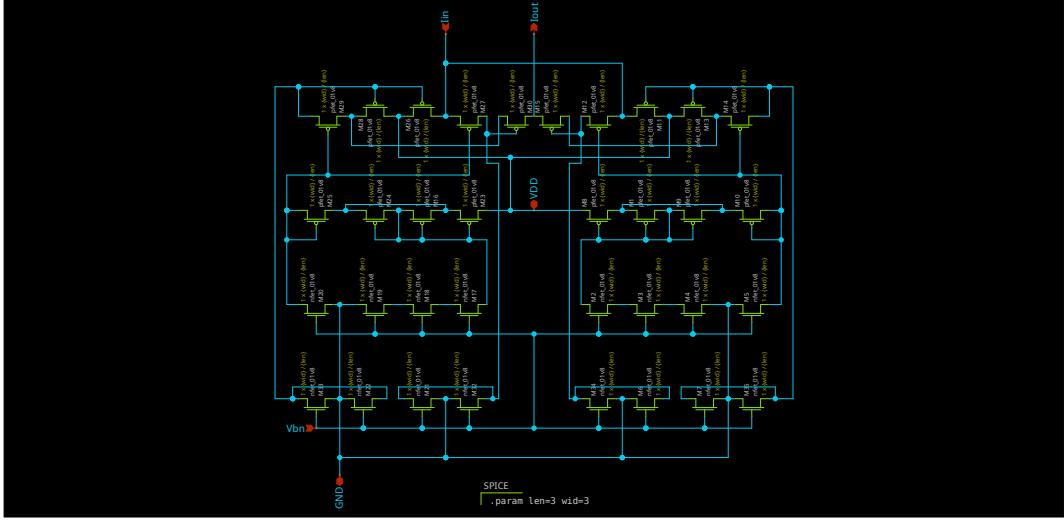


Figure 3: Transistor Level Schematic of our Current Mirror.

This current mirror does require an external bias, and it mirrors best when the bias is at least several times smaller than the input. Because of how the ladder operates, this means that we needed to divide down the bias current. We used the same principle as the ladder to create a 1/24 ratio.

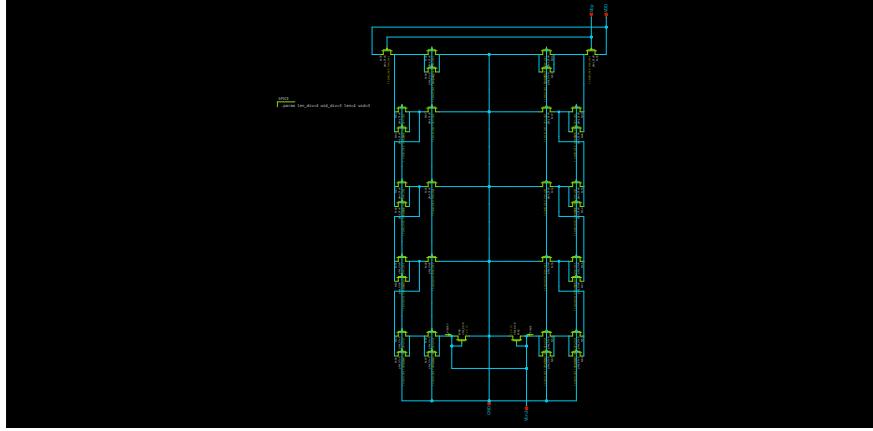


Figure 4: Transistor Level Schematic of Current Divider Circuit.

Another requirement of our DAC is that it has to have less than a  $0.5\%/V$  change in  $I_{out}$  for the range that it operates when  $VDD$  is swept. In other words, we needed supply-independent biasing. We ended up using the so-called "Magic Circuit" we covered in class.

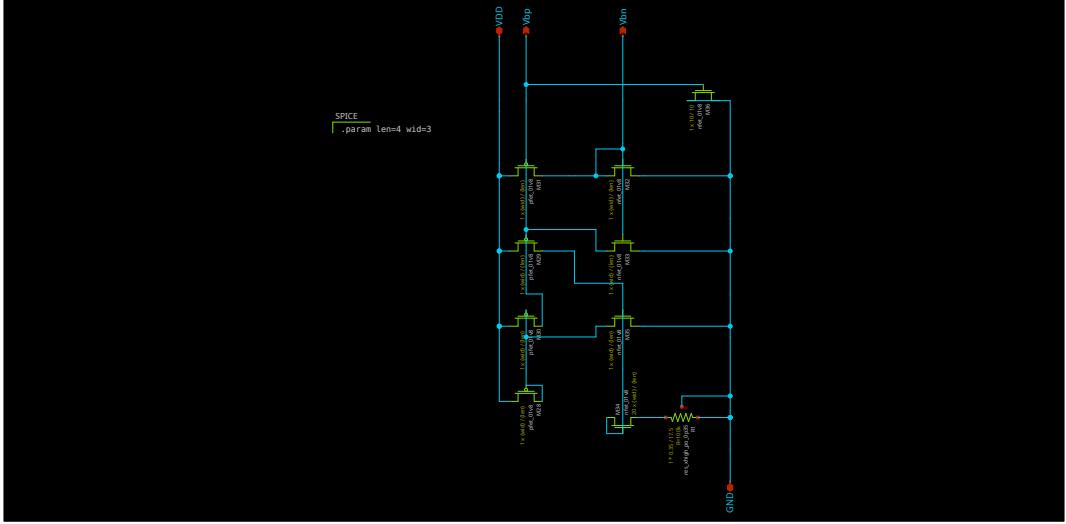


Figure 5: Transistor Level Schematic of our Bias Generator Circuit.

With all of these components, we created a hierarchical schematic of our DAC. We ran extensive transient simulations to ensure stability.

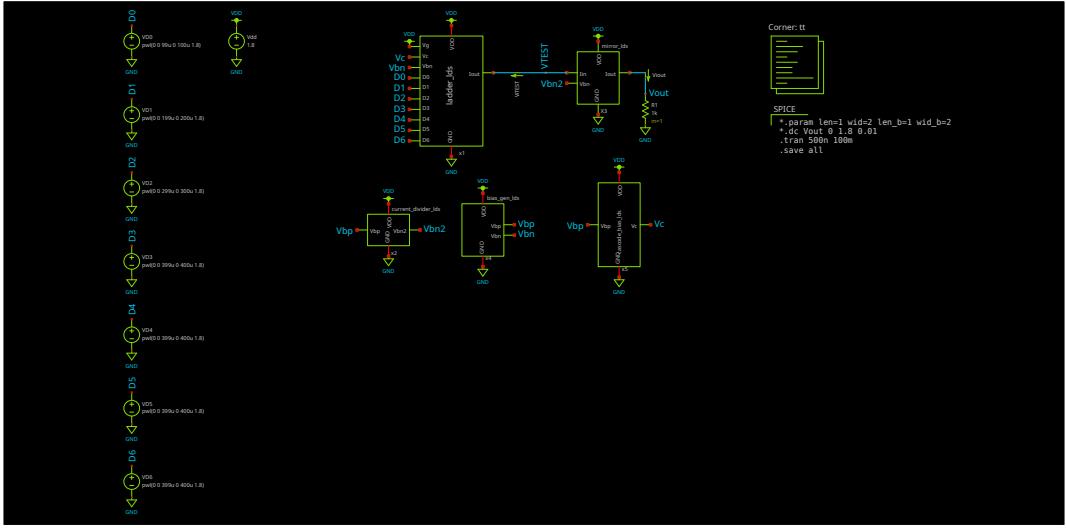


Figure 6: DAC Testbench.

Using a similar testbench with the SPICE from the example R-2R DAC, we looked at the output current for every digital input. We then normalized the output based on our bias current, allowing us to compute the DNL and INL of our DAC in terms of LSBs. The DAC needed to have less than 2 LSBs of DNL and less than 4 LSBs of INL.

For the TT corner, we achieved a DNL of 0.94 LSBs and an INL of -0.20 LSBs.

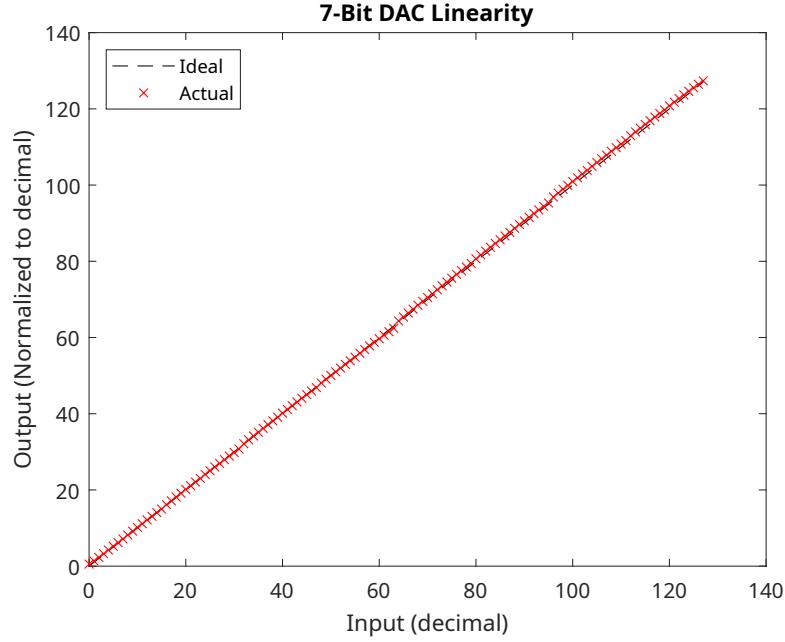


Figure 7: DAC Linearity.

Another requirement, which was particularly difficult, was to hit less than 8 LSBs of DNL/INL while using the mismatch models. We managed to achieve this in a run of 10 monte-carlo simulations.

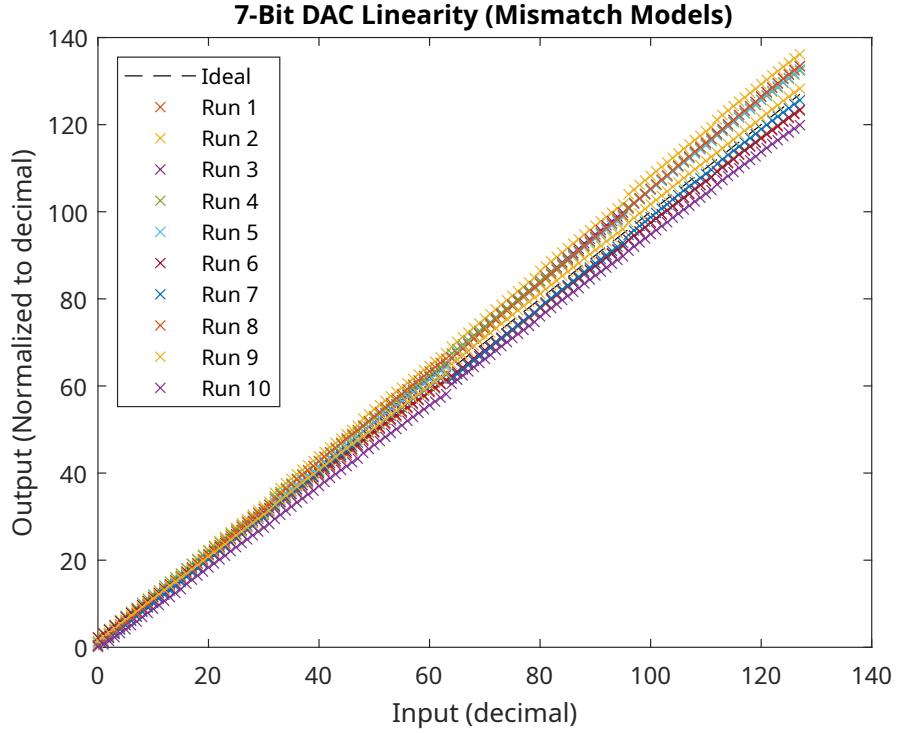


Figure 8: DAC Linearity with Mismatch.

The stats are as follows:

```
Run 1 Max DNL: 0.49166
Run 1 INL: -4.798
Run 2 Max DNL: 1.301
Run 2 INL: 7.9162
Run 3 Max DNL: 0.72349
Run 3 INL: 6.0911
Run 4 Max DNL: 1.2419
Run 4 INL: 3.0693
Run 5 Max DNL: 1.3314
Run 5 INL: 4.5819
Run 6 Max DNL: 0.30984
Run 6 INL: -5.9431
Run 7 Max DNL: 1.9677
Run 7 INL: -1.8717
Run 8 Max DNL: 0.90839
Run 8 INL: 5.858
Run 9 Max DNL: 1.2449
Run 9 INL: -0.25352
Run 10 Max DNL: 1.368
Run 10 INL: -7.1767
```

We swept  $V_{out}$ , and we found that there is a  $0.014\% / V$  change in  $I_{out}$  over 80% of the power supply range.

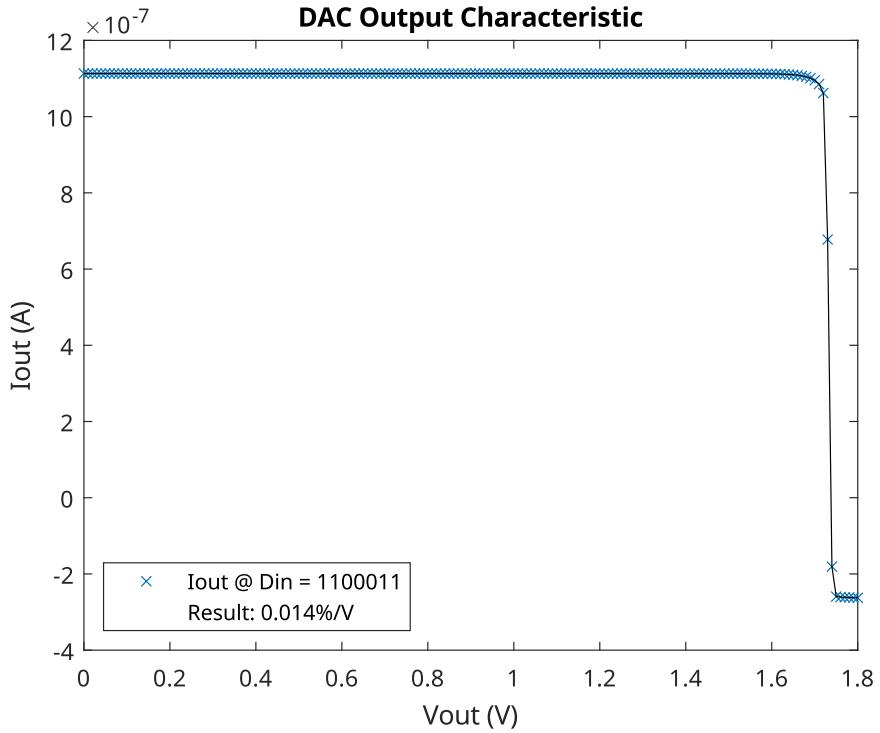


Figure 9: DAC Output Characteristic.

We swept  $V_{DD}$  and we found that for the range that the DAC operates in (about 1.4V - 1.8V), there is a  $0.946\% / V$  change in  $I_{out}$ .

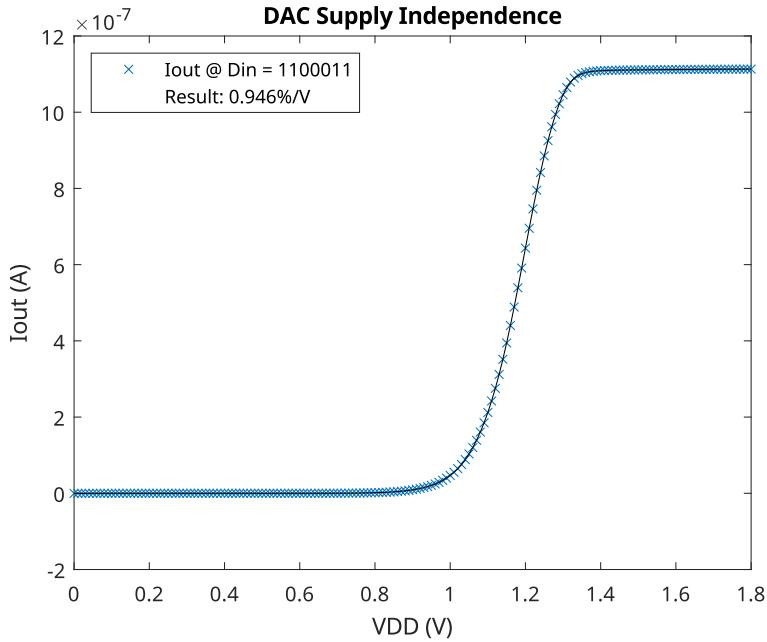


Figure 10: DAC Supply Independence.

## Layout & LVS

We used several best-practice analog layout techniques to minimize device mismatch. In general, we used fairly large transistors (several square microns in area) and minimized spacing in between devices.

The mirror and the current divider utilize common-centriod geometry to compensate for linear gradients.

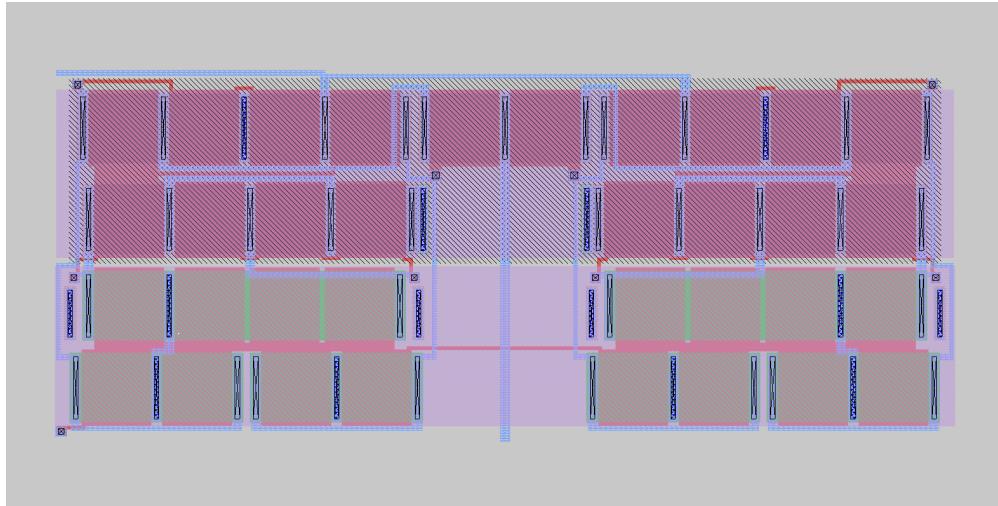


Figure 11: Current Mirror Layout.

The ladder, cascode bias, and bias generator all have their devices in the same orientation.

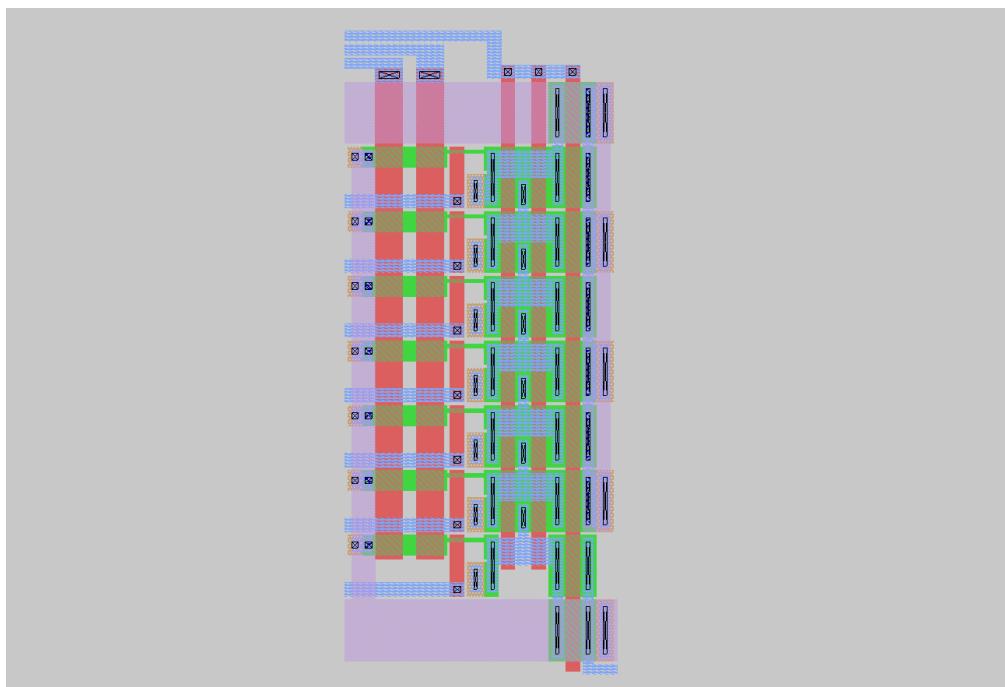


Figure 12: Current Mirror Layout.

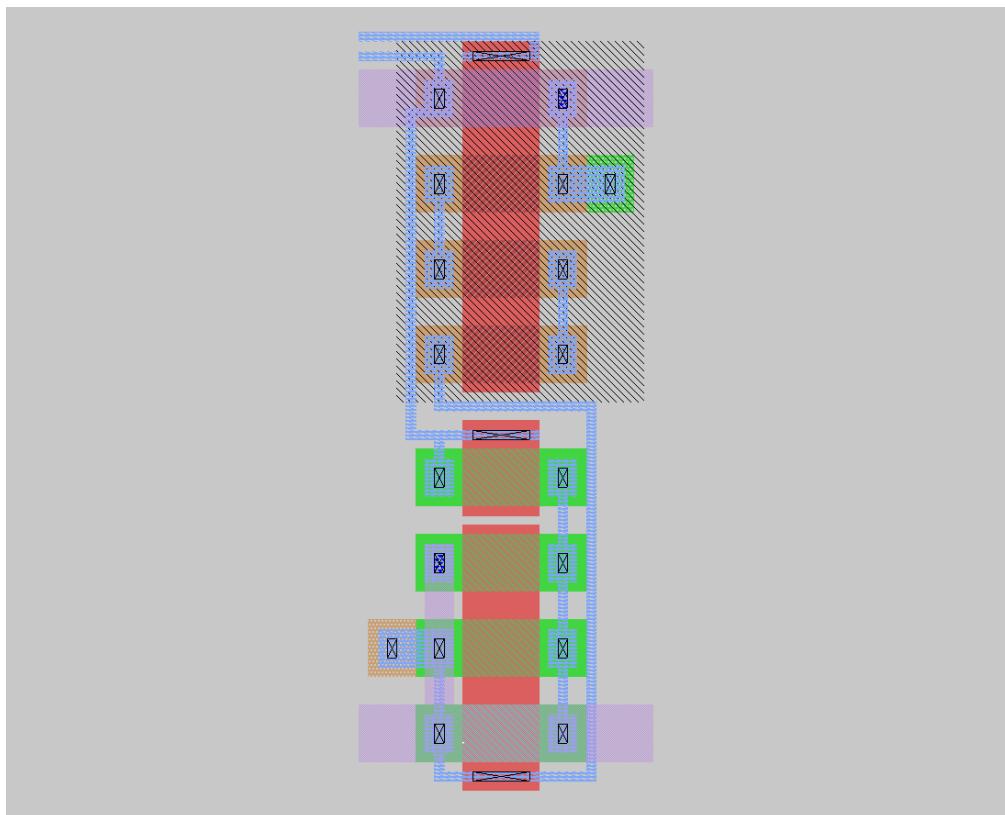


Figure 13: Cascode Bias Generator Layout.

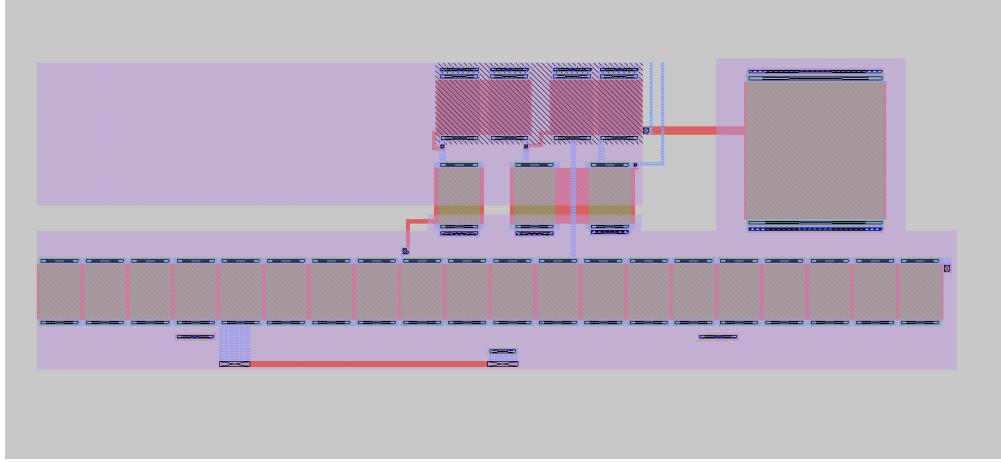


Figure 14: Supply-Independent Bias Generator Layout.

For the bias generator, we decided to use one of the P- precision resistors described here. This was kind of annoying to get working because for whatever reason it doesn't work the same as it did 4 years ago. We found this video helpful in fixing DRC.

Lastly, we connected all of our components. Something that we would probably change if we had time was consistency in layout. It's pretty easy to tell who did what block and there's clearly some issues in our cell I/O that could have been optimized further. Regardless, here is our final DAC layout:

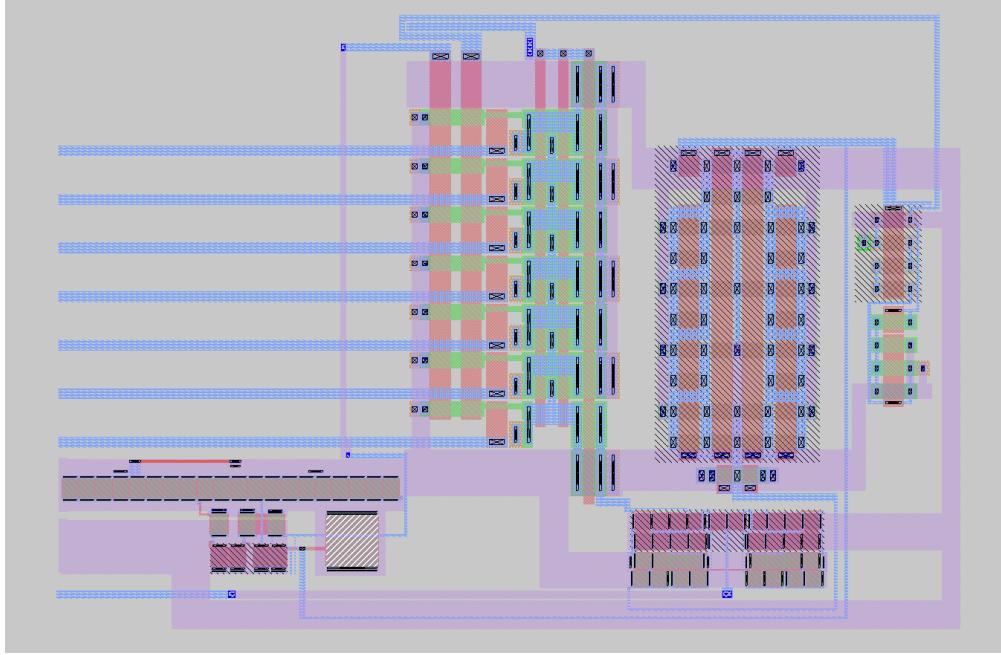


Figure 15: DAC Layout.

We then ran LVS, confirming that we had correctly laid out the DAC. There are property errors, but those stem from netgen not being able to deal with our parameterized schematics. The transistors are sized correctly.

Circuit 1 cell sky130\_fd\_pr\_\_nfet\_01v8 and Circuit 2 cell sky130\_fd\_pr\_\_nfet\_01v8 are black boxes.

```
Warning: Equate pins: cell sky130_fd_pr__nfet_01v8 is a placeholder, treated as a black box.  
Warning: Equate pins: cell sky130_fd_pr__nfet_01v8 is a placeholder, treated as a black box.
```

Subcircuit pins:

Circuit 1: sky130_fd_pr__nfet_01v8	Circuit 2: sky130_fd_pr__nfet_01v8
------------------------------------	------------------------------------

-----	-----
1	1
2	2
3	3
4	4

Cell pin lists are equivalent.

Device classes sky130\_fd\_pr\_\_nfet\_01v8 and sky130\_fd\_pr\_\_nfet\_01v8 are equivalent.

Circuit 1 cell sky130\_fd\_pr\_\_pfet\_01v8 and Circuit 2 cell sky130\_fd\_pr\_\_pfet\_01v8 are black boxes.

```
Warning: Equate pins: cell sky130_fd_pr__pfet_01v8 is a placeholder, treated as a black box.
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Subcircuit pins:

Circuit 1: sky130_fd_pr__pfet_01v8	Circuit 2: sky130_fd_pr__pfet_01v8
------------------------------------	------------------------------------

-----	-----
1	1
2	2
3	3
4	4

Cell pin lists are equivalent.

Device classes sky130\_fd\_pr\_\_pfet\_01v8 and sky130\_fd\_pr\_\_pfet\_01v8 are equivalent.

Circuit 1 cell sky130\_fd\_pr\_\_res\_xhigh\_po\_0p35 and Circuit 2 cell sky130\_fd\_pr\_\_res\_xhigh\_po\_0p35 are b

```
Warning: Equate pins: cell sky130_fd_pr__res_xhigh_po_0p35 is a placeholder, treated as a black box.
```

```
Warning: Equate pins: cell sky130_fd_pr__res_xhigh_po_0p35 is a placeholder, treated as a black box.
```

Subcircuit pins:

Circuit 1: sky130_fd_pr__res_xhigh_po_0p35	Circuit 2: sky130_fd_pr__res_xhigh_po_0p35
--	--

-----	-----
1	1
2	2
3	3

Cell pin lists are equivalent.

Device classes sky130\_fd\_pr\_\_res\_xhigh\_po\_0p35 and sky130\_fd\_pr\_\_res\_xhigh\_po\_0p35 are equivalent.

Flattening unmatched subcell ladder\_lds in circuit dac\_xschem (0)(1 instance)

Flattening unmatched subcell current\_divider\_lds in circuit dac\_xschem (0)(1 instance)

Flattening unmatched subcell mirror\_lds in circuit dac\_xschem (0)(1 instance)

Flattening unmatched subcell bias\_gen\_lds in circuit dac\_xschem (0)(1 instance)

Flattening unmatched subcell cascode\_bias\_lds in circuit dac\_xschem (0)(1 instance)

Flattening unmatched subcell bias\_gen in circuit mag\_DAC (1)(1 instance)

Flattening unmatched subcell mag\_current\_div in circuit mag\_DAC (1)(1 instance)

Flattening unmatched subcell mag\_ladder in circuit mag\_DAC (1)(1 instance)

Flattening unmatched subcell mag\_cascode\_bias in circuit mag\_DAC (1)(1 instance)

Flattening unmatched subcell mirror in circuit mag\_DAC (1)(1 instance)

Class dac\_xschem (0): Merged 28 parallel devices.

```

Class mag_DAC (1): Merged 47 parallel devices.
Subcircuit summary:
Circuit 1: dac_xschem |Circuit 2: mag_DAC
-----
sky130_fd_pr_nfet_01v8 (88->55) |sky130_fd_pr_nfet_01v8 (88->55)
sky130_fd_pr_pfet_01v8 (58->44) |sky130_fd_pr_pfet_01v8 (58->44)
sky130_fd_pr_res_xhigh_po_0p35 (1) |sky130_fd_pr_res_xhigh_po_0p35 (1)
Number of devices: 100 |Number of devices: 100
Number of nets: 69 |Number of nets: 69
-----

Resolving symmetries by property value.
Resolving symmetries by pin name.
Resolving symmetries by net name.
Netlists match with 37 symmetries with property errors.
mirror_lds:3/sky130_fd_pr_pfet_01v8:M16 vs. mirror_0/sky130_fd_pr_pfet_01v8:9:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M1 vs. mirror_0/sky130_fd_pr_pfet_01v8:3:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M28 vs. mirror_0/sky130_fd_pr_pfet_01v8:13:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M13 vs. mirror_0/sky130_fd_pr_pfet_01v8:2:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M23 vs. mirror_0/sky130_fd_pr_pfet_01v8:24:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M8 vs. mirror_0/sky130_fd_pr_pfet_01v8:16:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M14 vs. mirror_0/sky130_fd_pr_pfet_01v8:20:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M29 vs. mirror_0/sky130_fd_pr_pfet_01v8:26:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M26 vs. mirror_0/sky130_fd_pr_pfet_01v8:29:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M11 vs. mirror_0/sky130_fd_pr_pfet_01v8:25:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M30 vs. mirror_0/sky130_fd_pr_pfet_01v8:31:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M15 vs. mirror_0/sky130_fd_pr_pfet_01v8:21:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M27 vs. mirror_0/sky130_fd_pr_pfet_01v8:8:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M12 vs. mirror_0/sky130_fd_pr_pfet_01v8:33:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M25 vs. mirror_0/sky130_fd_pr_pfet_01v8:30:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr_pfet_01v8:M10 vs. mirror_0/sky130_fd_pr_pfet_01v8:6:
  L circuit1: 4  circuit2: 3  (delta=28.6%, cutoff=1%)
ladder_lds:1/sky130_fd_pr_nfet_01v8:M51 vs. mag_ladder_0/sky130_fd_pr_nfet_01v8:1:
  W circuit1: (unresolved expression) 18 (property type mismatch)
  L circuit1: (unresolved expression) 2 (property type mismatch)
ladder_lds:1/sky130_fd_pr_nfet_01v8:M43 vs. mag_ladder_0/sky130_fd_pr_nfet_01v8:3:
  W circuit1: (unresolved expression) 18 (property type mismatch)
  L circuit1: (unresolved expression) 2 (property type mismatch)
ladder_lds:1/sky130_fd_pr_nfet_01v8:M116 vs. mag_ladder_0/sky130_fd_pr_nfet_01v8:11:
  W circuit1: (unresolved expression) 1 (property type mismatch)

```





```

mirror_lds:3/sky130_fd_pr__nfet_01v8:M21 vs. mirror_0/sky130_fd_pr__nfet_01v8:5:
L circuit1: 4 circuit2: 3 (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr__nfet_01v8:M7 vs. mirror_0/sky130_fd_pr__nfet_01v8:10:
L circuit1: 4 circuit2: 3 (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr__nfet_01v8:M22 vs. mirror_0/sky130_fd_pr__nfet_01v8:19:
L circuit1: 4 circuit2: 3 (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr__nfet_01v8:M17 vs. mirror_0/sky130_fd_pr__nfet_01v8:22:
L circuit1: 4 circuit2: 3 (delta=28.6%, cutoff=1%)
mirror_lds:3/sky130_fd_pr__nfet_01v8:M2 vs. mirror_0/sky130_fd_pr__nfet_01v8:1:
L circuit1: 4 circuit2: 3 (delta=28.6%, cutoff=1%)

```

Subcircuit pins:

Circuit 1: dac_xschem	Circuit 2: mag_DAC
Iout	Iout
GND	GND
VDD	VDD
D3	D3
D2	D2
D4	D4
D5	D5
D1	D1
D0	D0
D6	D6

Cell pin lists are equivalent.

Device classes dac\_xschem and mag\_DAC are equivalent.

Final result: Circuits match uniquely.

Property errors were found.

The following cells had property errors:

dac\_xschem

## Design Files

All of our design files for this project can be found in this github repository.