

DSP Power

U1B TMS320C5535

ANA_LDO_OUT

3.3V

Power Regulation

CON1

BARREL_JACK_PWR

BT1 Battery

SL04-E3-08

U3

VR3V3

3.3V

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Title:

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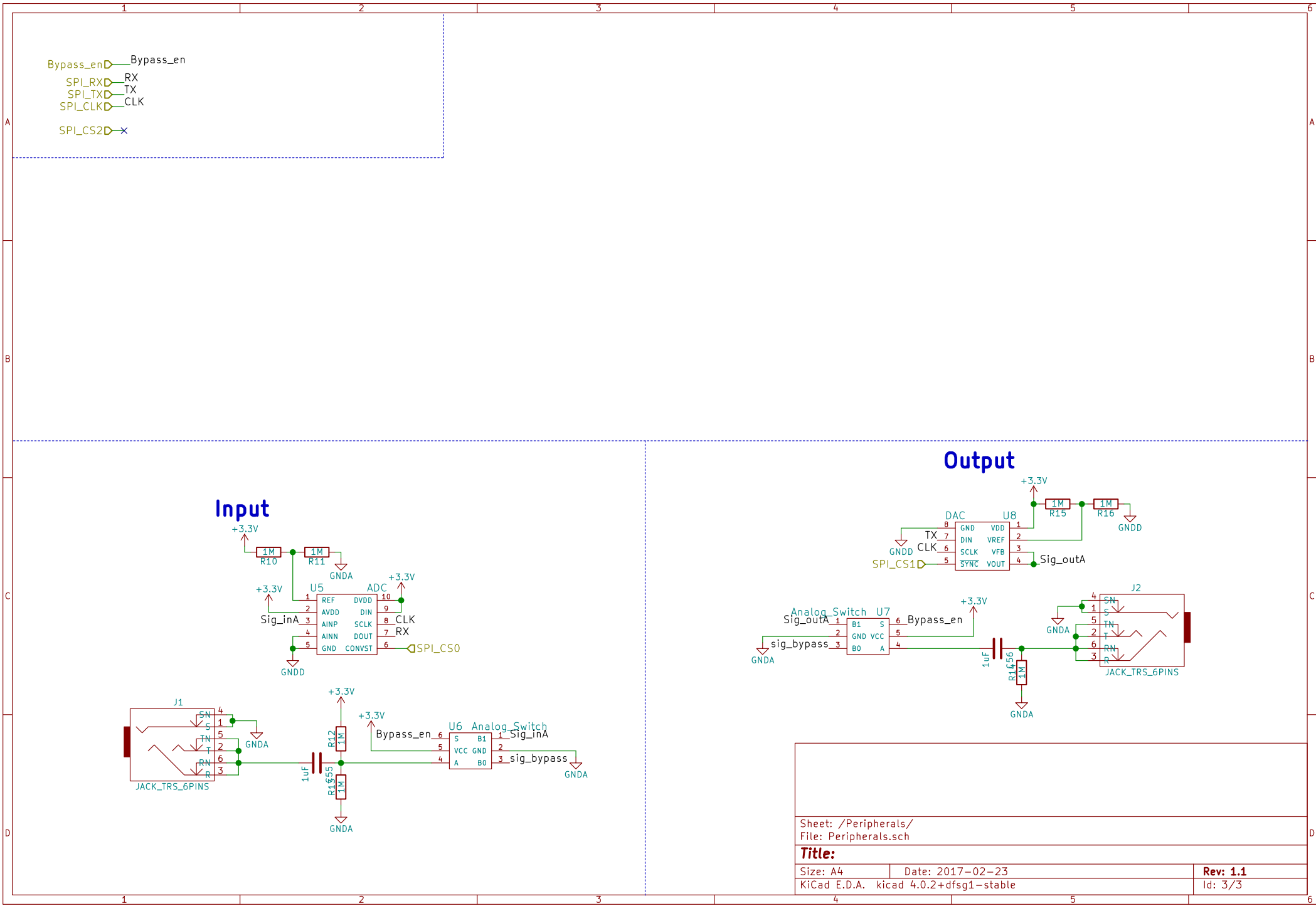
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The schematic diagram illustrates the DAC and Analog Switch circuit. The DAC (U8) is configured with its TX pin to GND, CLK pin to SPI_CS1, and SCLK pin to GND. The VREF pin is connected to a +3.3V supply through a 1MΩ resistor (R15). The VFB pin is connected to GND through a 1MΩ resistor (R16). The VOUT pin is connected to the Sig_outA signal. The Analog Switch (U7) is configured with its B1 pin to Sig_outA, B0 pin to GND, and S pin to Bypass_en. The A pin is connected to the output of the DAC (Sig_outA) through a 1μF capacitor and a 1MΩ resistor (R1456). The output of the Analog Switch is connected to the JACK_TRS_6PINS connector (J2).

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