	Fmax	Setup Time
Slow 1100mV 85C	442.67 MHz	-1.259
Slow 1100mV 0C	424.27 MHz	-1.357
Fast 1100mV 85C	N/A	-0.271
Fast 1100mV 0C	N/A	-0.207

Longest Path: -1.259

From Synchronizer:Synchonizer_1|flop_2[13] **to** Synchronizer:Synchonizer_Sum|flop_1[14]

Clock Delay: -0.060

Data Delay: 2.029

Slack: -1.259

	Fmax	Setup Time
Slow 1100mV 85C	274.05 MHz	16.351
Slow 1100mV 0C	275.18 MHz	16.366
Fast 1100mV 85C	N/A	17.696
Fast 1100mV 0C	N/A	17.883

Longest Path: 17.030

FROM Synchronizer:Synchonizer_2|flop_2[2] **TO** Synchronizer:Synchonizer_Sum|flop_1[6]

Clock Delay: -0.071

Data Delay: 2.729

Slack: 17.030

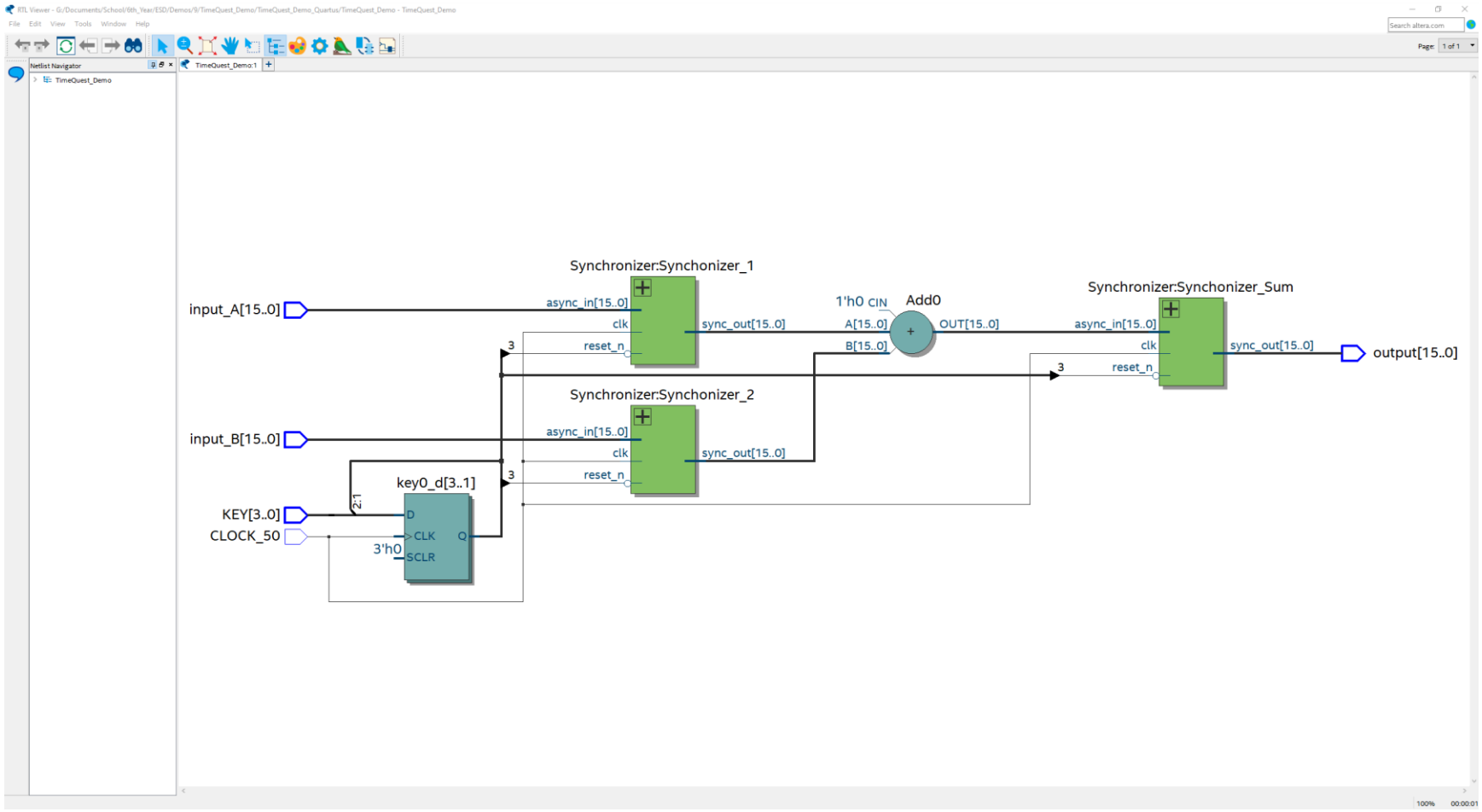
New slack for previously failing path: 18.090

New Clock Delay: -0.072

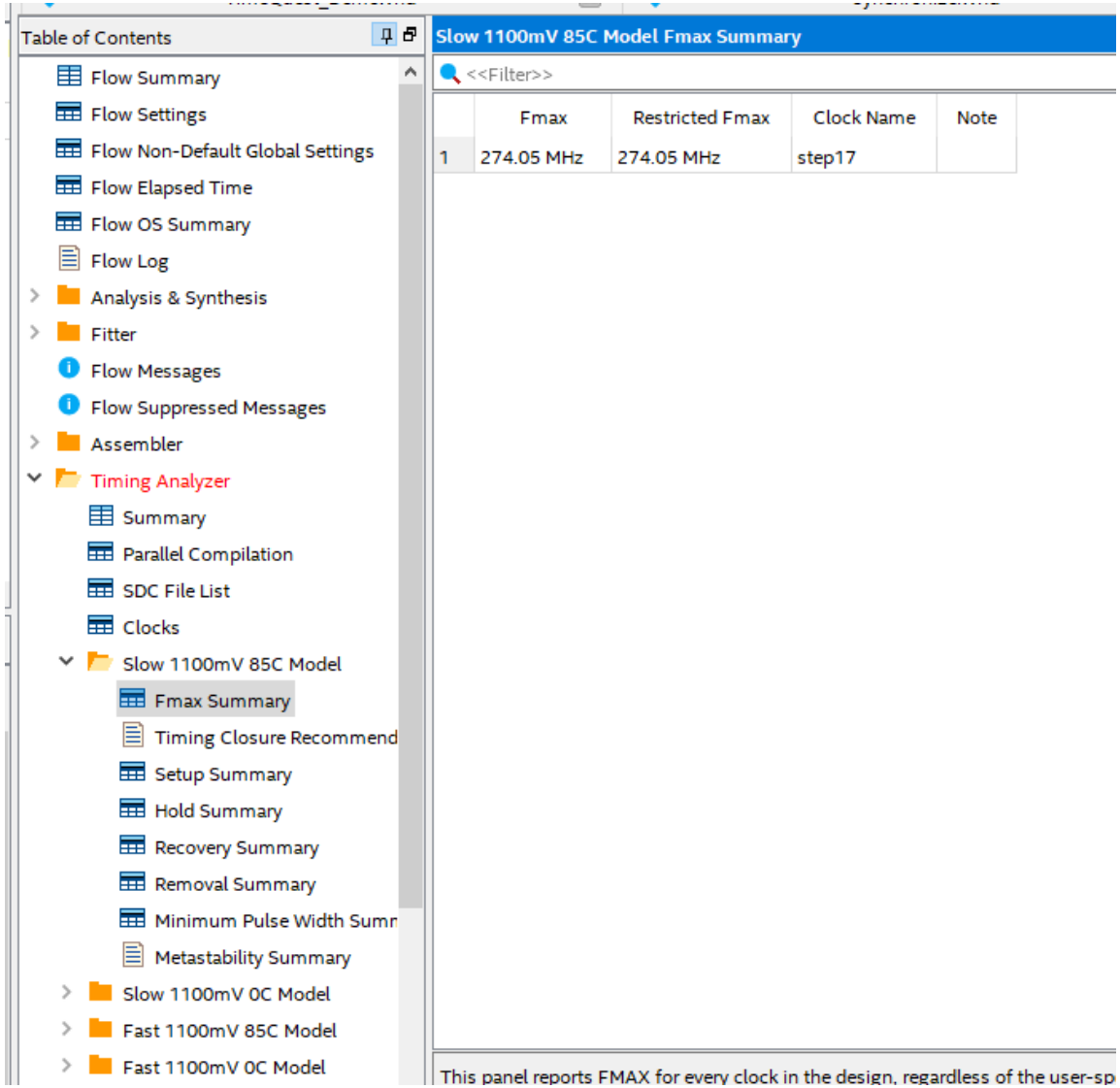
New Data Delay: 1.668

New Slack: 18.090

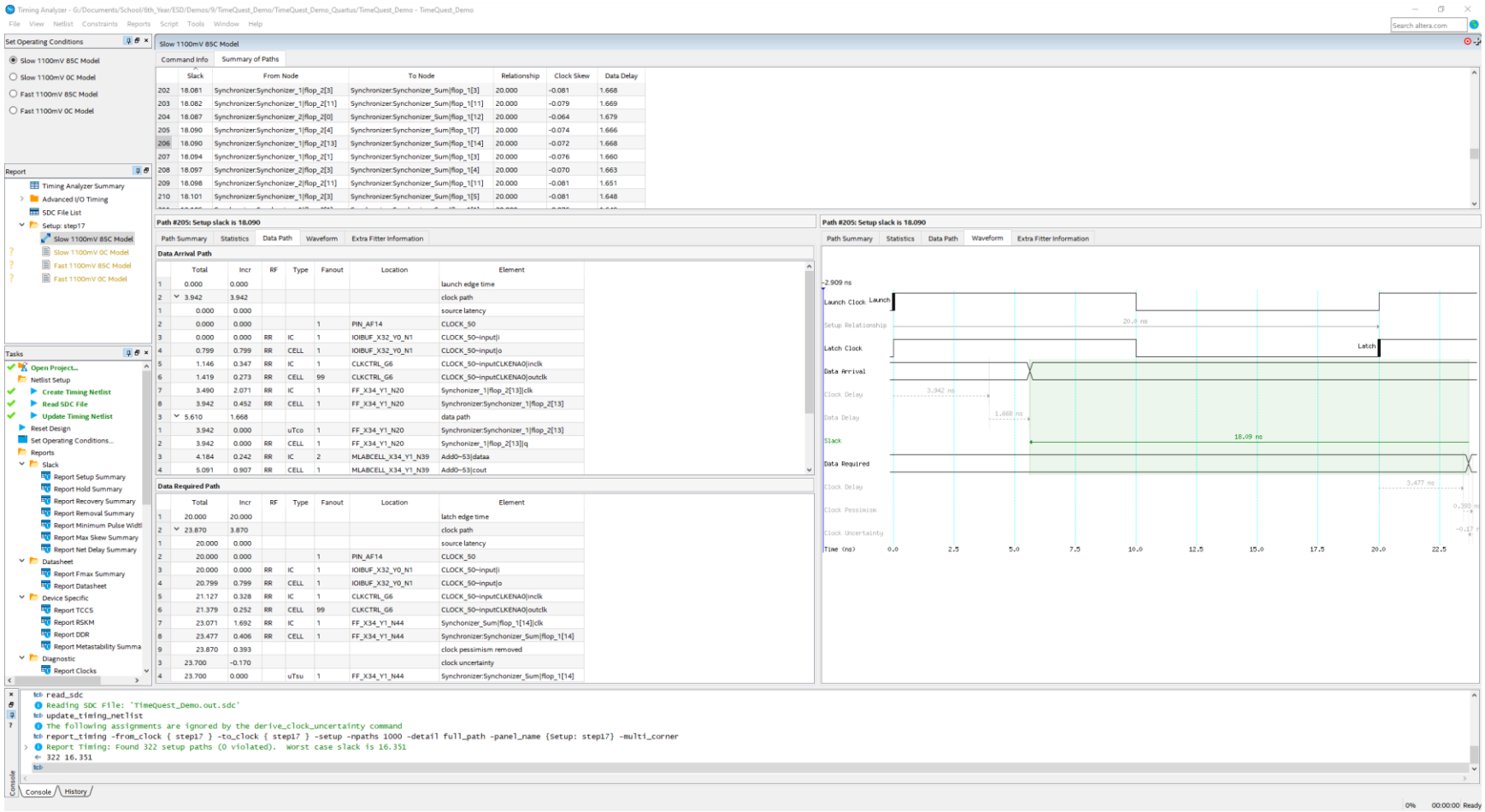
The clock delays are close, with the previous being -0.060 compared to the new value of -0.072. Data delays are a bit different, with a previous value of 2.029, and a new lower value of 1.668. And the biggest difference is in the slack times, with an original value of -1.259 and a new value of 18.090.


Synchronizer:Synchonizer_1
input_A[15..0]
async_in[15..0]
clk
reset_n
sync_out[15..0]
3
1'h0 CIN
Add0
A[15..0]
B[15..0]
OUT[15..0]
Synchronizer:Synchonizer_Sum
async_in[15..0]
clk
reset_n
sync_out[15..0]
output[15..0]
3
Synchronizer:Synchonizer_2
input_B[15..0]
async_in[15..0]
clk
reset_n
sync_out[15..0]
3
key0_d[3..1]
2:1
KEY[3..0]
CLOCK_50
D
CLK
Q
3'h0
SCLR

RTL View



Example of one of the model analyses for checking the Fmax value (in this case, for Slow 1100mV 85C model)



Step 25: Image showing the new information (path 206) for the previously failing path from steps 11-14.

At first, the slack is negative, meaning that I need to save that much time in order to pass the 1 nanosecond time constaraint. Once the clock is changed to the 20 nanosecond period, the slack is positive, and the Fmax changes as well. The data is no longer computed behind schedule, so the new design is faster. The timequest tool is useful in performing detailed analysis of design timing, with any issues regarding setup/completion time being easily viewed and fixed, so that the designs can be completed quick.