# DBG16 Overview

DBG16 is a simple RISC processor with eight sixteen bit registers. It supports a 24 bit code address and 16 bit data address. DBG16 makes use of a 64 entry return address stack internal to the processor. Interrupts and exceptions are not supported.

|  |  |  |
| --- | --- | --- |
| Regno |  |  |
| 0 | This register is always zero |  |
| 1 |  |  |
| 2 |  |  |
| 3 |  |  |
| 4 |  |  |
| 5 |  |  |
| 6 |  |  |
| 7 |  |  |

# Instruction Formats:

Register-Immediate Format:

|  |  |  |  |
| --- | --- | --- | --- |
| 15 11 | 10 8 | 7 5 | 4 0 |
| Immediate5 | Rt3 | Ra3 | Opcode5 |

Register-Register Format:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 15 14 | 13 11 | 10 8 | 7 5 | 4 0 |
| Fn2 | Rt3 | Rt3 | Ra3 | Opcode5 |

Conditional Branch Format:

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 5 | 4 0 |
| Displacement8 | Ra3 | Opcode5 |

Jump Format:

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 5 | 4 0 |
| Address7..0 | ~3 | Opcode5 |
| Address23..8 | | |

# Instruction Set Summary

|  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 02 | Rt3 | Rb3 | | Ra3 | | | | | 25 | ADD Rt,Ra,Rb |
| 12 | Rt3 | Rb3 | | Ra3 | | | | | 25 | SUB Rt,Ra,Rb |
| 22 | Rt3 | Rb3 | | Ra3 | | | | | 25 | CMP Rt,Ra,Rb |
| 32 | Rt3 | Rb3 | | Ra3 | | | | | 25 | CMPU Rt,Ra,Rb |
| 02 | Rt3 | Rb3 | | Ra3 | | | | | 35 | AND Rt,Ra,Rb |
| 12 | Rt3 | Rb3 | | Ra3 | | | | | 35 | OR Rt,Ra,Rb |
| 22 | Rt3 | Rb3 | | Ra3 | | | | | 35 | XOR Rt,Ra,Rb |
| Immediate5 | | | Rt3 | | Ra3 | | | 45 | | ADDI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 55 | | SUBI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 65 | | CMPI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 75 | | CMPUI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 85 | | ANDI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 95 | | ORI Rt,Ra,#i5 |
| Immediate5 | | | Rt3 | | Ra3 | | | 105 | | XORI Rt,Ra,#i5 |
| 02 | Rt3 | Rb3 | | Ra3 | | | | | 115 | SHL Rt,Ra,Rb |
| 12 | Rt3 | Rb3 | | Ra3 | | | | | 115 | SHR Rt,Ra,Rb |
| 22 | Rt3 | Imm3 | | Ra3 | | | | | 115 | SHLI Rt,Ra,#i3 |
| 32 | Rt3 | Imm3 | | Ra3 | | | | | 115 | SHRI Rt,Ra,#i3 |
| Immediate8 | | | | | Rt3 | | | 125 | | LDI Rt, #i8 |
| Displacement8 | | | | | | Ra3 | 165 | | | BEQ Ra, label |
| Displacement8 | | | | | | Ra3 | 175 | | | BNE Ra, label |
| Displacement8 | | | | | | Ra3 | 185 | | | BMI Ra, label |
| Displacement8 | | | | | | Ra3 | 195 | | | BPL Ra, label |
| Address7..0 | | | | | | ~3 | | 205 | | JMP Address |
| Address23..8 | | | | | | | | | |
| Address7..0 | | | | | | ~3 | | 215 | | JSR Address |
| Address23..8 | | | | | | | | | |
| ~11 | | | | | | | 225 | | | RTS |
| Address5 | | | Rt3 | | Ra3 | | | 245 | | LW Rt,d5(Ra) |
| Address5 | | | Rt3 | | Ra3 | | | 255 | | SW Rt,d5(Ra) |

## Immediate Constant Extension

**The five bit immediate constant may be extended to 16 bits using the code 10h/16d.**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 165 | Rt3 | Ra3 | 45 | ADDI Rt,Ra,#i16 |
| Immediate16 | | | |

## Condtional Branches

Conditional branches are based on the value in a register. They may branch on four different register statuses; zero, non-zero, plus, or minus. The status of the register may be setup by a compare instruction.

## Compare Instructions

Compare instructions set the value of a target register to -1, 0, or +1 depending on a comparison of a register to another register or immediate value. -1, 0, +1 represent a less than, equal or greater than result.