General Register Array

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
|  | Desgination |  |  | Designation |
| r0 | always zero |  | r32 |  |
| r1 | 1st return value |  | r33 |  |
| r2 | 2nd return value |  | r34 |  |
| r3 | 1st argument |  | r35 |  |
| r4 | … |  | r36 |  |
| r5 |  |  | r37 |  |
| r6 |  |  | r38 |  |
| r7 |  |  | r39 |  |
| r8 |  |  | r40 |  |
| r9 |  |  | r41 |  |
| r10 | 8th argument |  | r42 |  |
| r11 | 1st callee saved |  | r43 |  |
| r12 |  |  | r44 |  |
| r13 |  |  | r45 |  |
| r14 |  |  | r46 |  |
| r15 |  |  | r47 |  |
| r16 | register vars |  | r48 |  |
| r17 |  |  | r49 |  |
| r18 |  |  | tp / r50 | thread pointer |
| r19 |  |  | xlr / r51 | try/catch exception link reg. |
| r20 |  |  | bp / r52 | base pointer |
| r21 |  |  | sp / r53 | stack pointer |
| r22 | 12th callee saved |  | gp / r54 | global pointer |
| r23 | 1st caller saved |  | lr / r55 | link register |
| r24 |  |  | flg0 / r56 | flags registers to store the result of a compare operation |
| r25 |  |  | flg1 / r57 |
| r26 | temporaries |  | flg2 / r58 |
| r27 |  |  | flg3 / r59 |
| r28 |  |  | flg4 / r60 |
| r29 |  |  | flg5 / r61 |
| r30 | 8th caller saved |  | flg6 / r62 |
| r31 |  |  | pc / r63 | program counter relative addressing |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  | | | | | | | Rt6 | | | | | Ra6 | Opcode6 |  |
| ~22 | | | | | | | | H | | | ~2 | Vecno9 | | 00 | BRK |
| 04 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | ADD |
| 05 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | SUB |
| 06 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | CMP |
| 07 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | MUL |
| 08 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | MULU |
| 09 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | DIV |
| 10 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | DIVU |
| 12 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | AND |
| 13 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | OR |
| 14 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | XOR |
| 16 | Spr10 | | | | ~6 | | | ~6 | | | | | Ra6 | 02 | MTSPR |
| 17 | Spr10 | | | | Rt6 | | | ~6 | | | | | ~6 | 02 | MFSPR |
| 18 | ~10 | | | | ~6 | | | H | | ~5 | | | ~6 | 02 | RTE / RTI |
| 19 | ~10 | | | | Rt6 | | | ~6 | | | | | Ra6 | 02 | NEXTPC |
| 24 | 03 | ~7 | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | SHL |
| 24 | 13 | ~7 | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | SRU |
| 24 | 23 | ~7 | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | SRA |
| 25 | 03 | ~7 | | | Rt6 | | | Imm6 | | | | | Ra6 | 02 | SHLI |
| 25 | 13 | ~7 | | | Rt6 | | | Imm6 | | | | | Ra6 | 02 | SRUI |
| 25 | 23 | ~7 | | | Rt6 | | | Imm6 | | | | | Ra6 | 02 | SRAI |
| 26 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | MOD |
| 27 | ~10 | | | | Rt6 | | | Rb6 | | | | | Ra6 | 02 | MODU |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 04 | ADDI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 05 | SUBI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 06 | CMPI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 07 | MULI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 08 | MULUI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 09 | DIVI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 10 | DIVUI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 12 | ANDI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 13 | ORI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 14 | XORI |
| Displacement19 | | | | | | | Op3 | Rb6 | | | | | Ra6 | 16 | Bcc |
| Displacement19 | | | | | | | Op3 | Rb6 | | | | | Ra6 | 17 | Bcc |
| Displacement19 | | | | | | | Op3 | Rb6 | | | | | Ra6 | 18 | Bcc |
| Displacement22 | | | | | | | | Rt6 | | | | | Ra6 | 22 | JAL |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 26 | MODI |
| Immediate22 | | | | | | | | Rt6 | | | | | Ra6 | 27 | MODUI |
|  |  | | | | |  | | | | | | |  |  |  |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 32 | LB |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 33 | LBU |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 34 | LC |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 35 | LCU |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 36 | LH |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 37 | LHU |
| Disp11 | | | Sc2 | Md3 | | Rt6 | | | Rb6 | | | | Ra6 | 38 | LW |
| Disp11 | | | Sc2 | Md3 | | Rs6 | | | Rb6 | | | | Ra6 | 39 | SB |
| Disp11 | | | Sc2 | Md3 | | Rs6 | | | Rb6 | | | | Ra6 | 40 | SC |
| Disp11 | | | Sc2 | Md3 | | Rs6 | | | Rb6 | | | | Ra6 | 41 | SH |
| Disp11 | | | Sc2 | Md3 | | Rs6 | | | Rb6 | | | | Ra6 | 42 | SW |
| Disp11 | | | Sc2 | Md3 | | Imm6 | | | Rb6 | | | | Ra6 | 43 | INC |
|  | | | | | | | | | | | | | | 59 | NOP |
| Constant34 | | | | | | | | | | | | | | 60 | IMM1 |
| Constant34 | | | | | | | | | | | | | | 61 | IMM2 |

|  |  |  |
| --- | --- | --- |
| Md3 |  |  |
| 0 |  | reserved |
| 1 | d11[Ra+Rb\*Sc] | scaled indexed with displacement |
| 2 | d11[Ra+Rb\*Sc]-- | post auto-decrement |
| 3 | d11[Ra+Rb\*Sc]++ | post auto-increment |
| 4 |  | reserved |
| 5 | [d11[Ra]][Rb\*Sc] | memory indirect |
| 6 | [d11[Ra]][Rb\*Sc]-- | memory indirect |
| 7 | [d11[Ra]][Rb\*Sc]++ | memory indirect |

Rb increments or decrements by one.

If Rb is zero then Ra increments / decrements by the size of the operand.

Synthesized Modes

|  |  |  |
| --- | --- | --- |
| 1 | d11[Ra] | Set Rb to zero |
| 2 | d11[Ra]-- | Set Rb to zero |
| 3 | d11[Ra]++ | Set Rb to zero |
| 1 | [Ra] | Set Rb, disp11 to zero |
| 2 | [Ra]-- | Set Rb, disp11 to zero |
| 3 | [Ra]++ | Set Rb, disp11 to zero |

Scale

|  |  |
| --- | --- |
| Sc2 | \* |
| 0 | 1 |
| 1 | 2 |
| 2 | 4 |
| 3 | 8 |

Auto-Increment / Decrement

The difference between register indirect with displacement and scaled indexed addressing is primarily the size of the displacement. Register indirect with displacement mode can be synthesized from the scaled indexed addressing mode by setting Rb to zero.

Auto-increment / decrement is available only to scaled indexed address modes. In all likely-hood the displacement would be zero anyway when auto-increment or decrement is in use.