|  |  |  |  |
| --- | --- | --- | --- |
|  | In/Out |  |  |
| CLK | I | Input clock 32 MHz |  |
| PHI11 | O | 1 MHz Output phase 1 (non-overlapping) |  |
| PHI12 | O | 1 MHz Output phase 2 (non-overlapping) |  |
| PHI81 | O | 8 MHz Output phase 1 (non-overlapping) |  |
| PHI82 | O | 8 MHz Output phase 2 (non-overlapping) |  |
| PHI31 | O | 32 MHz |  |
| RST | I | reset |  |
| IRQ | I |  |  |
| NMI | I |  |  |
| ABORTB | I | abort |  |
| E | O | emulation status |  |
| BE | I | bus enable (tri-state the output signals) |  |
| BZ | I | bus zero (zero the output signals) |  |
| MLB | O | memory lock |  |
| MX | O | mode select (M/X bits of status reg) |  |
| CS0 | O | Chip select |  |
| CS1 | O | Chip select |  |
| CS2 | O | Chip select |  |
| CS3 | O | Chip select |  |
| CS4 | O | Chip select |  |
| CS5 | O | Chip select |  |
| CS6 | O | Chip Select Other |  |
| VDA | O | valid data address |  |
| VPB | O | vector pull |  |
| VPA | O | valid program address |  |
| RW | O | read/write |  |
| RDY | I | bus ready |  |
| A0-A23 | O | Address bus |  |
| D0-D7 | I/O | data bus |  |
|  | 51 |  |  |
|  | 13 | Power and ground pins |  |

1. The MBV signal is generated when the bus is operating in 1MHz mode. Megahertz mode must be selected via a prefix instruction. It can be used to enable chip selects for a low speed bus.

The programmable chip select array is located at $00F000. These registers are write-only. Once setup further programming of the chip select array can be disabled by writing ‘E0’ to register 15.

On reset the chip selects default to respond to the following addresses:

CS0 = $00D0xx ; 256 bytes – 1MHz

CS1 = $00D1xx ; 256 bytes – 1MHz

CS2 = $00D2xx ; 256 bytes – 1MHz

CS3 = $00D3xx ; 256 bytes – 1MHz

CS4 = $008xxx ; 32k bytes – 8MHz

CS5 = $01xxxx ; 32k bytes – 8MHz

CS6 = not (CS0 or CS1 or CS2 or CS3 or CS4 or CS5) ; full speed

Chip selects are active low.

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Reg |  | Bits Covered | Reset Value |  |
| 0 | CS0 | 15 to 8 | D0 |  |
| 1 | CS0 | 23 to 16 | 00 |  |
| 2 | CS1 | 15 to 8 | D1 |  |
| 3 | CS1 | 23 to 16 | 00 |  |
| 4 | CS2 | 15 to 8 | D2 |  |
| 5 | CS2 | 23 to 16 | 00 |  |
| 6 | CS3 | 15 to 8 | D3 |  |
| 7 | CS3 | 23 to 16 | 00 |  |
| 8 | CS4 | 22 to 15 | 01 |  |
| 9 | CS4 | 23 | 00 |  |
| A | CS5 | 22 to 15 | 02 |  |
| B | CS5 | 23 | 00 |  |
| C | SS1 |  | 0F | speed select 1MHz (1 = 1MHz) |
| D | SS8 |  | 30 | speed select 8MHz (1 = 8MHz) |
| E | SS32 |  | 00 | full speed select |
| F | EN |  |  | Write E0 to this register to disable the register set |

Bit 0 of the speed select register corresponds to CS0

Bit 1 of the speed select register corresponds to CS1

etc.

Only one bit should be set in a speed select for a chip select.

Opcode Map – 8 bit mode W65C816 compatible

|  |  |
| --- | --- |
|  | = Enhanced instructions not found on the 65C02 |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | -0 | -1 | -2 | -3 | -4 | -5 | -6 | -7 | -8 | -9 | -A | -B | -C | -D | -E | -F |
| 0- | BRK | ORA (d,x) | cop | ORA d,s | TSB d,r | ORA d | ASL d | ORA [d] | PHP | OR #i8 | ASL acc | PHD | TSB abs | ORA abs | ASL abs | ORA AL |
| 1- | BPL disp | ORA (d),y | ORA (d) | ORA (d,s),y | TRB d,r | OR d,x | ASL d,x | ORA [d],y | CLC | OR abs,y | INA | TAS | TRB abs | ORA abs,x | ASL abs,x | ORA AL,x |
| 2- | JSR abs | AND (d,x) | JSL abs24 | AND d,s | BIT d | AND d | ROL d | AND [d] | PLP | AND #i8 | ROL acc | PLD | BIT abs | AND abs | ROL abs | ~ |
| 3- | BMI disp | AND (d),y | AND (d) | AND (d,s),y | BIT d,x | AND d,x | ROL d,x | AND [d],y | SEC | AND abs,y | DEA | TSA | BIT abs,x | AND abs,x | ROL abs,x | ~ |
| 4- | RTI | EOR (d,x) | WDM | EOR d,s | MVP | EOR d | LSR d | ~ | PHA | EOR #i8 | LSR acc | PHK | JMP abs | EOR abs | LSR abs | ~ |
| 5- | BVC disp | EOR (d),y | EOR (d) | EOR (d,s),y | MVN | EOR d,x | LSR d,x | ~ | CLI | EOR abs,y | PHY | TCD | JML abs24 | EOR abs,x | LSR abs,x | ~ |
| 6- | RTS | ADC (d,x) | PER | ADC d,s | STZ d | ADC d | ROR d | ~ | PLA | ADC #i8 | ROR acc | RTL | JMP (abs) | ADC abs | ROR abs | ~ |
| 7- | BVS disp | ADC (d),y | ADC (d) | ADC (d,s),y | STZ d,x | ADC d,x | ROR d,x | ~ | SEI | ADC abs,y | PLY | TDC | JMP (abs,x) | ADC abs,x | ROR abs,x | ~ |
| 8- | BRA disp | STA (d,x) | BRL disp | STA d,s | STY d | STA d | STX d | ~ | DEY | BIT # | TXA | PHB | STY abs | STA abs | STX abs | ~ |
| 9- | BCC disp | STA (d),y | STA (d) | STA (d,s),y | STY d,x | STA d,x | STX d,y | ~ | TYA | STA abs,y | TXS | TXY | STZ abs | STA abs,x | STZ abs,x | ~ |
| A- | LDY #i8 | LDA (d,x) | LDX #i8 | LDA d,s | LDY d | LDA d | LDX d | ~ | TAY | LDA #i8 | TAX | PLB | LDY abs | LDA abs | LDX abs | ~ |
| B- | BCS disp | LDA (d),y | LDA (d) | LDA (d,s),y | LDY d,x | LDA d,x | LDX d,y | ~ | CLV | LDA abs,y | TSX | TYX | LDY abs,x | LDA abs,x | LDX abs,x | ~ |
| C- | CPY #i8 | CMP (d,x) | REP # | CMP d,s | CPY d | CMP d | DEC d | ~ | INY | CMP #i8 | DEX | WAI | CPY abs | CMP abs | DEC abs | ~ |
| D- | BNE disp | CMP (d),y | CMP (d) | CMP (d,s),y | PEI | CMP d,x | DEC d,r | ~ | CLD | CMP abs,y | PHX | STP | JML (a) | CMP abs,x | DEC abs,x | ~ |
| E- | CPX #i8 | SBC(d,x) | SEP # | SBC d,s | CPX d | SUB d | INC d | ~ | INX | SBC #i8 | NOP | XBA | CPX abs | SBC abs | INC abs | ~ |
| F- | BEQ disp | SBC (d),y | SBC(r) | SBC (d,s),y | PEA | SUB d,x | INC d,r | ~ | SED | SBC abs,y | PLX | NAT | JSR (abs,x) | SBC abs,x | INC abs,x | ~ |