# Paging System

The paging system is capable of mapping the entire 64 bit address space. A multi-level system of page directories and subdirectories is used. In most cases the address space mapped will be less than a full 64 bit address space. The paging system accommodates this by using a smaller directory hierarchy. For instance, if an application is less than 1GB in size, a two level page system is used. If the application can fit within 2MB only a single level is required. The depth of the directory system is controllable on an application/process basis. The page memory management unit takes care of walking the page tables in hardware in order to find a translation. Translations are stored in a translation look-aside buffer (TLB) which is a translation cache, so that the page tables don’t have to be walked for every translation.

## Page Directories

Page directories are 4kB in size and contain 512, 8 byte entries.

### Page Directory Entries (PDE’s)

The page directory entries identify where in memory further subdirectories or translation pages are.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Address63..12 | ~8 | d1 | a1 | ~1 | t1 |

## Page Tables

Page tables are 8kB in size and contain 512, 16 byte entries.

### Page Table Entries (PTE’s)

Page table entries map the virtual address to a physical one.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Address63..12 | | | | | | | | | ~8 | | | | | d1 | | a1 | | e1 | | t1 |
| p15 | p14 | p13 | p12 | p11 | p10 | p9 | p8 | p7 | | p6 | p5 | p4 | p3 | | p2 | | p1 | | p0 | |

a1: accessed

d1: dirty

e1: protection enabled

t1: page present

px: privilege bucket

|  |  |  |  |
| --- | --- | --- | --- |
| c1 | r1 | x1 | w1 |

c1: cacheable

r1: readable

x1: executable

w1: writeable

## The Page Table Address Register

This register contains the base address of the page table in memory. The page table must be aligned on a 8kB boundary. The lowest three bits of the register identify the translation space.

|  |  |  |
| --- | --- | --- |
| Address63..13 | ~10 | TS3 |

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| TS3 | Translation Space | Address Processed | | | | | |
| 0 | 2MB |  | | | | | Address20..12 |
| 1 | 1GB |  | | | | Address29..12 | |
| 2 | 512 GB |  | | | Address38..12 | | |
| 3 | 256 TB |  | | Address47..12 | | | |
| 4 | 128 XB |  | Address56..12 | | | | |
| 5 | 2^64 | Address63..12 | | | | | |
| 6 | not used |  | | | | | |
| 7 | not used |  | | | | | |