Thor Guide

This document contains information pertaining to the Thor processor including the instruction set and formats and softcore interfacing.

2013

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1/1/2013

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# Overview

Thor is a powerful 64 bit superscalar processor that represents a generational refinement of processor architecture. The processor contains 256, 64 bit general purpose integer registers. Thor uses variable length instructions varying between one and eight bytes in length and handles 8, 16, 32, and 64 bit data within a 64 bit address space.

## Design Objectives

This processor is somewhat pedantic in nature and targeted towards high performance operation as a general purpose processor. Following are some of the criteria that were used on which to base the design.

|  |
| --- |
| * Designed for Superscalar operation - the ability to execute more than one instruction at a time. To achieve high performance it is generally accepted that a processor must be able to execute more than a single instruction in any given clock cycle. |
| * Simplicity - architectural simplicity leads to a design that is easy to implement resulting in reliability and assured correctness along with easy implementation of supporting tools such as compilers. Simplicity also makes it easier to obtain high performance and results in lower overall cost. |
| * Extensibility - the design must be extensible so that features not present in the first release can easily be added at a later date. |
| * Low Cost |

This design meets the above objectives in the following ways. The instruction set has been designed to minimize the interactions between instructions, allowing instructions to be executed as independent units for superscalar operation. There are a sufficient number of registers to allow the compiler to schedule parallel processing of code. A reasonably large general purpose register set is available making the design reasonably compatible with many existing compilers and assemblers. Where needed, additional specialized instructions have been added to the processor to support a sophisticated operating system and interrupt management.

# Programming Model

## General Registers

There are 256 general purpose registers. General purpose registers are 64 bits wide.

Register #0 is always zero.

**Branch Registers**

The processor contains 16 branch registers (BR0-BR15). Several of the branch registers are reserved for predefined purposes. A branch register is used in the formation and storage of code addresses.

|  |  |  |
| --- | --- | --- |
| Reg # |  | Usage |
| 0 | Always Zero | Absolute address formation |
| 1 |  | Subroutine return address |
| 2 |  | This register is available for general use. |
| 3 |  | This register is available for general use. |
| 4 |  | This register is available for general use. |
| 5 |  | This register is available for general use. |
| 6 |  | This register is available for general use. |
| 7 |  | This register is available for general use. |
| 8 |  | This register is available for general use. |
| 9 |  |  |
| 10 |  |  |
| 11 | Catch Link Register | Used by the compiler to link to try/catch handlers. |
| 12 | Exception Table Pointer | This register points to the exception table in memory. |
| 13 | Exceptioned PC | This register is set when an exception occurs |
| 14 | Interrupted PC | This register is automatically set during a hardware interrupt |
| 15 | Program Counter | Relative address formation. |
|  |  |  |

Branch registers may be used to point to a block of code from which the JSR instruction can index into with its 24 bit offset. For instance a branch register may contain a pointer to a class method jump list; the JSR instruction can then index into this list in order to invoke a method.

The program counter branch register is read-only. The program counter cannot be modified by moving a value to this register.

## Predicates

The processor features predicated execution of all instructions. Whether or not an instruction is executed depends on the contents of a predicate register and the predicate condition specified in the predicate byte. There are 16 predicate registers each of which hold three flags. These flags are set as the result of a compare operation. The flags represent equality (eq) signed less than (lt) and unsigned less than (ltu).

|  |  |  |  |
| --- | --- | --- | --- |
| 3 | 2 | 1 | 0 |
| ~ | ltu | lt | eq |

All instructions are executed conditionally determined by the value of a predicate register. The special predicate 00 executes the break vector.

### Predicate Conditions

|  |  |  |  |
| --- | --- | --- | --- |
| Cond. |  | Test |  |
| 0 | PF | 0 | Always false – Instructions predicated with condition zero never execute regardless of the predicate register contents. This is used for extended immediate values as well. |
| 1 | PT | 1 | Always True – The instruction predicated with an always true condition always executes regardless of the predicate register contents. |
| 2 | PEQ | eq | Equal – instruction executes if the predicate register equal flag is set |
| 3 | PNE | !eq | Not Equal – instruction executes if the predicate register equal flag is clear |
| 4 | PLE | lt|eq | Less or Equal – predicate less or equal flag is set |
| 5 | PGT | !(lt|eq) | greater than |
| 6 | PGE | !lt | greater or equal |
| 7 | PLT | lt | less than |
| 8 | PLEU | ltu|eq | unsigned less or equal |
| 9 | PGTU | !(ltu|eq) | unsigned greater than |
| 10 | PGEU  POR | !ltu | unsigned greater or equal  Ordered for floating point |
| 11 | PLTU  PUN | ltu | unsigned less than  Unordered for floating point |
| 12 |  |  |  |
| 13 | PSIG | signal | execute if external signal is true |
| 14 |  |  |  |
| 15 |  |  |  |

### Compiler Usage

The compiler uses predicate register #15 to conditionally move TRUE / FALSE values to a register when evaluating a logical operation.

Predicate registers beginning with P0 and incrementing are applied for use as the control flow nesting level increases. The compiler does not support control flow nesting more than 14 levels in a single subroutine. Predicate registers beginning with P14 and decrementing are used in the evaluation of the hook operator. Care must be taken such that the number of predicate registers in use does not exceed the number available.

|  |  |  |
| --- | --- | --- |
| Pred. | Usage |  |
| P0 | control flow level 0 |  |
| P1 | control flow nesting level 1 |  |
| P2 | control flow nesting level 2 |  |
| … |  |  |
| Pn | control flow nesting level n (n not to exceed 14) |  |
| … |  |  |
| P12 | third hook operator in an expression |  |
| P13 | second hook operator in an expression |  |
| P14 | first hook operator in an expression |  |
| P15 | conditionally moves TRUE/FALSE for logical expressions |  |

## Status Register (SR)

This register contains bits that control the overall operation of the processor or reflect the processor’s state. Bits are included for interrupt masking, and system / application mode indicator. This register is split into two halves with both halves having the same format. The lower half of the register is what determines how the processor works. The upper half of the register maintains a backup copy of the lower half for interrupt processing. There are instructions provided for manipulating the interrupt mask.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 31..16 | 15 | 14 | 13 | 12 | 11..10 | 9..0 |
| same format as 15..0 | Interrupt Mask | Reserved | Kernel / Application Mode Indicator | Float Except. Enable |  | reserved |
|  | IM | ~ | S | FXE |  | ~ |

 The Kernel / Application Mode indicator is read-only.

IM = interrupt mask

Maskable interrupts are disabled when this bit is set.

# Segmentation

The processor contains sixteen segment registers. The upper nibble of an address (bits 60 to 63) identifies which segment register to use during address formation for data addresses. For code addresses segment register #15 is always used.

* If segmentation is not desired then segmentation can effectively be ignored by setting all the segment registers to zero. The processor can also be built without segmentation by commenting out the ‘SEGMENTATION’ definition.

## Software Support

Segment registers may only be transferred to or from one of the general purpose registers. The mtspr and mfspr instructions can be used to perform the move.

## Address Formation:

Non-segmented address bits 0 to 11 pass through the segmentation module unchanged. Address bits 59 to 12 are added to the contents of the segment register to form the final segmented address. Note that there is no shift associated with the segment addition. Future implementations of the processor may include additional low order address bits in the segment register in order to allow a finer grain for memory page / paragraph size.

|  |  |
| --- | --- |
| Address[59:12] | Address[11:0] |
| + | + |
| Segment register value[63:12] | 00012 |
| = | |
| Segmented address[63:0] | |

## Selecting a segment register

The upper nybble of an address (bits 60 to 63) identifies which segment register to use. This selection applies to data addresses only. Code addresses always use segment register #15 – the code segment.

## Non-Segmented Code Area

The address range defined as 64’hFxxxxxxxxxxxxxxx (the top nibble is ‘F’) is a non-segmented code area. This area allows the operating system to work without paying attention to the code segment. Interrupt and exception vectors should vector into the non-segmented code area. The only way to change the code segment is by transferring to the operating system via a sys call instruction.

## Changing the Code Segment

The only way to change the code segment is by transferring to the operating system via a sys call instruction. The operating system, while operating in the non-segmented code area, can alter the code segment without causing a transfer of control. The operating system establishes the code segment for a task while running in the non-segmented code area.

## Segment Usage Conventions

Segment register #15 is the code segment (CS) register. All program counter addresses are formed with the code segment register unless the upper nibble of the address is ‘F’ in which case the code segment is ignored.

Segment register #14 is the stack segment (SS) register by convention. Segment register #1 is the data segment (DS) by convention.

Segment register #13 is the volatile data segment (VDS). Addresses formed using this segment register bypass the data cache.

## Power-up State

On reset the value in the segment registers are undefined. Note that the processor begins executing instructions out of the non-segmented code area as the reset address is 64’hFFFFFFFFFFFFFFF0. One of the first tasks of the boot program would be to initialize the segment registers to known values. The segment register must be setup to perform data accesses properly.

#### Segment Registers

|  |  |  |  |
| --- | --- | --- | --- |
| Num |  | Long name | Comment |
| 0 | NS | NULL segment | by convention contains zero |
| 1 | DS | data segment | by convention |
| 2 | TS | thread storage | by convention |
| 3 | BS | BSS segment | by convention |
| 4 | RS | read only segment | by convention |
| 5 | ES | extra segment | by convention |
| … |  |  |  |
| 13 | VDS | volatile data segment | bypasses the cache |
| 14 | SS | Stack segment | by convention |
| 15 | CS | Code segment | always used for code addressing |

# TLB

The processor uses a 64 entry TLB (translation look-aside buffer) in order to support virtual memory. The TLB supports variable page sizes from 4kB to 1MB. The TLB is organized as an eight-way eight-set cache.

The TLB is updated by first placing values into the TLB holding registers using the TLB instruction, then issuing a TLB write command using the TLB command instruction.

Address translations will not take place until the TLB is enabled. An enable TLB command must be issued using the TLB command instruction.

TLB Entries:

C2..0

G

D

V

ASID7...0

Virtual Page51...0

Physical Page51...0

G = Global

The global bit marks the TLB entry as a global address translation where the ASID field is not used to match addresses.

ASID = address space identifier

The ASID field in the TLB entry must match the processor’s current ASID value in order for the translation to be considered valid, unless the G bit is set. If the G bit is set in the TLB entry, then the ASID field is ignored during the address comparison.

C = cachability bits

If the cachability bits are set to 001b then the page is uncached, otherwise the page is cached.

D = dirty bit

The dirty bit is set by hardware when a write occurs to the virtual memory page identified by the TLB entry.

V = valid bit

This bit must be set in order for the address translation to be considered valid. The entire TLB may be invalidated using the invalidate all command.

## TLB Registers

### TLBWired (#0h)

This register limits random updates to the TLB to a subset of the available number of ways. TLB ways below the value specified in the Wired register will not be updated randomly.

### TLBIndex (#1h)

This register contains the entry number of the TLB entry to be read from or written to.

### TLBRandom (#2h)

This register contains a random three bit value used to update a random TLB entry during a TLB write operation.

### TLBPageSize (#3h)

The TLBPageSize register controls which address bits are significant during a TLB lookup.

|  |  |  |
| --- | --- | --- |
| N | Page Size |  |
| 0 | 4KiB |  |
| 1 | 16kiB |  |
| 2 | 64kiB |  |
| 3 | 256kiB |  |
| 4 | 1MiB |  |
|  |  |  |
|  |  |  |

### TLBPhysPage (#5h)

The TLBPhysPage register is a holding register that contains the page number for an associated virtual address. This register is transferred to or from the TLB by TLB instructions.

|  |
| --- |
| 63 0 |
| Physical Page Number |

### 

### TLBVirtPage (#4h)

The TLBVirtPage register is a holding register that contains the page number for an associated physical address. This register is transferred to or from the TLB by TLB instructions.

|  |
| --- |
| 63 0 |
| Virtual Page Number |

### TLBASID (#7h)

The TLBASID register is a holding register that contains the address space identifier (ASID) , valid, dirty, global, and cachability bits associated with a TLB entry. This register is transferred to or from the TLB by TLB instructions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 63 16 | 15 8 | 6 4 | 2 | 1 | 0 |
| ----- | ASID | C | G | D | V |

# Vectors

The processor vectors to $FFFFFFFFFFFFFFF0 on a reset. All other vectoring is done through a vector table. The vector table allows for 256 entries. The vector table base address is established by branch address register BR12. During an external IRQ the processor looks at a vector number bus to determine the vector to use for the IRQ. This vector number may be hard-coded in which case all IRQ’s will be vectored to the same location. The address vectored to is the sum of BR12 and an offset supplied in the instruction multiplied by sixteen. The contents of BR12 are undefined at reset; this register must be loaded before interrupts can be processed.

### Vector table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Vector Number | Usage / Description | |  |  |
| 0 | BREAK instruction vector | |  |  |
| 1 | SLEEP vector (branch to self) | |  |  |
| 2 | Task reschedule interrupt | |  |  |
| … |  | |  |  |
| 192 | Spurious interrupt | |  |  |
| 193 | IRQ level 1 | 1000 Hz interrupt |  |  |
| 194 | IRQ level 2 | 100 Hz interrupt |  |  |
| … | Other IRQ levels |  |  |  |
| 207 | IRQ level 15 | keyboard interrupt |  |  |
| … |  | |  |  |
| 248 | DTLBMiss | |  |  |
| 249 | ITLB Miss | |  |  |
| 250 | Unimplemented instruction | |  |  |
| 251 | Bus error – data load / store | |  |  |
| 252 | Bus error – instruction fetch | |  |  |
| 253 | reserved | |  |  |
| 254 | NMI interrupt vector | |  |  |
| 255 | * reserved | |  |  |

# Hardware Ports

Thor uses a WISHBONE bus to communicate with the outside world.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | I/O | Width | WB |  |  |
| rst\_i | I | 1 | WB | reset signal |  |
| clk\_i | I | 1 | WB | clock |  |
| km | O | 1 |  | kernel mode indicator |  |
| nmi\_i | I | 1 |  | non-maskable interrupt input |  |
| irq\_i | I | 1 |  | maskable interrupt input |  |
| vec\_i | I | 8 |  | interrupt vector |  |
| bte\_o | O | 2 | WB | burst type extension |  |
| cti\_o | O | 3 | WB | cycle type indicator |  |
| bl\_o | O | 5 |  | burst length output |  |
| lock\_o | O | 1 | WB | bus lock |  |
| cyc\_o | O | 1 | WB | cycle is valid |  |
| stb\_o | O | 1 | WB | data transfer is taking place |  |
| ack\_i | I | 1 | WB | data transfer acknowledge |  |
| err\_i | I | 1 | WB | bus error occurred input |  |
| we\_o | O | 1 | WB | write enable |  |
| sel\_o | O | 8 | WB | byte lane selects |  |
| adr\_o | O | 64 | WB | address output |  |
| dat\_i | I | 64 | WB | data input bus |  |
| dat\_o | O | 64 | WB | data output bus |  |
|  |  |  |  |  |  |

WB = see the WISHBONE spec rev B3

Notes:

Stores issue only from the head of the instruction queue when it is known that no exceptions have taken place.

## Instruction Formats

Instructions vary in length from one to eight bytes. There are only a couple of single byte instructions consisting of only a predicate. Some of the more common formats are shown below.

All instruction sequences begin with a predicate byte that determines the conditions under which the instruction executes. With the exception of special predicate values, the next field in the instruction is always the opcode byte. All opcodes may be preceded by an extended constant value.

### RR - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | Opcode8 | Pn4 | Pc4 |

### RI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | Opcode8 | Pn4 | Pc4 |

### CMP Register-Register Compare

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 12 | 11 8 | 7 0 | |
| Rb | Ra | Opc | Pt | Predicate | |
| Rb8 | Ra8 | 14 | Pt4 | Pn4 | Pc4 |

### CMPI Register-Immediate Compare

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 24 | | 23 16 | | 15 12 | | 11 8 | | 7 0 | |
| Immed | | Ra | | Opc | | Pt | | Predicate | |
| Immed8 | | Ra8 | | 24 | | Pt4 | | Pn4 | Pc4 |
| TST - Register Test Compare | | | | | | | |  | |  | CTRL- Control | | |
| 23 16 | 15 12 | | 11 8 | | 7 0 | | |  | |  | 15 8 | 7 0 | |
| Ra | Opc | | Pt | | Predicate | | |  | |  | Opcode | Predicate | |
| Ra8 | 04 | | Pt4 | | Pn4 | | Pc4 |  | |  | Opcode8 | Pn4 | Pc4 |

|  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| BR - Relative Branch | | | | |  |  | | BRK/NOP | |
| 23 16 | 15 8 | | 7 0 | |  |  | | 7 0 | |
| Disp. | Opc | Disp. | Predicate | |  |  | | Predicate | |
| Disp7..0 | 34 | D11..8 | Pn4 | Pc4 |  | |  | 0/14 | 04 |

### JSR - Jump To Subroutine

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Offset | Br | Brt | Opcode | Predicate | |
| Offset23..0 | Br4 | Brt4 | Opcode8 | Pn4 | Pc4 |

# Instruction Set

### 2ADDU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 56h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 2 + Rb

#### Description:

Multiply Ra by two and add Rb and place the sum in the target register. This instruction will never cause an overflow exception.

### 2ADDUI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immed | Rb | Ra | Opcode | Predicate | |
| Immed8 | Rb8 | Ra8 | 6Bh8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 2 + immediate

#### Description:

Multiply Ra by two and add immediate and place the sum in the target register. This instruction will never cause an overflow exception.

### 4ADDU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 57h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 4 + Rb

#### Description:

Multiply Ra by four and add Rb and place the sum in the target register. This instruction will never cause an exception.

### 4ADDUI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immed | Rb | Ra | Opcode | Predicate | |
| Immed8 | Rb8 | Ra8 | 6Ch8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 4 + immediate

#### Description:

Multiply Ra by four and add immediate and place the sum in the target register. This instruction will never cause an exception.

### 8ADDU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 64h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 8 + Rb

#### Description:

Multiply Ra by eight and add Rb and place the sum in the target register. This instruction will never cause an exception.

### 8ADDUI - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immed | Rb | Ra | Opcode | Predicate | |
| Immed8 | Rb8 | Ra8 | 6Dh8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 8 + immediate

#### Description:

Multiply Ra by eight and add immediate and place the sum in the target register. This instruction will never cause an exception.

### 16ADDU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 65h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 16 + Rb

#### Description:

Multiply Ra by sixteen and add Rb and place the sum in the target register. This instruction will never cause an exception.

### 16ADDUI - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immed | Rb | Ra | Opcode | Predicate | |
| Immed8 | Rb8 | Ra8 | 6Eh8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* 16 + immediate

#### Description:

Multiply Ra by sixteen and add immediate and place the sum in the target register. This instruction will never cause an exception.

### ADD - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 40h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra + Rb

#### Description:

Add two registers and place the sum in the target register. This instruction may cause an overflow exception.

### ADDI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 48h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra + immediate

#### Description:

Add a register and immediate value and place the sum in the target register. This instruction may cause an overflow exception.

### ADDU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 44h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra + Rb

#### Description:

This instruction will never cause any exceptions.

### ADDUI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 4Ch8 | Pn4 | Pc4 |

### AND - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 50h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra & Rb

#### Description:

Locgially and’s two registers and places the result in a target register.

### ANDI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 53h8 | Pn4 | Pc4 |

### BCDADD - Register-Register

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Opcode | Rt | Rb | Ra | Opcode | Predicate | |
| 00h8 | Rt8 | Rb8 | Ra8 | F5h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra + Rb

#### Description:

Adds two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is an eight bit BCD number.

### BCDMUL - Register-Register

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Opcode | Rt | Rb | Ra | Opcode | Predicate | |
| 02h8 | Rt8 | Rb8 | Ra8 | F5h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra \* Rb

#### Description:

Multiplies two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is a 16 bit BCD value.

### BCDSUB - Register-Register

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Opcode | Rt | Rb | Ra | Opcode | Predicate | |
| 01h8 | Rt8 | Rb8 | Ra8 | F5h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra - Rb

#### Description:

Subtracts two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is an eight bit BCD number.

### BFCHG – Bitfield Change

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 34 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Inverts the bitfield in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

### BFCLR – Bitfield Clear

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 24 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Sets the bits to zero of the bitfield in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

### BFEXT – Bitfield Extract

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 54 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Extracts a bitfield from register Ra located between the mask begin (mb) and mask end (me) bits and places the sign extended result into the target register.

### BFEXTU – Bitfield Extract Unsigned

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 44 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Extracts a bitfield from register Ra located between the mask begin (mb) and mask end (me) bits and places the zero extended result into the target register.

### BFINS – Bitfield Insert

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 04 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Inserts a bitfield into the target register located between the mask begin (mb) and mask end (me) bits from the low order bits of Ra.

### BFSET – Bitfield Set

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 44 43 38 | | 37 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Func | me | mb | Rt | Ra | Opcode | Predicate | |
| 14 | me6 | mb6 | Rt8 | Ra8 | AAh8 | Pn4 | Pc4 |

#### Description:

Sets the bits to one of the bitfield in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

### BR - Relative Branch

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 16 | 15 8 | | 7 0 | |
| Disp. | Op | Disp | Predicate | |
| Disp7..0 | 3h4 | D11..8 | Pn4 | Pc4 |

#### Operation:

pc <= pc + displacement

#### Description:

A branch is made relative to the address of the branch instruction.

* The displacement field cannot be extended with an immediate constant prefix. Branches are executed immediately in the ifetch stage of the processor before it is known if there is a prefix present.

### BRK –Break

|  |  |
| --- | --- |
| 7 0 | |
| Predicate | |
| 04 | 04 |

#### Operation:

<none>

#### Description:

This instruction contains only a predicate byte. The Break exception is executed.

### BSR - Branch To Subroutine

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Offset | Br | Brt | Opcode | Predicate | |
| Offset23..0 | 154 | Brt4 | A2h8 | Pn4 | Pc4 |

#### Description:

This is an alternate mnemonic for the JSR instruction. A jump is made to the sum of the sign extended offset supplied in the offset field of the instruction and the specified branch register Br.

The subroutine return address is stored in a branch register specified in the Brt field of the instruction.

### CAS – Compare And Swap

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 55 48 | 47 40 | 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Rc | Rb | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Rc8 | Rb8 | Ra8 | 97h8 | Pn4 | Pc4 |

#### Operation:

Rt = memory [Ra + offset]

if memory[Ra+offset] = Rb

memory[Ra + offset] = Rc

#### Description:

If the contents of the addressed memory cell is equal to the contents of Rb then a sixty-four bit value is stored to memory from the source register Rc. The original contents of the memory cell are loaded into register Rt. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned. If the operation was successful then Rt and Rb will be the same value. The compare and swap operation is an atomic operation; the bus is locked during the load and potential store operation. This operation assumes that the addressed memory location is part of the volatile region of memory and bypasses the data cache.

#### Assembler:

CAS Rt,Rb,Rc,offset[Ra]

### CLI – Clear Interrupt Mask

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| Opcode | Predicate | |
| FAh8 | Pn4 | Pc4 |

#### Operation:

im = 0

#### Description:

This instruction is used to enable interrupts.

### CMP Register-Register Compare

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 12 | 11 8 | 7 0 | |
| Rb | Ra | Opc | Pt | Predicate | |
| Rb8 | Ra8 | 14 | Pt4 | Pn4 | Pc4 |

### CMPI Register-Immediate Compare

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 12 | 11 8 | 7 0 | |
| Immed | Ra | Opc | Pt | Predicate | |
| Immed8 | Ra8 | 24 | Pt4 | Pn4 | Pc4 |

#### Operation:

if signed Ra < signed immediate

P.lt = true

else

P.lt = false

if unsigned Ra < unsigned immediate

P.ltu = true

else

P.ltu = false

if Ra = immediate

P.eq = true

else

P.eq = false

#### Description:

The register immediate compare instruction compares a register to an immediate value and sets the flags in the target predict register as a result.

### EOR - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 52h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra ^ Rb

#### Description:

Logically exclusive or register with register and place result in target register.

### EORI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 55h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra ^ immediate

### IMM64,IMM56,IMM48,IMM40,IMM32,IMM24,IMM16

### Immediate Extensions

The immediate extension predicates are used to extend the immediate constant of the following instruction. The extensions may add from one to seven bytes more to the constant. Most, but not all instructions can accept a predicated immediate.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Immediate | | | | | | | Predicate | |
| Immediate63..8 | | | | | | | 84 | 04 |
| Immediate55..8 | | | | | | 74 | 04 |
| Immediate47..8 | | | | | 64 | 04 |
| Immediate39..8 | | | | 54 | 04 |
| Immediate31..8 | | | 44 | 04 |
| Immediate23..8 | | 34 | 04 |
| Immediate15..8 | 24 | 04 |

### INT –Interrupt

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Disp. | Br | Brt | Opcode | Predicate | |
| Offset7..0 | Ch4 | Eh4 | A6h8 | Pn4 | Pc4 |

#### Description:

This instruction calls a system function located as the sum of the zero extended offset times 16 plus branch register 12. The return address is stored in the IPC register (Branch register #14).

The offset field of this instruction cannot be extended.

Note that this instruction is automatically invoked for hardware interrupt processing. This instruction would not normally be used by software and is not supported by the assembler. The return address stored is the address of the interrupt instruction, not the address of the next instruction. To call system routines use the SYS instruction.

### JMP - Jump To Address

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Offset | Br | Brt | Opcode | Predicate | |
| Offset23..0 | Br4 | 04 | A2h8 | Pn4 | Pc4 |

#### Operation:

pc = Br[n] + offset

#### Description:

This is an alternate mnemonic for the JSR instruction.

The JMP instruction may be used with an immediate predicate constant in order to extend the address range of the jump. A jump is made to the sum of the zero extended offset supplied in the offset field of the instruction and the specified branch register Br.

### JSR - Jump To Subroutine Instruction

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Offset | Br | Brt | Opcode | Predicate | |
| Offset23..0 | Br4 | Brt4 | A2h8 | Pn4 | Pc4 |

#### Operation:

Br[t] = pc

pc = Br[n] + offset

#### Description:

The JSR instruction may be used with an immediate predicate constant in order to extend the address range of the jump. A jump is made to the sum of the zero extended offset supplied in the offset field of the instruction and the specified branch register Br.

The subroutine return address is stored in a branch register specified in the Brt field of the instruction. Typically branch register #1 is used.

An immediate constant prefix applied to this instruction overrides offset bits 8 to 23 and acts like an eight bit immediate constant extension used by other instructions.

### LB – Load Byte

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 80h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

An eight bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

### LBX – Load Byte Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B0h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

An eight bit value is loaded from memory and placed in the target register. The memory address is the sum of register Ra and register Rb.

### LBU – Load Byte Unsigned

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 81h8 | Pn4 | Pc4 |

#### Operation:

Rt = zero extend (mem[Ra+offset])

#### Description:

An eight bit value is loaded from memory and zero extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

### LBUX – Load Byte Unsigned Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B1h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

An eight bit value is loaded from memory zero extended and placed in the target register. The memory address is the sum of register Ra and register Rb.

### LC – Load Character

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 82h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

A sixteen bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be character aligned.

### LCX – Load Character Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B2h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

A sixteen bit value is loaded from memory, sign extended and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be character aligned.

### LCU – Load Character Unsigned

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 83h8 | Pn4 | Pc4 |

#### Operation:

Rt = zero extend (mem[Ra+offset])

#### Description:

A sixteen bit value is loaded from memory and zero extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be character aligned.

### LCUX – Load Character Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B3h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

A sixteen bit value is loaded from memory, zero extended and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be character aligned.

### LDI - Load-Immediate

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Opcode | Predicate | |
| Immediate7..0 | Rt8 | 6Fh8 | Pn4 | Pc4 |

#### Operation:

Rt = immediate

#### Description:

This instruction loads a sign extended immediate constant into a register. The immediate constant may be extended by using an immediate prefix instruction.

### LDIS - Load-Immediate Special

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Opcode | Predicate | |
| Immediate7..0 | Spr8 | 9Dh8 | Pn4 | Pc4 |

#### Operation:

Spr = immediate

#### Description:

This instruction loads a sign extended immediate constant into a special purpose register. The immediate constant may be extended by using an immediate prefix instruction. Typical usage is to initialize a branch register with a target address.

### LDIT8 - Load-Immediate Top Eight

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Opcode | Predicate | |
| Immediate7..0 | Rt8 | 9Ch8 | Pn4 | Pc4 |

#### Operation:

Rt[63:56] = immediate8

#### Description:

This instruction loads an immediate constant into the top eight bits of a register the lower bits of the register are unaffected. The primary purpose of this instruction is to set the segment used in address formation.

### LEA – Load Effective Address

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 4Ch8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra+offset

#### Description:

This is an alternate mnemonic for the ADDUI instruction. The memory address is placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

### LH – Load Half-Word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 84h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

A thirty-two bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be half-word aligned.

### LHX – Load Half-word Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B4h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

A thirty-two bit value is loaded from memory, sign extended and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be half-word aligned.

### LHU – Load Half-word Unsigned

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 85h8 | Pn4 | Pc4 |

#### Operation:

Rt = zero extend (mem[Ra+offset])

#### Description:

A thirty-two bit value is loaded from memory and zero extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be half-word aligned.

### LHUX – Load Half-word Unsigned Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B5h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+Rb]

#### Description:

A thirty-two bit value is loaded from memory, zero extended and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be half-word aligned.

### LOOP – Loop Branch

|  |  |  |  |
| --- | --- | --- | --- |
| 23 16 | 15 8 | 7 0 | |
| Disp. | Opcode | Predicate | |
| Disp7..0 | A4h8 | Pn4 | Pc4 |

#### Operation:

If lc <> 0

pc <= pc + displacement

lc = lc - 1

#### Description:

A branch is made relative to the current value of the program counter if the loop count register is non-zero. The loop count register is decremented by this instruction. The predicate condition must also be met.

### LVB – Load Volatile Byte

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | D0h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

An eight bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

### LVC – Load Volatile Character

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | D1h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

A sixteen bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

### LVH – Load Volatile Half-word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | D2h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

A thirty-two bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

### LVW – Load Volatile Word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | D3h8 | Pn4 | Pc4 |

#### Operation:

Rt = sign extend (mem[Ra+offset])

#### Description:

A sixty-four bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

### LW – Load Word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 86h8 | Pn4 | Pc4 |

#### Operation:

Rt = mem[Ra+offset]

#### Description:

A sixty-four bit value is loaded from memory and placed in the target register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

### LWS – Load Word Special

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 8Eh8 | Pn4 | Pc4 |

#### Operation:

Spr = mem[Ra+offset]

#### Description:

A sixty-four bit value is loaded from memory and placed in the special purpose register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

### LWX – Load Word Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | B6h8 | Pn4 | Pc4 |

#### Operation:

#### Rt = mem[Ra+Rb]

#### Description:

A sixty-four bit value is loaded from memory and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be word aligned.

### MEMDB – Memory Data Barrier

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| Opcode | Predicate | |
| F9h8 | Pn4 | Pc4 |

#### Operation:

im = 1

#### Description:

All memory accesses before the MEMDB command are completed before any memory accesses after the data barrier are started. Note that this instruction has an effect even if the predicate is false; this does not affect the correct operation of the program, only performance is affected.

### MEMSB – Memory Synchronization Barrier

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| Opcode | Predicate | |
| F8h8 | Pn4 | Pc4 |

#### Operation:

im = 1

#### Description:

All memory accesses before the MEMSB command are completed before execution continues. Note that this instruction has an effect even if the predicate is false; this does not affect the correct operation of the program, only performance is affected.

### MFSPR – Special Register-Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Spr | Opcode | Predicate | |
| Rt8 | Spr8 | A8h8 | Pn4 | Pc4 |

#### Operation:

Rt = Spr[n]

#### Special Purpose Registers

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Reg # | R/W |  |  |  |
| 0 | R | MID | Machine ID |  |
| 1 | R | FEAT | Features |  |
| 2 | R | TICK | Tick count |  |
| 3 | RW | LC | Loop Counter |  |
| 4 | RW | PREGS | Predicate register array |  |
| 6 | RW | ASID | address space identifier |  |
| 16-31 | RW | BREGS | Branch register array (BR0 to BR15) |  |
| 32-47 | RW | SREGS | Segment register array (SEG0-SEG15) |  |

### MOV - Register-Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Ra | Opcode | Predicate | |
| Rt8 | Ra8 | A78 | Pn4 | Pc4 |

#### Operation:

Rt = Ra

#### Description:

This instruction moves one general purpose register to another.

### MOVS – Move Special Register- Special Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Sprt | Spra | Opcode | Predicate | |
| Sprt8 | Spr8 | AB8 | Pn4 | Pc4 |

#### Operation:

Sprt = Spra

#### Description:

This instruction moves one special purpose register to another.

### MTSPR –Register-Special Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Spr | Ra | Opcode | Predicate | |
| Spr8 | Ra8 | A9h8 | Pn4 | Pc4 |

#### Operation:

Spr[n] = Ra

### MUX – Multiplex

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rc | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rc8 | Rb8 | Ra8 | 72h8 | Pn4 | Pc4 |

#### Operation:

For n = 0 to 63

If Ra[n] is set then

Rt[n] = Rb[n]

else

Rt[n] = Rc[n]

#### Description:

If a bit in Ra is set then the bit of the target register is set to the corresponding bit in Rb, otherwise the bit in the target register is set to the corresponding bit in Rc.

### NEG - Negate Register

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Ra | Opcode | Predicate | |
| Rt8 | Ra8 | 70h8 | Pn4 | Pc4 |

#### Operation:

Rt = - Ra

#### Description:

This instruction negates a register and places the result in a target register.

### NOP – No Operation

|  |  |
| --- | --- |
| 7 0 | |
| Predicate | |
| 14 | 04 |

#### Operation:

<none>

#### Description:

This instruction contains only a predicate byte. This is a single byte no-operation code. It can be used to align code addresses or as a fill byte.

### OR - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 51h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra | Rb

#### Description:

Logically inclusively or two registers and place the result in the target register.

### ORI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 54h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra | imm

### RTE – Return From Exception Routine

|  |  |  |
| --- | --- | --- |
| Opcode | Predicate | |
| F3h8 | Pn4 | Pc4 |

#### Operation**:**

pc = Br[13]

Flags = FlagsBackup

#### **Description**:

The program counter is loaded with the value contained in branch register #13 which is the EPC register.

### RTI – Return From Interrupt Routine

|  |  |  |
| --- | --- | --- |
| Opcode | Predicate | |
| F4h8 | Pn4 | Pc4 |

#### Operation:

pc = Br[14]

Flags = FlagsBackup

Flags.im = 0

#### **Description**:

The program counter is loaded with the value contained in branch register #14 which is the IPC register.

### RTS – Return From Subroutine

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Br | Im | Opcode | Predicate | |
| Br4 | Im4 | A3h8 | Pn4 | Pc4 |

#### Operation:

pc = Br[N]

#### **Description**:

The program counter is loaded with the value contained in the specified branch register plus a zero extended four bit immediate constant. The constant may not be extended. This allows the return instruction to return a few bytes past the usual return address. This is used to allow static parameters to be passed to the subroutine in inline code.

Note that the JMP instruction may also be used to return from a subroutine. Similarly this instruction may also be used to perform a jump to one of the first sixteen addresses relative to a branch register.

#### Short Form:

|  |  |
| --- | --- |
| Predicate | |
| 14 | 14 |

#### Operation:

pc = Br[1]

#### **Description**:

The program counter is loaded with the value contained in branch register #1.

### SB – Store Byte

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 90h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Rb[7..0]

#### Description:

An eight bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended offset and register Ra.

### SBX – Store Byte Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | C0h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+Rb] = Rb

#### Description:

An eight bit value is stored to memory from the source register Rb. The memory address is the sum of register Ra and Rb.

### SC – Store Character

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 91h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Rb[15..0]

#### Description:

A sixteen bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended offset and register Ra. The memory address must be character aligned.

### SCX – Store Character Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | C1h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+Rb] = Rb

#### Description:

A sixteen bit value is stored to memory from the source register Rb. The memory address is the sum of register Ra and Rb. The memory address must be character aligned.

### SEI – Set Interrupt Mask

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| Opcode | Predicate | |
| FBh8 | Pn4 | Pc4 |

#### Operation:

im = 1

#### Description:

The interrupt mask is set, disabling maskable interrupts.

### SH – Store Half-word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 92h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Rb[31..0]

#### Description:

A thirty-two bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended offset and register Ra. The memory address must be half-word aligned.

### SHX – Store Half-word Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | C2h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+Rb] = Rb

#### Description:

A thirty-two bit value is stored to memory from the source register Rb. The memory address is the sum of register Ra and Rb. The memory address must be half-word aligned.

### STI – Store Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Imm | Ra | Opcode | Predicate | |
| Offset7..0 | Imm8 | Ra8 | 96h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Imm[7..0]

#### Description:

A eight bit value is zero extended to sixty-four bits and stored to memory. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

### STSB – Store String Byte

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Rb | Ra | Opcode | Predicate | |
| Rb8 | Ra8 | 98h8 | Pn4 | Pc4 |

#### Operation:

temp = 0

while LC <> 0

mem[Ra+temp] = Rb[7:0]

temp =temp + 1

LC = LC – 1

#### Description:

This instruction stores a byte to consecutive memory locations beginning at the address in Ra until the loop counter reaches zero. This instruction is interruptible.

### STSW – Store String Word

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 24 | 23 16 | 15 8 | 7 0 | |
| Rb | Ra | Opcode | Predicate | |
| Rb8 | Ra8 | 9Ah8 | Pn4 | Pc4 |

#### Operation:

temp = 0

while LC <> 0

mem[Ra+temp] = Rb

temp =temp + 8

LC = LC – 1

#### Description:

This instruction stores a word to consecutive memory locations beginning at the address in Ra until the loop counter reaches zero. This instruction is interruptible.

### SUB - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 418 | Pn4 | Pc4 |

#### Operation:

Rt = Ra - Rb

#### Description:

This instruction subtracts one register from another and places the result into a third register. This instruction may cause an overflow exception.

### SUBI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 49h8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra – Imm

#### Description:

This instruction subtracts an immediate value from a register and places the result into a register. This instruction may cause an overflow exception.

### SUBU - Register-Register

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rt | Rb | Ra | Opcode | Predicate | |
| Rt8 | Rb8 | Ra8 | 458 | Pn4 | Pc4 |

#### Operation:

Rt = Ra - Rb

#### Description:

This instruction subtracts one register from another and places the result into a third register. This instruction never causes an exception.

### SUBUI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Immediate | Rt | Ra | Opcode | Predicate | |
| Immediate7..0 | Rt8 | Ra8 | 4Dh8 | Pn4 | Pc4 |

#### Operation:

Rt = Ra – Imm

#### Description:

This instruction subtracts an immediate value from a register and places the result into a register. This instruction never causes an exception.

### SW – Store Word

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Rt | Ra | Opcode | Predicate | |
| Offset7..0 | Rt8 | Ra8 | 93h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Rb

#### Description:

A sixty-four bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

### SWS – Store Word Special

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Offset | Spr | Ra | Opcode | Predicate | |
| Offset7..0 | Spr8 | Ra8 | 9Eh8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+offset] = Spr

#### Description:

A sixty-four bit value is stored to memory from the source special purpose register Spr. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

### SWX – Store Word Indexed

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 32 | 31 24 | 23 16 | 15 8 | 7 0 | |
| Rc | Rb | Ra | Opcode | Predicate | |
| Rc8 | Rb8 | Ra8 | C3h8 | Pn4 | Pc4 |

#### Operation:

memory[Ra+Rb] = Rc

#### Description:

A sixty-four bit value is stored to memory from the source register Rc. The memory address is the sum of register Ra and Rb. The memory address must be word aligned.

### SYS –Call system routine

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Disp. | Br | Brt | Opcode | Predicate | |
| Offset7..0 | Ch4 | Dh4 | A5h8 | Pn4 | Pc4 |

#### Description:

This instruction calls a system function located as the sum of the offset times 16 plus branch register 12. The return address is stored in the EPC register (Branch register #13).

### TLB – TLB Command

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 16 | | 15 8 | 7 0 | |
| Rb/Rt | Tn | Cmd | Opcode | Predicate | |
| Rb/Rt8 | Tn4 | Cmd4 | F0h8 | Pn4 | Pc4 |

#### Description:

The command is executed on the TLB unit. The command results are placed in internal TLB registers which can be read or written using TLB command instruction. If the operation is a read register operation then the register value is placed into Rt. If the operation is a write register operation, then the value for the register comes from Rb. Otherwise the Rb/Rt field in the instruction is ignored.

Tn4 – This field identifies which TLB register is being read or written.

|  |  |  |
| --- | --- | --- |
| Reg no. |  | Assembler |
| 0 | Wired | Wired |
| 1 | Index | Index |
| 2 | Random | Random |
| 3 | Page Size | PageSize |
| 4 | Virtual page | VirtPage |
| 5 | Physical page | PhysPage |
| 7 | ASID | ASID |
| 8 | Data miss address | DMA |
| 9 | Instruction miss address | IMA |
| 10 | Page Table Address | PTA |
| 11 | Page Table Control | PTC |

#### TLB Commands

|  |  |  |
| --- | --- | --- |
| Cmd | Description | Assembler |
| 0 | No operation |  |
| 1 | Probe TLB entry | TLBPB |
| 2 | Read TLB entry | TLBRD |
| 3 | Write TLB entry corresponding to random register | TLBWR |
| 4 | Write TLB entry corresponding to index register | TLBWI |
| 5 | Enable TLB | TLBEN |
| 6 | Disable TLB | TLBDIS |
| 7 | Read register | TLBRDREG |
| 8 | Write register | TLBWRREG |

Probe TLB – The TLB will be tested to see if an address translation is present.

Read TLB – The TLB entry specified in the index register will be copied to TLB holding registers.

Write Random TLB – A random TLB entry will be written into from the TLB holding registers.

Write Indexed TLB – The TLB entry specified by the index register will be written from the TLB holding registers.

Disable TLB – TLB address translation is disabled so that the physical address will match the supplied virtual address.

Enable TLB – TLB address translation is enabled. Virtual address will be translated to physical addresses using the TLB lookup tables.

The TLB will automatically update the miss address registers when a TLB miss occurs only if the registers are zero to begin with. System software must reset the registers to zero after a miss is processed. This mechanism ensures the first miss that occurs is the one that is recorded by the TLB.

PageTableAddr – This is a scratchpad register available for use to store the address of the page table.

PageTableCtrl – This is a scratchpad register available for use to store control information associated with the page table.

### TST - Register Test Compare

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 16 | 15 12 | 11 8 | 7 0 | |
| Ra | Opc | Pt | Predicate | |
| Ra8 | 04 | Pt4 | Pn4 | Pc4 |

#### Operation:

if Ra < 0

Pt.lt = 1

else

Pt.lt = 0

if Ra = 0

Pt.eq = 1

else

Pt.eq = 0

Pt.ltu = 0

#### Description:

The register test compare compares a register against the value zero and sets the predicate flags appropriately.