Thor Guide

This document contains information pertaining to the Thor processor including the instruction set and formats and softcore interfacing.

2015

robfinch@Finitron.ca

Finitron

1/1/2015

Table of Contents

[Overview 9](#_Toc437827339)

[Design Objectives 9](#_Toc437827340)

[Programming Model 10](#_Toc437827341)

[General Registers 10](#_Toc437827342)

[Code Address Registers 12](#_Toc437827343)

[Program Counter 13](#_Toc437827344)

[Predicates 14](#_Toc437827345)

[Predicate Conditions 14](#_Toc437827346)

[Compiler Usage 15](#_Toc437827347)

[Status Register (SR) 16](#_Toc437827348)

[Debug Address Register (61,0 to 61,3) 17](#_Toc437827349)

[Debug Control Register (61,4) 18](#_Toc437827350)

[Debug Status Register (61,5) 18](#_Toc437827351)

[Operating Modes 19](#_Toc437827352)

[Segmentation 20](#_Toc437827353)

[Software Support 20](#_Toc437827354)

[Address Formation: 20](#_Toc437827355)

[Selecting a segment register 20](#_Toc437827356)

[Non-Segmented Code Area 20](#_Toc437827357)

[Changing the Code Segment 21](#_Toc437827358)

[Segment Usage Conventions 21](#_Toc437827359)

[Power-up State 21](#_Toc437827360)

[Segment Registers 21](#_Toc437827361)

[TLB 22](#_Toc437827362)

[TLB Registers 24](#_Toc437827363)

[TLBWired (#0h) 24](#_Toc437827364)

[TLBIndex (#1h) 24](#_Toc437827365)

[TLBRandom (#2h) 24](#_Toc437827366)

[TLBPageSize (#3h) 24](#_Toc437827367)

[TLBPhysPage (#5h) 24](#_Toc437827368)

[TLBVirtPage (#4h) 25](#_Toc437827369)

[TLBASID (#7h) 25](#_Toc437827370)

[Memory Operations: 26](#_Toc437827371)

[Basic Operations 26](#_Toc437827372)

[Memory Addressing Modes 26](#_Toc437827373)

[Pre-fetching data 26](#_Toc437827374)

[Bypassing the Data Cache 26](#_Toc437827375)

[Push Operations 26](#_Toc437827376)

[Load Speculation 26](#_Toc437827377)

[Store Issuing 26](#_Toc437827378)

[Address Reservation 26](#_Toc437827379)

[Synchronization Operations 27](#_Toc437827380)

[Exceptions 28](#_Toc437827381)

[Precision 28](#_Toc437827382)

[Nesting 28](#_Toc437827383)

[Vectors 28](#_Toc437827384)

[Vector table: 28](#_Toc437827385)

[Hardware Ports 30](#_Toc437827386)

[Reset 30](#_Toc437827387)

[Clock Cycle Counts 31](#_Toc437827388)

[Core Parameters 32](#_Toc437827389)

[Instruction Formats 33](#_Toc437827390)

[RR - Register-Register 33](#_Toc437827391)

[RI - Register-Immediate 33](#_Toc437827392)

[CMP Register-Register Compare 33](#_Toc437827393)

[CMPI Register-Immediate Compare 33](#_Toc437827394)

[TST - Register Test Compare 33](#_Toc437827395)

[CTRL- Control 33](#_Toc437827396)

[BR - Relative Branch 33](#_Toc437827397)

[BRK/NOP 33](#_Toc437827398)

[RTS 33](#_Toc437827399)

[JSR - Jump To Subroutine 33](#_Toc437827400)

[Instruction Set Summary 35](#_Toc437827401)

[Branch Instructions 35](#_Toc437827402)

[Branch Speculation 35](#_Toc437827403)

[Loops 35](#_Toc437827404)

[Subroutine Call / Return 35](#_Toc437827405)

[Comparison Operations 35](#_Toc437827406)

[Arithmetic Operations 35](#_Toc437827407)

[Bitwise Operations 36](#_Toc437827408)

[Logical Operations 36](#_Toc437827409)

[Detailed Instruction Set 37](#_Toc437827410)

[2ADDU - Register-Register 37](#_Toc437827411)

[2ADDUI - Register-Immediate 38](#_Toc437827412)

[4ADDU - Register-Register 39](#_Toc437827413)

[4ADDUI - Register-Immediate 40](#_Toc437827414)

[8ADDU - Register-Register 41](#_Toc437827415)

[8ADDUI - Register-Immediate 42](#_Toc437827416)

[16ADDU - Register-Register 43](#_Toc437827417)

[16ADDUI - Register-Immediate 44](#_Toc437827418)

[ABS – Absolute Value Register 45](#_Toc437827419)

[ADD - Register-Register 46](#_Toc437827420)

[ADDI - Register-Immediate 47](#_Toc437827421)

[ADDU - Register-Register 48](#_Toc437827422)

[ADDUI - Register-Immediate 49](#_Toc437827423)

[AND - Register-Register 50](#_Toc437827424)

[ANDC – And with Complement 51](#_Toc437827425)

[ANDI - Register-Immediate 52](#_Toc437827426)

[BCDADD - Register-Register 53](#_Toc437827427)

[BCDMUL - Register-Register 54](#_Toc437827428)

[BCDSUB - Register-Register 55](#_Toc437827429)

[BFCHG – Bit-field Change 56](#_Toc437827430)

[BFCLR – Bit-field Clear 57](#_Toc437827431)

[BFEXT – Bit-field Extract 58](#_Toc437827432)

[BFEXTU – Bit-field Extract Unsigned 59](#_Toc437827433)

[BFINS – Bit-field Insert 60](#_Toc437827434)

[BFINSI – Bit-field Insert Immediate 61](#_Toc437827435)

[BFSET – Bit-field Set 62](#_Toc437827436)

[BITI – Test bits Register-Immediate 63](#_Toc437827437)

[BR - Relative Branch 64](#_Toc437827438)

[BRK –Break 65](#_Toc437827439)

[BSR - Branch to Subroutine 66](#_Toc437827440)

[CACHE – Cache Command 67](#_Toc437827441)

[CAS – Compare and Swap 68](#_Toc437827442)

[CLI – Clear Interrupt Mask 69](#_Toc437827443)

[CMP Register-Register Compare 70](#_Toc437827444)

[CMPI Register-Immediate Compare 71](#_Toc437827445)

[CNTLO- Count Leading Ones 72](#_Toc437827446)

[CNTLZ- Count Leading Zeros 73](#_Toc437827447)

[CNTPOP- Population Count 74](#_Toc437827448)

[COM – Bitwise Complement 75](#_Toc437827449)

[CPUID – CPU Identification 76](#_Toc437827450)

[DIV - Register-Register Divide 77](#_Toc437827451)

[DIVI - Register-Immediate Divide 78](#_Toc437827452)

[DIVIU – Unsigned Register-Immediate Divide 80](#_Toc437827453)

[DIVU – Unsigned Register-Register Divide 81](#_Toc437827454)

[ENOR - Register-Register 82](#_Toc437827455)

[EOR - Register-Register 83](#_Toc437827456)

[EORI - Register-Immediate 84](#_Toc437827457)

[INC – Increment Memory 85](#_Toc437827458)

[IMM64,IMM56,IMM48,IMM40,IMM32,IMM24,IMM16 86](#_Toc437827459)

[INT –Interrupt 87](#_Toc437827460)

[JMP - Jump To Address 88](#_Toc437827461)

[JSR - Jump To Subroutine Instruction 89](#_Toc437827462)

[LB – Load Byte 90](#_Toc437827463)

[LBU – Load Byte Unsigned 91](#_Toc437827464)

[LBUX – Load Byte Unsigned Indexed 92](#_Toc437827465)

[LBX – Load Byte Indexed 93](#_Toc437827466)

[LC – Load Character 94](#_Toc437827467)

[LCL – Load Cache Line 95](#_Toc437827468)

[LCU – Load Character Unsigned 96](#_Toc437827469)

[LCUX – Load Character Unsigned Indexed 97](#_Toc437827470)

[LCX – Load Character Indexed 98](#_Toc437827471)

[LDI - Load-Immediate 99](#_Toc437827472)

[LDIS - Load-Immediate Special 100](#_Toc437827473)

[LEA – Load Effective Address 101](#_Toc437827474)

[LH – Load Half-Word 102](#_Toc437827475)

[LHU – Load Half-word Unsigned 104](#_Toc437827476)

[LHUX – Load Half-word Unsigned Indexed 105](#_Toc437827477)

[LHX – Load Half-word Indexed 106](#_Toc437827478)

[LOOP – Loop Branch 107](#_Toc437827479)

[LVB – Load Volatile Byte 108](#_Toc437827480)

[LVC – Load Volatile Character 109](#_Toc437827481)

[LVH – Load Volatile Half-word 110](#_Toc437827482)

[LVW – Load Volatile Word 111](#_Toc437827483)

[LVWAR – Load Volatile Word and Reserve 112](#_Toc437827484)

[LW – Load Word 113](#_Toc437827485)

[LWS – Load Word Special 114](#_Toc437827486)

[LWX – Load Word Indexed 115](#_Toc437827487)

[MAX - Register-Register 116](#_Toc437827488)

[MEMDB – Memory Data Barrier 117](#_Toc437827489)

[MEMSB – Memory Synchronization Barrier 118](#_Toc437827490)

[MFSPR – Special Register-Register 119](#_Toc437827491)

[MIN - Register-Register 120](#_Toc437827492)

[MLO – Mystery Logical Operation 121](#_Toc437827493)

[MOV - Register-Register 122](#_Toc437827494)

[MOVS – Move Special Register- Special Register 123](#_Toc437827495)

[MTSPR –Register-Special Register 124](#_Toc437827496)

[MUL - Register-Register Multiply 125](#_Toc437827497)

[MULI - Register-Immediate Multiply 126](#_Toc437827498)

[MULU – Unsigned Register-Register Multiply 127](#_Toc437827499)

[MULUI – Unsigned Register-Immediate Multiply 128](#_Toc437827500)

[MUX – Multiplex 129](#_Toc437827501)

[NAND - Register-Register 130](#_Toc437827502)

[NEG - Negate Register 131](#_Toc437827503)

[NOP – No Operation 132](#_Toc437827504)

[NOR - Register-Register 133](#_Toc437827505)

[NOT – Logical Not 134](#_Toc437827506)

[OR - Register-Register 135](#_Toc437827507)

[ORC – Or with Complement 136](#_Toc437827508)

[ORI - Register-Immediate 137](#_Toc437827509)

[ROL – Rotate Left 138](#_Toc437827510)

[ROLI – Rotate Left by Immediate 147](#_Toc437827511)

[ROR – Rotate Right 148](#_Toc437827512)

[RORI – Rotate Right by Immediate 149](#_Toc437827513)

[RTD – Return from Debug Exception Routine 150](#_Toc437827514)

[RTE – Return from Exception Routine 151](#_Toc437827515)

[RTI – Return from Interrupt Routine 152](#_Toc437827516)

[RTS – Return from Subroutine 153](#_Toc437827517)

[SB – Store Byte 155](#_Toc437827518)

[SBX – Store Byte Indexed 156](#_Toc437827519)

[SC – Store Character 157](#_Toc437827520)

[SCX – Store Character Indexed 158](#_Toc437827521)

[SEI – Set Interrupt Mask 159](#_Toc437827522)

[SH – Store Half-word 160](#_Toc437827523)

[SHL – Shift Left 161](#_Toc437827524)

[SHLI – Shift Left by Immediate 162](#_Toc437827525)

[SHLU – Shift Left Unsigned 163](#_Toc437827526)

[SHLUI – Shift Left Unsigned by Immediate 164](#_Toc437827527)

[SHR – Shift Right 165](#_Toc437827528)

[SHRI – Shift Right by Immediate 166](#_Toc437827529)

[SHRU – Shift Right Unsigned 167](#_Toc437827530)

[SHRUI – Shift Right Unsigned by Immediate 168](#_Toc437827531)

[SHX – Store Half-word Indexed 169](#_Toc437827532)

[STCMP – String Compare 170](#_Toc437827533)

[STFND – String Find 171](#_Toc437827534)

[STI – Store Immediate 172](#_Toc437827535)

[STIX – Store Immediate Indexed 173](#_Toc437827536)

[STMV – String Move 174](#_Toc437827537)

[STP – Stop / Slow Down 175](#_Toc437827538)

[STSB – Store String Byte 176](#_Toc437827539)

[STSC – Store String Character 177](#_Toc437827540)

[STSH – Store String Half-word 178](#_Toc437827541)

[STSW – Store String Word 179](#_Toc437827542)

[SUB - Register-Register 180](#_Toc437827543)

[SUBI - Register-Immediate 181](#_Toc437827544)

[SUBU - Register-Register 182](#_Toc437827545)

[SUBUI - Register-Immediate 183](#_Toc437827546)

[SW – Store Word 184](#_Toc437827547)

[SWCR – Store Word and Clear Reservation 185](#_Toc437827548)

[SWS – Store Word Special 186](#_Toc437827549)

[SWX – Store Word Indexed 187](#_Toc437827550)

[SXB – Sign Extend Byte 188](#_Toc437827551)

[SXC – Sign Extend Character 189](#_Toc437827552)

[SXH – Sign Extend Half-word 190](#_Toc437827553)

[SYNC – Synchronization Barrier 191](#_Toc437827554)

[SYS –Call system routine 192](#_Toc437827555)

[TLB – TLB Command 193](#_Toc437827556)

[TST - Register Test Compare 195](#_Toc437827557)

[ZXB – Zero Extend Byte 196](#_Toc437827558)

[ZXC – Zero Extend Character 197](#_Toc437827559)

[ZXH – Zero Extend Half-word 198](#_Toc437827560)

[Opcode Map 199](#_Toc437827561)

# Overview

Thor is a powerful 64 bit superscalar processor that represents a generational refinement of processor architecture. The processor contains 64, 64 bit general purpose integer registers. Thor uses variable length instructions varying between one and eight bytes in length and handles 8, 16, 32, and 64 bit data within a 64 bit address space.

## Design Objectives

This processor is somewhat pedantic in nature and targeted towards high performance operation as a general purpose processor. Following are some of the criteria that were used on which to base the design.

|  |
| --- |
| * Designed for Superscalar operation - the ability to execute more than one instruction at a time. To achieve high performance it is generally accepted that a processor must be able to execute more than a single instruction in any given clock cycle. |
| * Simplicity - architectural simplicity leads to a design that is easy to implement resulting in reliability and assured correctness along with easy implementation of supporting tools such as compilers. Simplicity also makes it easier to obtain high performance and results in lower overall cost. |
| * Extensibility - the design must be extensible so that features not present in the first release can easily be added at a later date. |
| * Low Cost |

This design meets the above objectives in the following ways. The instruction set has been designed to minimize the interactions between instructions, allowing instructions to be executed as independent units for superscalar operation. There are a sufficient number of registers to allow the compiler to schedule parallel processing of code. A reasonably large general purpose register set is available making the design reasonably compatible with many existing compilers and assemblers. Where needed, additional specialized instructions have been added to the processor to support a sophisticated operating system and interrupt management.

# Programming Model

## General Registers

There are 64 general purpose registers. General purpose registers are 64 bits wide. The general registers may hold integer or floating point values.

Register #0 is always zero.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  |  |  |  |  |  |
| r0 | always zero |  |  | LC | Loop Counter |
| r1 | return value |  |  |  |  |
| r2 | return value |  |  | C0 | always zero |
| r3 |  |  |  | C1 | return address |
| r4 |  |  |  | C2 |  |
| r5 |  |  |  | C3 |  |
| r6 |  |  |  | C4 |  |
| r7 |  |  |  | C5 |  |
| r8 |  |  |  | C6 |  |
| r9 |  |  |  | C7 |  |
| r10 |  |  |  | C8 |  |
| r11 |  |  |  | C9 |  |
| r12 |  |  |  | C10 | catch link address |
| r13 |  |  |  | C11 | debug return address |
| r14 |  |  |  | C12 | exception table pointer |
| r15 |  |  |  | C13 | exceptioned PC |
| r16 |  |  |  | C14 | interrupted PC |
| r17 |  |  |  | C15 | program counter, read only |
| r18 |  |  |  |  |  |
| r19 |  |  |  | ZS | zero segment |
| r20 |  |  |  | DS | data segment |
| r21 |  |  |  | ES | extra segment |
| r22 |  |  |  | FS |  |
| r23 |  |  |  | GS |  |
| r24 |  |  |  | HS |  |
| r26 | Base Pointer |  |  | SS | stack segment |
| r27 | User Stack Pointer1 |  |  | CS | code segment |
| r28 | Accessible only in kernel mode |  |  |  |  |
| r29 |  |  |  | DBAD0 | Debug Address #0 |
| r30 |  |  |  | DBAD1 | Debug address #1 |
| r31 |  |  |  | DBAD2 | Debug address #2 |
| r32/F0 | Floating point |  |  | DBAD3 | Debug Address #3 |
| … |  |  |  | DBCTRL | Debug Control |
| r63/F31 |  |  |  | DBSTAT | Debug Status |

1 this register is implied in the push and rts instructions, and updated by hardware

## Code Address Registers

The processor contains sixteen code address registers (C0-C15). Several of the registers are reserved for predefined purposes. A code address register is used in the formation and storage of code addresses.

|  |  |  |
| --- | --- | --- |
| Reg # |  | Usage |
| 0 | Always Zero | Absolute address formation |
| 1 |  | Subroutine return address |
| 2 |  | This register is available for general use. |
| 3 |  | This register is available for general use. |
| 4 |  | This register is available for general use. |
| 5 |  | This register is available for general use. |
| 6 |  | This register is available for general use. |
| 7 |  | This register is available for general use. |
| 8 |  | This register is available for general use. |
| 9 |  |  |
| 10 | Catch Link Register | Used by the compiler to link to try/catch handlers. |
| 11 | Debug Exception PC | This register is set when a debug exception occurs |
| 12 | Exception Table Pointer | This register points to the exception table in memory. |
| 13 | Exceptioned PC | This register is set when an exception occurs |
| 14 | Interrupted PC | This register is automatically set during a hardware interrupt |
| 15 | Program Counter | Relative address formation. |

Code address registers may be used to point to a block of code from which the JSR instruction can index into with its 24 bit offset. For instance a register may contain a pointer to a class method jump list; the JSR instruction can then index into this list in order to invoke a method.

The presence of multiple code address registers allows multi-level return addresses to be used for performance. Leaf routines may use C1 as the return address. Next to leaf routines may use C2, etc. So that memory operations are avoided when implementing subroutine call and return.

The program counter register is read-only. The program counter cannot be modified by moving a value to this register.

Setting of code address register #12 should be followed with a [SYNC](#_SYNC_–_Synchronization) instruction. The core assumes c12 is essentially static and does not provide full bypassing for this register. The register value may be stale until the sync instruction executes.

### Program Counter

|  |  |
| --- | --- |
| 63 32 | 31 0 |
| Program Bank | Program Counter |

The program counter is special in that it is always incrementing by the size of the instructions fetched as a program runs. Program code is byte aligned. To improve performance only the low order 32 bits of the program counter increment. The entire program counter may be loaded with a jump instruction. If the upper four bits of the program counter/ bank are all ones, then segmentation with the code segment is ignored.

## Predicates

The processor features predicated execution of all instructions. Whether or not an instruction is executed depends on the contents of a predicate register and the predicate condition specified in the predicate byte. There are 16 predicate registers each of which hold three flags. These flags are set as the result of a compare operation. The flags represent equality (eq) signed less than (lt) and unsigned less than (ltu).

|  |  |  |  |
| --- | --- | --- | --- |
| 3 | 2 | 1 | 0 |
| ~ | ltu | lt | eq |

All instructions are executed conditionally determined by the value of a predicate register. The special predicate 00 executes the break vector.

### Predicate Conditions

|  |  |  |  |
| --- | --- | --- | --- |
| Cond. |  | Test |  |
| 0 | PF | 0 | Always false – Instructions predicated with condition zero never execute regardless of the predicate register contents. This is used for extended immediate values as well. The false predicate byte for instructions is 90h. |
| 1 | PT | 1 | Always True – The instruction predicated with an always true condition always executes regardless of the predicate register contents. The always true predicate byte is 01h. Other true predicates are instruction short-forms. |
| 2 | PEQ | eq | Equal – instruction executes if the predicate register equal flag is set |
| 3 | PNE | !eq | Not Equal – instruction executes if the predicate register equal flag is clear |
| 4 | PLE | lt|eq | Less or Equal – predicate less or equal flag is set |
| 5 | PGT | !(lt|eq) | greater than |
| 6 | PGE | !lt | greater or equal |
| 7 | PLT | lt | less than |
| 8 | PLEU | ltu|eq | unsigned less or equal |
| 9 | PGTU | !(ltu|eq) | unsigned greater than |
| 10 | PGEU  POR | !ltu | unsigned greater or equal  Ordered for floating point |
| 11 | PLTU  PUN | ltu | unsigned less than  Unordered for floating point |
| 12 |  |  |  |
| 13 | PSIG | signal | execute if external signal is true |
| 14 |  |  |  |
| 15 |  |  |  |

### Compiler Usage

The compiler uses predicate register #15 to conditionally move TRUE / FALSE values to a register when evaluating a logical operation.

Predicate registers beginning with P0 and incrementing are applied for use as the control flow nesting level increases. The compiler does not support control flow nesting more than 14 levels in a single subroutine. Predicate registers beginning with P14 and decrementing are used in the evaluation of the hook operator. Care must be taken such that the number of predicate registers in use does not exceed the number available.

|  |  |  |
| --- | --- | --- |
| Pred. | Usage |  |
| P0 | control flow level 0 |  |
| P1 | control flow nesting level 1 |  |
| P2 | control flow nesting level 2 |  |
| … |  |  |
| Pn | control flow nesting level n (n not to exceed 14) |  |
| … |  |  |
| P12 | third hook operator in an expression |  |
| P13 | second hook operator in an expression |  |
| P14 | first hook operator in an expression |  |
| P15 | conditionally moves TRUE/FALSE for logical expressions |  |

## Status Register (SR)

This register contains bits that control the overall operation of the processor or reflect the processor’s state. Bits are included for interrupt masking, and system / application mode indicator. This register is split into two halves with both halves having the same format. The lower half of the register is what determines how the processor works. The upper half of the register maintains a backup copy of the lower half for interrupt processing. There are instructions provided for manipulating the interrupt mask.

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 31..16 | 15 | 14 | 13 | 12 | 11..8 | 7..0 |
| same format as 15..0 | Interrupt Mask | Reserved | Kernel / Application Mode Indicator | Float Except. Enable |  |  |
|  | IM | ~ | S | FXE |  |  |

 The Kernel / Application Mode indicator is read-only.

IM = interrupt mask

Maskable interrupts are disabled when this bit is set.

## Debug Address Register (61,0 to 61,3)

These registers contain addresses of instruction or data breakpoints.

|  |
| --- |
| 63 0 |
| Address 63..0 |

## Debug Control Register (61,4)

This register contains bits controlling the circumstances under which a debug interrupt will occur.

|  |  |  |  |
| --- | --- | --- | --- |
| bits |  |  |  |
| 3 to 0 | Enables a specific debug address register to do address matching. If the corresponding bit in this register is set and the address (instruction or data) matches the address in the debug address register then a debug interrupt will be taken. |  |  |
| 17, 16 | This pair of bits determine what should match the debug address register zero in order for a debug interrupt to occur.   |  |  |  | | --- | --- | --- | | 17:16 |  |  | | 00 | match the instruction address |  | | 01 | match a data store address |  | | 10 | reserved |  | | 11 | match a data load or store address |  | |  |  |
| 19, 18 | This pair of bits determine how many of the address bits need to match in order to be considered a match to the debug address register. These bits are ignored when matching instruction addresses, which are always byte aligned.   |  |  |  | | --- | --- | --- | | 19:18 |  | Size | | 00 | all bits must match | byte | | 01 | all but the least significant bit should match | char | | 10 | all but the two LSB’s should match | half | | 11 | all but the three LSB’s should match | word | |  |  |
| 23 to 20 | Same as 16 to 19 except for debug address register one. |  |  |
| 27 to 24 | Same as 16 to 19 except for debug address register two. |  |  |
| 31 to 28 | Same as 16 to 19 except for debug address register three. |  |  |
| 62 |  |  |  |
| 63 |  |  |  |

## Debug Status Register (61,5)

This register contains bits indicating which addresses matched. These bits are set when an address match occurs, and must be reset by software.

|  |  |
| --- | --- |
| bit |  |
| 0 | matched address register zero |
| 1 | matched address register one |
| 2 | matched address register two |
| 3 | matched address register three |
| 63 to 4 | not used, reserved |

# Operating Modes

The core operates in one of two modes: application/user mode or kernel mode. Kernel mode is switched to when an interrupt or exception occurs. On power-up the core is running in kernel mode. An RTI instruction must be executed in order to leave kernel mode after power-up.

A subset of instructions is limited to kernel mode.

# Segmentation

The processor contains eight segment registers. The segment register to use during address formation for data addresses is identified by a field in the instruction. This field is set to default values by the assembler. For code addresses segment register #7 (the CS) is always used.

* If segmentation is not desired then segmentation can effectively be ignored by setting all the segment registers to zero. The processor can also be built without segmentation by commenting out the ‘SEGMENTATION’ definition.

## Software Support

Segment registers may only be transferred to or from one of the general purpose registers. The [mtspr](#_MTSPR_–Register-Special_Register) and [mfspr](#_MFSPR_–_Special) instructions can be used to perform the move. A segment register may also be loaded using the [LDIS](#_LDIS_-_Load-Immediate) instruction. After loading a segment register the instruction stream should be synchronized with a memory barrier ([MEMSB](#_MEMSB_–_Memory)) to ensure the segment value can be ready for a following memory operation.

## Address Formation:

Non-segmented address bits 0 to 11 pass through the segmentation module unchanged. Address bits 63 to 12 are added to the contents of the segment register to form the final segmented address. Note that there is no shift associated with the segment addition. Future implementations of the processor may include additional low order address bits in the segment register in order to allow a finer grain for memory page / paragraph size.

|  |  |
| --- | --- |
| Address[63:12] | Address[11:0] |
| + | + |
| Segment register value[63:12] | 00012 |
| = | |
| Segmented address[63:0] | |

## Selecting a segment register

A specific segment register for a memory operation may be selected using a segment prefix in assembler code. Segment prefixes apply to data addresses only. Code addresses always use segment register #7 – the code segment.

## Non-Segmented Code Area

The address range defined as 64’hFxxxxxxxxxxxxxxx (the top nibble is ‘F’) is a non-segmented code area. This area allows the operating system to work without paying attention to the code segment. Interrupt and exception vectors should vector into the non-segmented code area. The only way to change the code segment is by transferring to the operating system via a sys call instruction.

## Changing the Code Segment

The only way to change the code segment is by transferring to the operating system via a sys call instruction. The operating system, while operating in the non-segmented code area, can alter the code segment without causing a transfer of control. The operating system establishes the code segment for a task while running in the non-segmented code area.

## Segment Bounds

If an address is greater than or equal to the limit specified in the segment limit register then a segment limit exception occurs. This applies for all segments including code and data segments.

## Segment Usage Conventions

Segment register #7 is the code segment (CS) register. All program counter addresses are formed with the code segment register unless the upper nibble of the address is ‘F’ in which case the code segment is ignored.

Segment register #6 is the stack segment (SS) register by convention. Future versions of the core may use this register implicitly for stack accesses. Segment register #1 is the data segment (DS) by convention.

## Power-up State

On reset the value in the segment registers are undefined. Note that the processor begins executing instructions out of the non-segmented code area as the reset address is 64’hFFFFFFFFFFFFEFF0. One of the first tasks of the boot program would be to initialize the segment registers to known values. The segment register must be setup to perform data accesses properly.

### Segment Registers

|  |  |  |  |
| --- | --- | --- | --- |
| Num |  | Long name | Comment |
| 0 | ZS | zero (NULL) segment | by convention contains zero |
| 1 | DS | data segment | by convention – default for loads/stores |
| 2 | ES | extra segment | by convention |
| 3 | FS |  |  |
| 4 | GS |  |  |
| 5 | HS |  |  |
| 6 | SS | Stack segment | default for stack load/stores |
| 7 | CS | Code segment | always used for code addressing |

# TLB

The processor uses a 64 entry TLB (translation look-aside buffer) in order to support virtual memory. The TLB supports variable page sizes from 4kB to 1MB. The TLB is organized as an eight-way eight-set cache.

The TLB is updated by first placing values into the TLB holding registers using the TLB instruction, then issuing a TLB write command using the TLB command instruction.

Address translations will not take place until the TLB is enabled. An enable TLB command must be issued using the TLB command instruction.

TLB Entries:

C2..0

G

D

V

ASID7...0

Virtual Page51...0

Physical Page51...0

G = Global

The global bit marks the TLB entry as a global address translation where the ASID field is not used to match addresses.

ASID = address space identifier

The ASID field in the TLB entry must match the processor’s current ASID value in order for the translation to be considered valid, unless the G bit is set. If the G bit is set in the TLB entry, then the ASID field is ignored during the address comparison.

C = cachability bits

If the cachability bits are set to 001b then the page is uncached, otherwise the page is cached.

D = dirty bit

The dirty bit is set by hardware when a write occurs to the virtual memory page identified by the TLB entry.

V = valid bit

This bit must be set in order for the address translation to be considered valid. The entire TLB may be invalidated using the invalidate all command.

## TLB Registers

### TLBWired (#0h)

This register limits random updates to the TLB to a subset of the available number of ways. TLB ways below the value specified in the Wired register will not be updated randomly. Setting this register provides a means to create fixed translation settings. For instance if the wired register is set to two, the sixteen fixed entries will be available.

### TLBIndex (#1h)

This register contains the entry number of the TLB entry to be read from or written to.

### TLBRandom (#2h)

This register contains a random three bit value used to update a random TLB entry during a TLB write operation.

### TLBPageSize (#3h)

The TLBPageSize register controls which address bits are significant during a TLB lookup.

|  |  |  |
| --- | --- | --- |
| N | Page Size |  |
| 0 | 4KiB |  |
| 1 | 16kiB |  |
| 2 | 64kiB |  |
| 3 | 256kiB |  |
| 4 | 1MiB |  |
|  |  |  |
|  |  |  |

### TLBPhysPage (#5h)

The TLBPhysPage register is a holding register that contains the page number for an associated virtual address. This register is transferred to or from the TLB by TLB instructions.

|  |
| --- |
| 63 0 |
| Physical Page Number |

### TLBVirtPage (#4h)

The TLBVirtPage register is a holding register that contains the page number for an associated physical address. This register is transferred to or from the TLB by TLB instructions.

|  |
| --- |
| 63 0 |
| Virtual Page Number |

### TLBASID (#7h)

The TLBASID register is a holding register that contains the address space identifier (ASID) , valid, dirty, global, and cachability bits associated with a TLB entry. This register is transferred to or from the TLB by TLB instructions.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 63 16 | 15 8 | 6 4 | 2 | 1 | 0 |
| ----- | ASID | C | G | D | V |

# Memory Operations:

## Basic Operations

Basic memory operations include loads, stores, pushes, pops and string operates. Other than those operations there are no other instructions that access memory. Note that return addresses are not pushed onto the stack automatically.

## Memory Addressing Modes

The core supports both register indirect with displacement and scaled indexed addressing. Indexed addressing is supported only with the general purpose register load store operations.

## Pre-fetching data

The load instructions may be used to pre-fetch data by specifying a load into register R0. If R0 is used as the load target register then the load operation will not cause any exception.

## Bypassing the Data Cache

There are several load instructions that bypass the data-cache when loading – see the load volatile (LVx) instructions. These instructions are useful for I/O operations or for when it is better if the data cache is not loaded for performance reasons.

The volatile load instructions only offer sign extension and not zero extension. To zero extend data loaded by a volatile load operation follow it with one of the zero extension (ZXx) instructions.

## Push Operations

The core supports a data push to stack and data pop operation. The data push operation both decrements the stack pointer and stores data to the stack. Argument pushing is commonly used in high-level languages. Subroutine arguments pushed to the stack in high-level languages are usually popped off the stack simply by adding to the stack pointer.

An additional push operation includes pushing an effective address to the stack.

## Load Speculation

The core may load data speculatively in advance of its use provided there is no address overlap with a preceding store instruction.

## Store Issuing

Stores will only be issued if there are no instructions that can exception before the store in the instruction queue. Since many instructions do not cause any exceptions this happens fairly often.

## Atomic Operations

The core has a single atomic memory operation which is the CAS (compare-and-swap) instruction.

## Address Reservation

The address reservation instructions rely on the external memory system to support address reservation. There are only two instruction (LVWAR, SWCR) associated with address reservation. The load instruction creates an address reservation and the store instruction clears it. In a multi-core system the reservation may be created or cleared by another processing core.

## Synchronization Operations

The core includes memory data barrier and memory instruction barrier instructions to allow data to be synchronized during program runs.

# Exceptions

## Precision

Thor’s exceptions are precise. They are processed in order at the location of the exception. For instance if a divide by zero exception occurred then the exception return address is the address of the divide by zero instruction. Instructions after the divide by zero are not committed to the machine state (the results are dropped).

## Nesting

Software exceptions are allowed to nest up to 255 levels. The nesting level is tracked by the core and when it is non-zero the core is in kernel mode. When an exception occurs the nesting level increases, when a return from exception is performed (RTE or RTD) the nesting level decreases. From a software standpoint this allows exceptions to occur in an exception handler. For instance it may be desirable for a debug exception to occur in the handler.

Hardware interrupts do not track the nesting level. The core does not allow nested hardware interrupts. When a hardware interrupt occurs the core is switched to kernel mode.

## Vectors

The processor vectors to $FFFFFFFFFFFFEFF0 on a reset. All other vectoring is done through a vector table. The vector table allows for 256 entries. The vector table base address is established by code address register C12. During an external IRQ the processor looks at a vector number bus to determine the vector to use for the IRQ. This vector number may be hard-coded in which case all IRQ’s will be vectored to the same location. The address vectored to is the sum of C12 and an offset supplied in the instruction multiplied by sixteen. The contents of C12 are undefined at reset; this register must be loaded before interrupts can be processed. Note that segmentation is temporarily disabled during exception processing to allow the vector to be accessed.

### Vector table:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Vector Number | Usage / Description | |  |  |
| 0 | BREAK instruction vector | |  |  |
| 1 | SLEEP vector (branch to self) | |  |  |
| 2 | Task reschedule interrupt | |  |  |
| … |  | |  |  |
| 192 | Spurious interrupt | |  |  |
| 193 | IRQ level 1 | 1000 Hz interrupt |  |  |
| 194 | IRQ level 2 | 100 Hz interrupt |  |  |
| … | Other IRQ levels |  |  |  |
| 207 | IRQ level 15 | keyboard interrupt |  |  |
| … |  | |  |  |
| 240 | overflow (integer) | |  |  |
| 241 | divide by zero (integer) | |  |  |
| 242 | floating point | |  |  |
| 243 | debug | |  |  |
| 244 | segmentation | |  |  |
| 245 | privilege violation | |  |  |
| …. |  | |  |  |
| 248 | DTLBMiss | |  |  |
| 249 | ITLB Miss | |  |  |
| 250 | Unimplemented instruction | |  |  |
| 251 | Bus error – data load / store | |  |  |
| 252 | Bus error – instruction fetch | |  |  |
| 253 | reserved | |  |  |
| 254 | NMI interrupt vector | |  |  |
| 255 | * reserved | |  |  |

**Mnemonics**

|  |  |
| --- | --- |
|  |  |
| DBG | debug |
| DBE | data bus error |
| TLB | TLB miss |
| LMT | segment limit |
|  |  |

# Hardware Ports

Thor uses a WISHBONE bus to communicate with the outside world.

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
|  | I/O | Width | WB |  |  |
| corenum | I | 32 |  | core number – this number is used to identify the core and is reflected in the cpuid register. Meant to be a hardcoded constant. |  |
| rst\_i | I | 1 | WB | reset signal |  |
| clk\_i | I | 1 | WB | clock |  |
| clk\_o | O | 1 |  | output (gated) clock |  |
| km | O | 1 |  | kernel mode indicator |  |
| nmi\_i | I | 1 |  | non-maskable interrupt input |  |
| irq\_i | I | 1 |  | maskable interrupt input |  |
| vec\_i | I | 8 |  | interrupt vector |  |
| bte\_o | O | 2 | WB | burst type extension |  |
| cti\_o | O | 3 | WB | cycle type indicator |  |
| bl\_o | O | 5 |  | burst length output |  |
| lock\_o | O | 1 | WB | bus lock |  |
| resv\_o | O | 1 |  | reserve address |  |
| resv\_i | I | 1 |  | address reservation status in |  |
| cres\_o | O | 1 |  | clear address reservation |  |
| cyc\_o | O | 1 | WB | cycle is valid |  |
| stb\_o | O | 1 | WB | data transfer is taking place |  |
| ack\_i | I | 1 | WB | data transfer acknowledge |  |
| err\_i | I | 1 | WB | bus error occurred input |  |
| we\_o | O | 1 | WB | write enable |  |
| sel\_o | O | 8 | WB | byte lane selects |  |
| adr\_o | O | 64 | WB | address output |  |
| dat\_i | I | 64 | WB | data input bus |  |
| dat\_o | O | 64 | WB | data output bus |  |
|  |  |  |  |  |  |

WB = see the WISHBONE spec rev B3

# Reset

On reset the core begins fetching and executing instruction at address $FFFFFFFFFFFF**E**FF0. Note that the last 4k bytes of memory are unreachable to the processing core due to limitations in the segment boundary checking. The last 4k bytes should not be used to store instructions or data.

On power-up or reset interrupts are disabled automatically, In order to enable interrupts the RTI instruction must be executed. An [RTI](#_RTI_–_Return) automatically enables interrupts. Note that the interrupt mask must also be cleared with the CLI instruction to allow maskable interrupts to occur.

After reset or NMI the core begins processing at a half the maximum clock rate. The [STP](#_STP_–_Stop) instruction must be issued to get the processer running at full speed.

# Clock Cycle Counts

The core has a minimum CPI of 0.5 clocks per instruction running trivial sample code. Many instructions can be done in pairs provided there are no dependencies between the instructions. Due to the out of order execution ability of the core the latency of longer running instructions may be hidden. The core may be busy working on up to four instructions at once: two ALU or an ALU and memory op, a floating point op and a branch instruction.

# Core Parameters

|  |  |  |
| --- | --- | --- |
| DBW | 32 | The parameter controls the width of data processed by the core. Set to 64 for 64 bit processing. This parameter should be either 64 or 32. If the width is set to 32 bit then double precision floating point operations are unavailable. Also only eight predicate registers are available. |
| ABW | 32 | This parameter controls the width of the external address bus. |
| ALU1BIG | 0 | This parameter controls whether or not ALU1 supports all instructions or only a subset of instructions. The default is to support only the most common instructions. (0 = limited, 1 = all) in order to reduce the size of the core.  Limiting the number of instructions supported may impact performance of the core because it may not be possible to issue two instructions in the same cycle. |

# Configuration Defines

|  |  |  |
| --- | --- | --- |
| Definition | Default | Comment |
| SEGMENTATION | 1 | Causes the core to include segmentation. If segmentation is not desired then this can be commented out to produce an unsegmented core. |
| STRINGOPS | 1 | Causes the core to include memory string operations. |
| DEBUG\_LOGIC | 1 | Causes the core to include logic to support the debug registers. Once the application is working well it may be desirable to reduce the size of the core by removing the debug registers and associated logic. |
| TRAP\_ILLEGALOPS | 1 | Causes the core to include logic to trap for illegal operations during runtime. Once the target application is working well it may be desirable to remove the illegal instruction trapping. |
| FLOATING\_POINT | 1 | Causes the core to include floating point operations. Comment out to reduce the size of the core. |
| BITFIELDOPS | 1 | Causes the core to include bit-field operations if defined. |

# Instruction Formats

Instructions vary in length from one to eight bytes. There are only a few of single byte instructions consisting of only a predicate. Some of the more common formats are shown below.

All instruction sequences begin with a predicate byte that determines the conditions under which the instruction executes. With the exception of special predicate values, the next field in the instruction is always the opcode byte. All instructions may be preceded by an extended constant value.

### RR - Register-Register

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Func | Rt | Rb | Ra | Opcode | Predicate | |
| Func6 | Rt6 | Rb6 | Ra6 | Opcode8 | Pn4 | Pc4 |

### RI - Register-Immediate

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | Opcode8 | Pn4 | Pc4 |

### CMP Register-Register Compare

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 12 | 11 8 | 7 0 | |
| Opc4 | Rb6 | Ra6 | 14 | Pt4 | Pn4 | Pc4 |

### CMPI Register-Immediate Compare

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 31 22 | | | | 21 16 | | | | 15 12 | | | 11 8 | | 7 0 | | | |
| Immed9..0 | | | | Ra6 | | | | 24 | | | Pt4 | | Pn4 | | | Pc4 |
| TST - Register Test Compare | | | | | | | | | | | | |  | | | |  | | CTRL- Control | | | | | | |
| 2322 21 16 | | | 15 12 | | | 11 8 | | | 7 0 | | | |  | | | |  | | 15 8 | | 7 0 | | | | |
| O2 | Ra6 | | 04 | | | Pt4 | | | Pn4 | | Pc4 | |  | | | |  | | Opcode8 | | Pn4 | | | Pc4 | |
| BR - Relative Branch | | | | | | | | | | | |  | |  | | | | BRK/NOP | | | |  | RTS | | | |
| 23 16 | | 15 8 | | | | | 7 0 | | | | |  | |  | | | | 7 0 | | | |  | 7 0 | | | |
| Disp7..0 | | 34 | | | D11..8 | | Pn4 | | | Pc4 | |  | | |  | | | 0/14 | | 04 | |  | 14 | | 14 | |

### JSR - Jump To Subroutine

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 47 24 | 23 16 | | 15 8 | 7 0 | |
| Offset23..0 | Cr4 | Crt4 | Opcode8 | Pn4 | Pc4 |

# Instruction Set Summary

A number of rarely used instructions may only execute on ALU #0. These instructions are identified in the text.

## Illegal Instructions

By default the core traps all illegal instructions through vector #250. The logic to trap illegal instructions may be removed by commenting out the TRAP\_ILLEGALOPS definition.

## Branch Instructions

The core has only a single relative branch instruction which branches relative to the address of the next instruction. This single branch instruction may be used to implement branching on multiple complex conditions when combined with a predicate. The branch instruction supports a 12 bit displacement field.

### Branch Speculation

Branches are performed speculatively in the fetch stage of the core according to branch predictor output. Branches use a (2, 2) co-relating branch predictor with a 256 entry branch history table. Both global and local branch histories are maintained.

## Loops

There is a loop instruction and corresponding loop count register to support counted loops. The loop instruction is predicted as always taken and does not consume room in the branch history table. Like a branch instruction a loop instruction takes place at the fetch stage of the core. The loop instruction supports only and eight bit displacement field which may not be extended.

## Subroutine Call / Return

Program counter relative jumps and calls may be achieved using the program counter as the index register in jump instructions. The jump instruction directly supports up to 24 bit addressing. A shorter jump instruction is available that supports 16 bit addressing. The addressing capabilities of the jump instruction may be increased by applying an immediate prefix to the instruction. It is envisioned that the 16/24 bit jump addressing is sufficient for most cases when combined with usage of the code segment.

## Comparison Operations

Comparison operations include CMP and TST (compare to zero). Comparison operations set a predicate register to the result status of the comparison.

## Arithmetic Operations

|  |  |
| --- | --- |
| Mnemonic |  |
| ADD | addition |
| ADDU | unsigned addition |
| SUB | subtraction |
| SUBU | unsigned subtraction |
| MUL | multiplication |
| MULU |  |
| DIV | division |
| DIVU |  |
| NEG | negative |
| ABS | absolute value |
| MIN | minimum value |
| MAX | maximum value |

## Bitwise Operations

Bitwise operations include ‘and’, ‘or’ and exclusive ‘or’ along with their inverted versions.

|  |  |  |
| --- | --- | --- |
| Mnemonic | Has Immediate Form |  |
| AND | Y |  |
| OR | Y |  |
| EOR | Y |  |
| NAND | N |  |
| NOR | N |  |
| ENOR | N |  |
| ANDC | N |  |
| ORC | N |  |
| COM | N | invert bits |

## Logical Operations

The core includes the logical ‘not’ (NOT) operation. The NOT operation reduces the value to a one or zero result.

# Detailed Instruction Set

### 2ADDU - Register-Register

**Description:**

Multiply Ra by two and add Rb and place the sum in the target register. This instruction will never cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 08h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 2 + Rb

**Exceptions:** none

### 2ADDUI - Register-Immediate

**Description:**

Multiply Ra by two and add immediate and place the sum in the target register. This instruction will never cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 6Bh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 2 + immediate

**Exceptions:** none

### 4ADDU - Register-Register

**Description:**

Multiply Ra by four and add Rb and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 09h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 4 + Rb

**Exceptions:** none

### 4ADDUI - Register-Immediate

**Description:**

Multiply Ra by four and add immediate and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immed11..0 | Rt6 | Ra6 | 6Ch8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 4 + immediate

**Exceptions:** none

### 8ADDU - Register-Register

**Description:**

Multiply Ra by eight and add Rb and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 0Ah6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 8 + Rb

**Exceptions:** none

### 8ADDUI - Register-Immediate

**Description:**

Multiply Ra by eight and add immediate and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immed11..0 | Rt6 | Ra6 | 6Dh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 8 + immediate

**Exceptions:** none

### 16ADDU - Register-Register

**Description:**

Multiply Ra by sixteen and add Rb and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 0Bh6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 16 + Rb

**Exceptions:** none

### 16ADDUI - Register-Immediate

**Description:**

Multiply Ra by sixteen and add immediate and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immed11..0 | Rt6 | Ra6 | 6Eh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra \* 16 + immediate

**Exceptions:** none

### ABS – Absolute Value Register

**Description:**

This instruction takes the absolute value of a register and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 34 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

If Ra < 0

Rt = -Ra

else

Rt = Ra

**Exceptions:** none

### ADD - Register-Register

**Description:**

Add two registers and place the sum in the target register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 00h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra + Rb

**Exceptions:** integer overflow

### ADDI - Register-Immediate

**Description:**

Add a register and immediate value and place the sum in the target register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 48h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra + immediate

**Exceptions:** integer overflow

### ADDU - Register-Register

**Description:**

Add registers Ra and Rb and place the result into register Rt. This instruction will never cause any exceptions.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 04h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra + Rb

**Exceptions:** none

### ADDUI - Register-Immediate

**Description:**

Add a register and immediate value and place the sum in the target register. This instruction will never cause an exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Ch8 | Pn4 | Pc4 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 22 | 21 16 | 15 8 | 7 0 | |
| Immediate9..0 | Rt6 | 47h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra + Immediate

**Exceptions:** none

### AND - Register-Register

**Description:**

Bitwise and’s two registers and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 00h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra & Rb

**Exceptions:** none

### ANDC – And with Compliment

**Description:**

Bitwise and’s a register Ra with the compliment of register Rb and places the result in a target register. There is no immediate form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 06h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra & ~Rb

**Exceptions:** none

### ANDI - Register-Immediate

**Description:**

Bitwise and’s register and an immediate value and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 53h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Rt = Ra & immediate

**Exceptions:** none

### BCDADD - Register-Register

**Description:**

Adds two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is an eight bit BCD number.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 00h6 | Rt6 | Rb6 | Ra6 | F5h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra + Rb

**Exceptions:** none

### BCDMUL - Register-Register

**Description:**

Multiplies two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is a 16 bit BCD value.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 02h6 | Rt6 | Rb6 | Ra6 | F5h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 Only

**Operation:**

Rt = Ra \* Rb

**Exceptions:** none

### BCDSUB - Register-Register

**Description:**

Subtracts two registers using BCD arithmetic and places the result in a target register. Only the low order byte of the register is used. The result is an eight bit BCD number.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 01h6 | Rt6 | Rb6 | Ra6 | F5h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra - Rb

**Exceptions:** none

### BFCHG – Bit-field Change

**Description:**

Inverts the bit-field in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 34 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFCLR – Bit-field Clear

**Description:**

Sets the bits to zero of the bit-field in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 24 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFEXT – Bit-field Extract

**Description:**

Extracts a bit-field from register Ra located between the mask begin (mb) and mask end (me) bits and places the sign extended result into the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 54 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFEXTU – Bit-field Extract Unsigned

**Description:**

Extracts a bit-field from register Ra located between the mask begin (mb) and mask end (me) bits and places the zero extended result into the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 44 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFINS – Bit-field Insert

**Description:**

Inserts a bit-field into the target register located between the mask begin (mb) and mask end (me) bits from the low order bits of Ra.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 04 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFINSI – Bit-field Insert Immediate

**Description:**

Inserts a bit-field into the target register located between the mask begin (mb) and mask end (me) bits from the bits specified in the instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 64 | me6 | mb6 | Rt6 | Imm6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BFSET – Bit-field Set

**Description:**

Sets the bits to one of the bit-field in Ra located between the mask begin (mb) and mask end (me) bits and stores the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 4744 | 43 40 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | 14 | me6 | mb6 | Rt6 | Ra6 | AAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Exceptions:** none

### BITI – Test bits Register-Immediate

**Description:**

Logically and’s register and an immediate value and places the result in a predicate register. If the result of the ‘and’ operation is zero the predicate register’s zero flag is set, otherwise it is cleared. If the result is negative the predicate’s less than flag is set, otherwise it is cleared.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 28 | 26 | 25 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | ~2 | Pt4 | Ra6 | 46h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Pt = flag results( Ra & immediate)

**Predicate Results:**

|  |  |
| --- | --- |
| Predicate flag | Setting |
| eq | set if result is zero |
| lt | set if result is negative |
| ltu | set if result is odd (bit 0 is set) |
|  |  |

**Exceptions:** none

### BR - Relative Branch

**Description:**

A branch is made relative to the address of the next instruction.

* The twelve bit displacement field cannot be extended with an immediate constant prefix. Branches are executed immediately in the instruction fetch stage of the processor before it is known if there is a prefix present.

**Instruction Format:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 16 | 15 8 | | 7 0 | |
| Disp7..0 | 3h4 | D11..8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s / Branch

**Operation:**

PC <= PC + displacement

**Exceptions:** none

### BRK –Break

**Description:**

This instruction contains only a predicate byte. The Break exception is executed. The core will be switched to kernel mode.

**Instruction Format:**

|  |  |
| --- | --- |
| 7 0 | |
| 04 | 04 |

### BSR - Branch to Subroutine

**Description:**

This is an alternate mnemonic for the JSR instruction. A jump is made to the sum of the sign extended displacement supplied in the displacement field of the instruction and the specified code address register Cr.

The subroutine return address is stored in a code address register specified in the Crt field of the instruction.

Typically code address register #1 is used to store the return address.

**Instruction Formats:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 47 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Displacement23..0 | 154 | Crt4 | A2h8 | Pn4 | Pc4 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 24 | 23 20 | 1916 | 15 8 | 7 0 | |
| Displacement15..0 | 154 | Crt4 | A1h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Exceptions:** none

### CACHE – Cache Command

**Description:**

This instruction issues a command to the cache.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 31 26 | 2524 | 23 22 | 21 16 | 15 8 | 7 0 | |
| Func6 | ~2 | ~2 | Ra6 | 9Fh8 | Pn4 | Pc4 |

**Operation:**

**Commands:**

|  |  |
| --- | --- |
| Func6 |  |
| 0 | Invalidate entire instruction cache |
| 1 | Invalidate instruction cache line (address in Ra) |
| 32 | Invalidate entire data cache |
| 33 | Invalidate data cache line (address in Ra) |
|  |  |

### CAS – Compare and Swap

**Description:**

If the contents of the addressed memory cell is equal to the contents of Rb then a sixty-four bit value is stored to memory from the source register Rc. The original contents of the memory cell are loaded into register Rt. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be word aligned. If the operation was successful then Rt and Rb will be the same value. The compare and swap operation is an atomic operation; the bus is locked during the load and potential store operation. This operation assumes that the addressed memory location is part of the volatile region of memory and bypasses the data cache.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Displacement7..0 | Rt6 | Rc6 | Rb6 | Ra6 | 97h8 | Pn4 | Pc4 |

**Operation:**

Rt = memory [Ra + displacement]

if memory[Ra + displacement] = Rb

memory[Ra + displacement] = Rc

**Assembler:**

CAS Rt,Rb,Rc,offset[Ra]

### CLI – Clear Interrupt Mask

**Description:**

This instruction is used to enable interrupts. This instruction is available only while operating in kernel mode.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| FAh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Operation:**

im = 0

**Exceptions:** privilege violation

### CMP Register-Register Compare

**Description:**

The register compare instruction compares two registers and sets the flags in the target predict register as a result.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3128 | 27 22 | 21 16 | 15 12 | 11 8 | 7 0 | |
| 04 | Rb6 | Ra6 | 14 | Pt4 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

if signed Ra < signed Rb

P.lt = true

else

P.lt = false

if unsigned Ra < unsigned Rb

P.ltu = true

else

P.ltu = false

if Ra = Rb

P.eq = true

else

P.eq = false

**Exceptions:** none

### CMPI Register-Immediate Compare

**Description:**

The register immediate compare instruction compares a register to an immediate value and sets the flags in the target predict register as a result. Both a signed and unsigned comparison take place at the same time.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 22 | 21 16 | 15 12 | 11 8 | 7 0 | |
| Immed10 | Ra6 | 24 | Pt4 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

if signed Ra < signed immediate

P.lt = true

else

P.lt = false

if unsigned Ra < unsigned immediate

P.ltu = true

else

P.ltu = false

if Ra = immediate

P.eq = true

else

P.eq = false

### CNTLO- Count Leading Ones

**Description:**

This instruction counts the number of leading ones in a register and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 64 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

**Exceptions:** none

### CNTLZ- Count Leading Zeros

**Description:**

This instruction counts the number of leading zeros in a register and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 54 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

**Exceptions:** none

### CNTPOP- Population Count

**Description:**

This instruction counts the number of one bits in a register and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 74 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

**Exceptions:** none

### COM – Bitwise Compliment

**Description:**

This instruction performs a bitwise compliment on a register and places the result in a target register. If bit is a one then the bit is replaced with is zero otherwise it is replaced with a one.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| B4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = ~ Ra

**Exceptions:** none

### CPUID – CPU Identification

**Description:**

This instruction returns general information about the core. Register Ra is used as a table index to determine which row of information to return.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 04 | Rt6 | Ra6 | 41h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Info[Ra]

**Exceptions**: none

|  |  |  |
| --- | --- | --- |
| Index | bits | Information Returned |
| 0 | 63 to 0 | The processor core identification number. This field is determined from an external input. It would be hard wired to the number of the core in a multi-core system. |
| 2 | 63 to 0 | Manufacturer name first eight chars “Finitron” |
| 3 | 63 to 0 | Manufacturer name last eight characters |
| 4 | 63 to 0 | CPU class “64BitSS” |
| 5 | 63 to 0 | CPU class |
| 6 | 63 to 0 | CPU Name “Thor” |
| 7 | 63 to 0 | CPU Name |
| 8 | 63 to 0 | Model Number “M1” |
| 9 | 63 to 0 | Serial Number “1234” |
| 10 | 63 to 0 | Features bitmap |
| 11 | 31 to 0 | Instruction Cache Size (32kB) |
| 11 | 63 to 32 | Data cache size (16kB) |

### DIV - Register-Register Divide

**Description:**

Performs a signed division of two registers and places the quotient in the target register. This instruction may cause an overflow or divide by zero exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 03h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 65

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra / Rb

**Exceptions**: divide by zero

### DIVI - Register-Immediate Divide

**Description:**

Performs a signed divide of a register and an immediate value and places the result in a target register. This instruction may cause an overflow or divide by zero exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Bh8 | Pn4 | Pc4 |

**Clock Cycles:** 65

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra / immediate

**Exceptions**: divide by zero

### DIVIU – Unsigned Register-Immediate Divide

**Description:**

Performs an unsigned divide of a register and an immediate value and places the result in a target register. This instruction will not cause an overflow or divide by zero exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Fh8 | Pn4 | Pc4 |

**Clock Cycles:** 65

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra / immediate

**Exceptions:** none

### DIVU – Unsigned Register-Register Divide

**Description:**

Performs an unsigned division of two registers and places the quotient in the target register. This instruction not cause an overflow or divide by zero exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 07h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 65

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra / Rb

**Exceptions:** none

### ENOR - Register-Register

**Description:**

Bitwise exclusive or register with register and place inverted result in target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 05h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = ~(Ra ^ Rb)

**Exceptions:** none

### EOR - Register-Register

**Description:**

Bitwise exclusive or register with register and place result in target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 02h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra ^ Rb

**Exceptions:** none

### EORI - Register-Immediate

**Description:**

Bitwise exclusive or register with immediate and place result in target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 55h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra ^ immediate

**Exceptions:** none

### INC – Increment Memory

**Description:**

Memory is incremented by the amount specified in the instruction. The memory address is the sum of the sign extended displacement and register Ra. The amount is between -128 and +127. Note that the increment is not an atomic memory operation. The bus is not locked during the increment to allow cached data to be incremented. For atomic memory operations see the [CAS](#_CAS_–_Compare) instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 47 40 | 3937 | 36 28 | 27 22 | | 21 16 | 15 8 | 7 0 | |
| Amt8 | Sg3 | Displacement8..0 | O3 | Sz3 | Ra6 | C7h8 | Pn4 | Pc4 |

**Execution Units:** All Memory

**Operation:**

(mem[Ra+offset]) = (mem[Ra+offset]) + amt

### IMM64,IMM56,IMM48,IMM40,IMM32,IMM24,IMM16

**Immediate Extensions**

The immediate extension predicates are used to extend the immediate constant of the following instruction. The extensions may add from one to seven bytes more to the constant. Most, but not all instructions can accept a predicated immediate.

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Immediate | | | | | | | Predicate | |
| Immediate63..8 | | | | | | | 84 | 04 |
| Immediate55..8 | | | | | | 74 | 04 |
| Immediate47..8 | | | | | 64 | 04 |
| Immediate39..8 | | | | 54 | 04 |
| Immediate31..8 | | | 44 | 04 |
| Immediate23..8 | | 34 | 04 |
| Immediate15..8 | 24 | 04 |

**Clock Cycles:** 1

**Execution Units: Enqueue**

**Exceptions:** none

### INT –Interrupt

**Description:**

This instruction calls a system function located as the sum of the zero extended offset times 16 plus code address register 12. The return address is stored in the IPC register (code address register #14).

The offset field of this instruction cannot be extended.

Note that this instruction is automatically invoked for hardware interrupt processing. This instruction would not normally be used by software and is not supported by the assembler. The return address stored is the address of the interrupt instruction, not the address of the next instruction. To call system routines use the [SYS](#_SYS_–Call_system) instruction.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset7..0 | Ch4 | Eh4 | A6h8 | Pn4 | Pc4 |

### JMP - Jump To Address

**Description:**

This is an alternate mnemonic for the JSR instruction.

A jump is made to the sum of the zero extended offset supplied in the offset field of the instruction and the specified code address register Cr. The JMP instruction may be used with an immediate predicate constant in order to extend the address range of the jump.

**Instruction Formats:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 47 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset23..0 | Cr4 | 04 | A2h8 | Pn4 | Pc4 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset15..0 | Cr4 | 04 | A1h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

pc = Cr[n] + offset

**Exceptions:** none

### JSR - Jump To Subroutine Instruction

**Description:**

A jump is made to the sum of the zero extended offset supplied in the offset field of the instruction and the specified code address register Cr. The JSR instruction may be used with an immediate predicate constant in order to extend the address range of the jump.

The subroutine return address is stored in a code address register specified in the Crt field of the instruction. Typically code address register #1 is used.

An immediate constant prefix applied to this instruction overrides offset bits 8 to 23 and acts like an eight bit immediate constant extension used by other instructions.

**Instruction Formats:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 47 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset23..0 | Cr4 | Crt4 | A2h8 | Pn4 | Pc4 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset15..0 | Cr4 | Crt4 | A1h8 | Pn4 | Pc4 |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 20 | 19 16 | 15 8 | 7 0 | |
| Cr4 | Crt4 | A0h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Cr[t] = pc

pc = Cr[n] + offset

**Exceptions:** none

### LB – Load Byte

**Description:**

An eight bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

This instruction will load data from the cache and cause a cache load operation if the data isn’t in the cache. To bypass the cache use the [LVB](#_LVB_–_Load) instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 80h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra+offset])

**Exceptions:** DBE, DBG, LMT, TLB

### LBU – Load Byte Unsigned

**Description:**

An eight bit value is loaded from memory and zero extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 81h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = zero extend (mem[Ra+offset])

**Exceptions:** DBE, DBG, LMT, TLB

### LBUX – Load Byte Unsigned Indexed

**Description:**

An eight bit value is loaded from memory zero extended and placed in the target register Rt. The memory address is the sum of register Ra and scaled register Rb.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B1h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = mem[Ra+Rb]

**Exceptions:** DBE, DBG, LMT, TLB

### LBX – Load Byte Indexed

**Description:**

An eight bit value is loaded from memory and placed in the target register. The memory address is the sum of register Ra and scaled register Rb.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B0h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra+Rb])

**Exceptions:** DBE, DBG, LMT, TLB

### LC – Load Character

**Description:**

A sixteen bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 82h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra + displacement])

**Exceptions:** DBE, DBG, LMT, TLB

### LCL – Load Cache Line

**Description:**

The cache line is loaded from memory into the cache (instruction or data). The memory address is the sum of the sign extended offset and register Ra.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Tgt6 | Ra6 | 8Fh8 | Pn4 | Pc4 |

**Execution Units:** Cache / Memory

**Operation:**

Rt = sign extend (mem[Ra+offset])

Target:

|  |  |
| --- | --- |
| Tgt6 | Cache |
| 0 | instruction cache |
| 1 | data cache |

### LCU – Load Character Unsigned

**Description:**

A sixteen bit value is loaded from memory and zero extended, then placed in the target register. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 83h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = zero extend (mem[Ra + displacement])

**Exceptions:** DBE, DBG, LMT, TLB

### LCUX – Load Character Unsigned Indexed

**Description:**

A sixteen bit value is loaded from memory, zero extended and placed in the target register Rt. The memory address is the sum of register Ra and scaled register Rb. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B3h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = mem[Ra + Rb \* scale]

**Exceptions:** DBE, DBG, LMT, TLB

### LCX – Load Character Indexed

**Description:**

A sixteen bit value is loaded from memory, sign extended and placed in the target register Rt. The memory address is the sum of register Ra and scaled register Rb. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B2h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = mem[Ra + Rb \* scale]

**Exceptions:** DBE, DBG, LMT, TLB

### LDI - Load-Immediate

**Description:**

This instruction loads a sign extended immediate constant into a register. The immediate constant may be extended by using an immediate prefix instruction.

**Instruction Format:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 22 | 21 16 | 15 8 | 7 0 | |
| Immediate9..0 | Rt6 | 6Fh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = immediate

### LDIS - Load-Immediate Special

**Description:**

This instruction loads a sign extended immediate constant into a special purpose register. The immediate constant may be extended by using an immediate prefix instruction. Typical usage is to initialize a code address register with a target address.

**Instruction Format:**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 31 22 | 21 16 | 15 8 | 7 0 | |
| Immediate9..0 | Spr6 | 9Dh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Spr = immediate

### LEA – Load Effective Address

**Description:**

This is an alternate mnemonic for the ADDUI instruction. The memory address is placed in the target register. The memory address is the sum of the sign extended offset and register Ra.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Offset11..0 | Rt6 | Ra6 | 4Ch8 | Pn4 | Pc4 |

**Operation:**

Rt = Ra+offset

**Execution Units:** All ALU’s

### LH – Load Half-Word

**Description:**

A thirty-two bit value is loaded from memory and sign extended, then placed in the target register Rt. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 84h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra + displacement])

**Exceptions:** DBE, DBG, LMT, TLB

### LHU – Load Half-word Unsigned

**Description:**

A thirty-two bit value is loaded from memory and zero extended, then placed in the target register Rt. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 85h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = zero extend (mem[Ra + displacement])

**Exceptions:** DBE, DBG, LMT, TLB

### LHUX – Load Half-word Unsigned Indexed

**Description:**

A thirty-two bit value is loaded from memory, zero extended and placed in the target register. The memory address is the sum of register Ra and register Rb. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B5h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = mem[Ra+Rb\*scale]

**Exceptions:** DBE, DBG, LMT, TLB

### LHX – Load Half-word Indexed

**Description:**

A thirty-two bit value is loaded from memory sign extended and placed in the target register Rt. The memory address is the sum of register Ra and scaled register Rb. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B4h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra + Rb \* scale])

**Exceptions:** DBE, DBG, LMT, TLB

### LOOP – Loop Branch

**Description:**

A branch is made relative to the address of the next instruction if the loop count register is non-zero. The loop count register is decremented by this instruction. The predicate condition must also be met. The loop branch is predicted as always taken and does not consume room in the branch predication tables. The displacement constant may not be extended as the loop takes place in the instruction fetch stage of the core.

**Instruction Format:**

|  |  |  |  |
| --- | --- | --- | --- |
| 23 16 | 15 8 | 7 0 | |
| Disp7..0 | A4h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s / Branch

**Operation:**

If LC <> 0

PC <= PC + displacement

LC = LC - 1

### LVB – Load Volatile Byte

**Description:**

An eight bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended displacement and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices. This instruction may also be used when it is known that the data is better not cached.

There is no indexed or unsigned form for this instruction. The value loaded may be zero extended rather than sign extended by following it with the [ZXB](#_ZXB_–_Zero) instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | ACh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra+offset])

**Exceptions:** DBE, DBG, LMT, TLB

### LVC – Load Volatile Character

**Description:**

A sixteen bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

There is no indexed or unsigned form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | ADh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra+offset])

**Exceptions:** DBE, DBG, LMT, TLB

### LVH – Load Volatile Half-word

**Description:**

A thirty-two bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

There is no indexed or unsigned form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | AEh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra+offset])

**Exceptions:** DBE, DBG, LMT, TLB

### LVW – Load Volatile Word

**Description:**

A sixty-four bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices.

There is no indexed or unsigned form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | AFh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra + displacement])

**Exceptions:** DBE, DBG, LMT, TLB

### LVWAR – Load Volatile Word and Reserve

**Description:**

A sixty-four bit value is loaded from memory and sign extended, then placed in the target register. The memory address is the sum of the sign extended offset and register Ra. Additionally the reserve signal is activated on the bus to tell the memory system to place an address reservation. This instruction bypasses the data cache. Use this instruction to load data from volatile memory regions such as I/O devices. The primary purpose of this instruction is to setup semaphores. See also the [SWCR](#_SWCR_–_Store), [CAS](#_CAS_–_Compare) instructions.

There is no indexed form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 8Bh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = sign extend (mem[Ra + displacement]); reserve = 1

**Exceptions:** DBE, DBG, LMT, TLB

### LW – Load Word

**Description:**

A sixty-four bit value is loaded from memory and placed in the target register. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 86h8 | Pn4 | Pc4 |

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 31 29 | 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | ~ | Rt6 | Ra6 | D6h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Exceptions:**

If the target register is R0 then this instruction will not cause an exception. Otherwise an exception may be caused by a data-bus error signal input or a TLB miss.

**Operation:**

Rt = mem[Ra + displacement]

**Exceptions:** DBE, DBG, LMT, TLB

### LWS – Load Word Special

**Description:**

A sixty-four bit value is loaded from memory and placed in the special purpose register. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

There is no indexed form for this instruction.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 8Eh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Spr = mem[Ra + displacement]

**Exceptions:** DBE, DBG, LMT, TLB

### LWX – Load Word Indexed

**Description:**

A sixty-four bit value is loaded from memory and placed in the target register. The memory address is the sum of register Ra and scaled register Rb. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | B6h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

Rt = mem[Ra + Rb\*scale]

**Exceptions:** DBE, DBG, LMT, TLB

### MAX - Register-Register

**Description:**

Determines the maximum of two values in registers Ra and Rb and places the result in the target register Rt.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 11h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

IF Ra < Rb

Rt = Rb

else

Rt = Ra

### MEMDB – Memory Data Barrier

**Description:**

All memory accesses before the MEMDB command are completed before any memory accesses after the data barrier are started. Note that this instruction has an effect even if the predicate is false; this does not affect the correct operation of the program, only performance is affected.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| F9h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** Memory

### MEMSB – Memory Synchronization Barrier

**Description:**

All instructions before the MEMSB command are completed before any memory access is started. Note that this instruction has an effect even if the predicate is false; this does not affect the correct operation of the program, only performance is affected.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| F8h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** Memory

### MFSPR – Special Register-Register

**Description:**

This instruction moves from a special purpose register into a general purpose one.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | Rt6 | Spr6 | A8h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Spr[n]

**Special Purpose Registers**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Reg # | R/W |  |  |  |
| 00-15 | RW | PRED | specific predicate register #0 to 15 |  |
| 16-31 | RW | CREGS | Code address register array (C0 to C15) |  |
| 32-39 | RW | SREGS | Segment base register array (zs,ds,es,fs,gs,hs,ss,cs) |  |
| 40-47 |  |  | * reserved for segmentation |  |
| 48 | R | MID | Machine ID |  |
| 49 | R | FEAT | Features |  |
| 50 | R | TICK | Tick count |  |
| 51 | RW | LC | Loop Counter |  |
| 52 | RW | PREGS | Predicate register array |  |
| 53 | RW | ASID | address space identifier |  |
| 59 | RW | EXC | exception cause register |  |
| 60 | W | BIR | Breakout index register |  |
| 61 | RW |  | Breakout register - additional spr’s |  |
| 63 |  |  | reserved |  |

Additional Spr’s are available by setting the breakout index register to an Sor index value, then accessing the Spr through the breakout register.

### MIN - Register-Register

**Description:**

Determines the minimum of two values in registers Ra and Rb and places the result in the target register Rt.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 10h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

IF Ra < Rb

Rt = Ra

else

Rt = Rb

### MLO – Mystery Logical Operation

**Description:**

The MLO instruction performs an operation that is determined at run-time as opposed to compile time. The operation to be performed is one of the register-register logical operations. Register Rc contains the function code for the operation. Registers Ra and Rb are the operands to the instruction. The result is placed in register Rt.

The MLO instruction is provided to help avoid writing self-modifying code for performance reasons.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Rt6 | Rc6 | Rb6 | Ra6 | 51h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra op(Rc) Rb

### MOV - Register-Register

**Description:**

This instruction moves one general purpose register to another. This instruction is shorter and uses one less register port than using the OR instruction to move between registers.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 04 | Rt6 | Ra6 | A78 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra

### MOVS – Move Special Register- Special Register

**Description:**

This instruction moves one special purpose register to another. The primary purpose of this instruction is to allow transfers directly between code address or segment registers.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | Sprt6 | Spr6 | AB8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Sprt = Spra

### MTSPR –Register-Special Register

**Description:**

Move a general purpose register into a special purpose register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| ~4 | Spr6 | Ra6 | A9h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Spr[n] = Ra

### MUL - Register-Register Multiply

**Description:**

Performs a signed multiply of two registers and places the product in the target register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 02h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 5

**Execution Units:** ALU #0 Only

**Operation:**

Rt = Ra \* Rb

### MULI - Register-Immediate Multiply

**Description:**

Performs a signed multiply of a register and an immediate value and places the result in a target register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Ah8 | Pn4 | Pc4 |

**Clock Cycles:** 5

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra \* immediate

### MULU – Unsigned Register-Register Multiply

**Description:**

Performs an unsigned multiply of two registers and places the product in the target register. This instruction will never cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 06h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 5

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra \* Rb

**Exceptions:** none

### MULUI – Unsigned Register-Immediate Multiply

**Description:**

Performs an unsigned multiply of a register and an immediate value and places the result in a target register. This instruction will never cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Eh8 | Pn4 | Pc4 |

**Clock Cycles:** 5

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra \* immediate

**Exceptions:** none

### MUX – Multiplex

**Description:**

If a bit in Ra is set then the bit of the target register is set to the corresponding bit in Rb, otherwise the bit in the target register is set to the corresponding bit in Rc.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Rt6 | Rc6 | Rb6 | Ra6 | 72h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

For n = 0 to 63

If Ra[n] is set then

Rt[n] = Rb[n]

else

Rt[n] = Rc[n]

**Exceptions:** none

### NAND - Register-Register

**Description:**

Bitwise and’s two registers inverts the result and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 03h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = ~(Ra & Rb)

**Exceptions:** none

### NEG - Negate Register

**Description:**

This instruction negates a register and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 14 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = - Ra

### NOP – No Operation

**Description:**

This instruction contains only a predicate byte. This is a single byte no-operation code. It can be used to align code addresses or as a fill byte.

The NOP operation is not queued by the processing core and is not present in the pipeline.

**Instruction Format:**

|  |  |
| --- | --- |
| 7 0 | |
| 14 | 04 |

**Two byte Format:**

|  |  |  |  |
| --- | --- | --- | --- |
| 18 8 | | 7 0 | |
| F4 | 14 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** None

**Operation:**

<none>

**Exceptions:** none

### NOR - Register-Register

**Description:**

Bitwise inclusively or two registers and place inverted result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 04h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = ~(Ra | Rb)

**Exceptions:** none

### NOT – Logical Not

**Description:**

This instruction performs a logical NOT on a register and places the result in a target register. If the value in a register is non-zero then the result is zero. If the value in the register is zero then the result is one. This instruction results in either a one or zero being placed in the target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 24 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = ! Ra

**Exceptions:** none

### OR - Register-Register

**Description:**

Bitwise inclusively or two registers and place the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 01h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra | Rb

**Exceptions:** none

### ORC – Or with Compliment

**Description:**

Bitwise inclusively or register Ra and the compliment of register Rb and place the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 07h6 | Rt6 | Rb6 | Ra6 | 50h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra | ~Rb

**Exceptions:** none

### ORI - Register-Immediate

**Description:**

Bitwise inclusively or register with immediate and place the result in the target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 54h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra | imm

**Exceptions:** none

### PAND – Predicate And

**Description:**

Bitwise and’s the specified predicate register bits and places the result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 06 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = Pr[Ra] & Pr[Rb]

**Exceptions:** none

### PANDC – Predicate And Compliment

**Description:**

Bitwise and’s the specified predicate register bits and places the result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 66 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = Pr[Ra] & ~Pr[Rb]

**Exceptions:** none

### PEOR – Predicate Exclusive Or

**Description:**

Bitwise exclusive or’s the specified predicate register bits and places the result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 26 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = Pr[Ra] ^ Pr[Rb]

**Exceptions:** none

### PENOR – Predicate Exclusive Nor

**Description:**

Bitwise exclusive or’s the specified predicate register bits and places the inverted result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 56 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = ~(Pr[Ra] ^ Pr[Rb])

**Exceptions:** none

### PNAND – Predicate Nand

**Description:**

Bitwise and’s the specified predicate register bits and places the inverted result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 36 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = ~( Pr[Ra] & Pr[Rb])

**Exceptions:** none

### POR – Predicate Or

**Description:**

Bitwise or’s the specified predicate register bits and places the result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 16 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = Pr[Ra] | Pr[Rb]

**Exceptions:** none

### PORC – Predicate Or Compliment

**Description:**

Bitwise or’s the specified predicate register bits and places the result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 76 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = Pr[Ra] | ~Pr[Rb]

**Exceptions:** none

### PNOR – Predicate Nor

**Description:**

Bitwise or’s the specified predicate register bits and places the inverted result in a target bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 46 | Bt6 | Bb6 | Ba6 | 42h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** AllALU’s

**Operation:**

Pr[Rt] = ~(Pr[Ra] | Pr[Rb])

**Exceptions:** none

### ROL – Rotate Left

**Description:**

Rotate register Ra left by Rb bits and place the result into register Rt. The most significant bit is shifted into the least significant bit. The rotation takes place modulo 64 of the value in register Rb (only the lower six bits of the register are used).

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 04h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << Rb

**Exceptions:** none

### ROLI – Rotate Left by Immediate

**Description:**

Rotate register Ra left by n bits and place the result into register Rt. The most significant bit is shifted into the least significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 14h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << #n

**Exceptions:** none

### ROR – Rotate Right

**Description:**

Rotate register Ra right by Rb bits and place the result into register Rt. The least significant bit is shifted into the most significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 05h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> Rb

**Exceptions:** none

### RORI – Rotate Right by Immediate

**Description:**

Rotate register Ra right by n bits and place the result into register Rt. The least significant bit is shifted into the most significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 15h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> #n

**Exceptions:** none

### RTD – Return from Debug Exception Routine

**Description:**

The program counter is loaded with the value contained in code address register #11 which is the DPC register. This instruction may cause the core to transition back to applications mode. It is only available while the core is in kernel mode.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| FCh8 | Pn4 | Pc4 |

**Operation:**

PC = Cr[11]

if (StatusEXL > 0) StatusEXL = StatusEXL - 1

**Exceptions:** PRIV

### RTE – Return from Exception Routine

**Description:**

The program counter is loaded with the value contained in code address register #13 which is the EPC register. This instruction may cause the core to transition back to applications mode. It is only available while the core is in kernel mode.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| F3h8 | Pn4 | Pc4 |

**Operation:**

PC = Cr[13]

if (StatusEXL > 0) StatusEXL = StatusEXL - 1

**Exceptions:** PRIV

### RTI – Return from Interrupt Routine

**Description:**

The program counter is loaded with the value contained in code address register #14 which is the IPC register. Additionally the interrupt mask is cleared to enable interrupts. This instruction will cause the core to transition back to applications mode. It is only available while the core is in kernel mode.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| F4h8 | Pn4 | Pc4 |

**Operation:**

pc = Cr[14]

Flags = FlagsBackup

Flags.im = 0

StatusHWI = 0

**Exceptions:** PRIV

### RTS – Return from Subroutine

**Description:**

The program counter is loaded with the value contained in the specified code address register plus a zero extended four bit immediate constant. The constant may not be extended. This allows the return instruction to return a few bytes past the usual return address. This is used to allow static parameters to be passed to the subroutine in inline code. The stack pointer may also be adjusted using the proper form of the RTS instruction for which the immediate constant must be a multiple of eight.

Note that the JMP instruction may also be used to return from a subroutine. Similarly this instruction may also be used to perform a jump to one of the first sixteen addresses relative to a code address register.

This instruction has a single byte short form that always executes when encountered. For the short form the program counter is loaded from code address register one.

**Instruction Formats:**

**Return past calling address**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| 23 20 | 19 16 | 15 8 | 7 0 | |
| Cr4 | Im4 | A3h8 | Pn4 | Pc4 |

**Stack pointer adjusting**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Immed8 | Cr4 | Im4 | F2h8 | Pn4 | Pc4 |

**Short Form:**

|  |  |
| --- | --- |
| 7 0 | |
| 14 | 14 |

**Execution Units:** All ALU’s / Branch

**Operation:**

PC = Cr[N] +Imm4

**Short Form Operation:**

PC = Cr[1] +Imm4

**Stack Pointer Adjust:**

PC = Cr[1] +Imm4

SP = SP + Imm

**Exceptions:** none

### SB – Store Byte

**Description:**

An eight bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended displacement and register Ra.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 90h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+offset] = Rb[7..0]

**Exceptions**: DBE, DBG, TLB, LMT

### SBX – Store Byte Indexed

**Description:**

An eight bit value is stored to memory from the source register Rc. The memory address is the sum of register Ra and Rb.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | C0h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+Rb] = Rb

**Exceptions**: DBE, DBG, TLB, LMT

### SC – Store Character

**Description:**

A sixteen bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 91h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+displacement] = Rb[15..0]

**Exceptions**: DBE, DBG, TLB, LMT

### SCX – Store Character Indexed

**Description:**

A sixteen bit value is stored to memory from the source register Rc. The memory address is the sum of register Ra and scaled register Rb. The memory address must be character aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | C1h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+Rb\*scale] = Rb

**Exceptions**: DBE, DBG, TLB, LMT

### SEI – Set Interrupt Mask

**Description:**

The interrupt mask is set, disabling maskable interrupts. This instruction is available only in kernel mode.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| FBh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Operation:**

im = 1

**Exceptions:** none

### SH – Store Half-word

**Description:**

A thirty-two bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | Displacement8..0 | Rb6 | Ra6 | 92h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra + displacement] = Rb[31..0]

**Exceptions**: DBE, DBG, TLB, LMT

### SHL – Shift Left

**Description:**

Shift register Ra left by Rb bits and place result into register Rt. A zero is shifted into the least significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 00h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << Rb

**Exceptions:** none

### SHLI – Shift Left by Immediate

**Description:**

Shift register Ra left by n bits and place result into register Rt. A zero is shifted into the least significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 10h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << #n

**Exceptions:** none

### SHLU – Shift Left Unsigned

**Description:**

Shift register Ra left by Rb bits and place the result into register Rt. A zero is shifted into the least significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 02h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << Rb

**Exceptions:** none

### SHLUI – Shift Left Unsigned by Immediate

**Description:**

Shift register Ra left by n bits and place the result into register Rt. A zero is shifted into the least significant bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 12h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra << #n

**Exceptions:** none

### SHR – Shift Right

**Description:**

Shift register Ra right by Rb bits and place result in register Rt. The sign bit is preserved.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 01h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> Rb

**Exceptions:** none

### SHRI – Shift Right by Immediate

**Description:**

Shift register Ra right by n bits and place result into register Rt. The sign bit is preserved.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 11h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> #n

**Exceptions:** none

### SHRU – Shift Right Unsigned

**Description:**

Shift register Ra right by register Rb bits. A zero is shifted into the sign bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 03h6 | Rt6 | Rb6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> Rb

**Exceptions:** none

### SHRUI – Shift Right Unsigned by Immediate

**Description:**

Shift register Ra right by n bits and place result into register Rt. A zero is shifted into the sign bit.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 13h6 | Rt6 | Imm6 | Ra6 | 58h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra >> #n

**Exceptions:** none

### SHX – Store Half-word Indexed

**Description:**

A thirty-two bit value is stored to memory from the source register Rb. The memory address is the sum of register Ra and scaled register Rb. The memory address must be half-word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | C2h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+Rb] = Rb

**Exceptions**: DBE, DBG, TLB, LMT

### STCMP – String Compare

**Description:**

This instruction compares data from the memory location addressed by Ra plus Rc to the memory location addressed by Rb plus Rc until the loop counter LC reaches zero or until a mismatch occurs. Rc acts as an index and increments or decrements by the size of the operation as the move takes place. This instruction is interruptible. The data must be in the same segment and appropriately aligned. The loop counter is set to zero when a mismatch occurs. The index of the mismatch is contained in register Rc.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 37 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | O3 | Rc6 | Rb6 | Ra6 | 9Ah8 | Pn4 | Pc4 |

|  |  |  |
| --- | --- | --- |
| O3 | Assembler Mnemonic |  |
| 0 | STCMP.BI | bytes incrementing |
| 1 | STCMP.CI | characters incrementing |
| 2 | STCMP.HI | half-word incrementing |
| 3 | STCMP.WI | words incrementing |
| 4 | STCMP.BD | bytes decrementing |
| 5 | STCMP.CD | characters decrementing |
| 6 | STCMP.HD | half-word decrementing |
| 7 | STCMP.WD | word decrementing |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Rb + Rc] = mem[Ra + Rc]

Rc = Rc +/- amt

LC = LC – 1

### STFND – String Find

**Description:**

This instruction compares data from the memory location addressed by Ra plus Rc to the data in register Rb until the loop counter LC reaches zero or until a match occurs. Rc acts as an index and increments or decrements by the size of the operation as the move takes place. This instruction is interruptible. The data must be appropriately aligned. The loop counter is set to zero when a match occurs. The index of the match is contained in register Rc.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 37 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | O3 | Rc6 | Rb6 | Ra6 | 9Bh8 | Pn4 | Pc4 |

|  |  |  |
| --- | --- | --- |
| O3 | Assembler Mnemonic |  |
| 0 | STFNDBI | bytes incrementing |
| 1 | SFNDCI | characters incrementing |
| 2 | STFNDHI | half-word incrementing |
| 3 | STFNDWI | words incrementing |
| 4 | STFNDBD | bytes decrementing |
| 5 | STFNDCD | characters decrementing |
| 6 | STFNDHD | half-word decrementing |
| 7 | STFNDWD | word decrementing |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

if (mem[Ra + Rc] = Rb)

stop

Rc = Rc +/- amt

LC = LC – 1

### STI – Store Immediate

**Description:**

A six bit value is zero extended to sixty-four bits and stored to memory. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | Displacement8..0 | Imm6 | Ra6 | 96h8 | Pn4 | Pc4 |

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra + displacement] = zero extend (Imm[5..0])

### STIX – Store Immediate Indexed

**Description:**

A ten bit value is zero extended to sixty-four bits and stored to memory. The memory address is the sum of register Ra and scaled register Rb. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 36 | 35 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Imm9..6 | Sc2 | Imm5..0 | Rb6 | Ra6 | C6h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra + Rb \* scale] = zero extend (Imm[9..0])

### STMOV – String Move

**Description:**

This instruction moves a data from the memory location addressed by Ra plus Rc to the memory location addressed by Rb plus Rc until the loop counter LC reaches zero. Rc acts as an index and increments or decrements by the size of the operation as the move takes place. This instruction is interruptible. The data moved must be in the same segment and appropriately aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 37 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | O3 | Rc6 | Rb6 | Ra6 | 99h8 | Pn4 | Pc4 |

|  |  |  |
| --- | --- | --- |
| O3 | Assembler Mnemonic |  |
| 0 | STMOV.BI | move bytes incrementing |
| 1 | STMOV.CI | move characters incrementing |
| 2 | STMOV.HI | move half-word incrementing |
| 3 | STMOV.WI | move words incrementing |
| 4 | STMOV.BD | move bytes decrementing |
| 5 | STMOV.CD | move characters decrementing |
| 6 | STMOV.HD | move half-word decrementing |
| 7 | STMOV.WD | move word decrementing |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Rb + Rc] = mem[Ra + Rc]

Rc = Rc +/- amt

LC = LC – 1

### STP – Stop / Slow Down

**Description:**

This instruction controls the core clock rate which affects power consumption. The immediate constant is loaded into a shift register that controls the frequency of clock pulses seen by the processor. Setting the constant to FFFFh provides the maximum clock rate. Setting the constant to zero stops the clock completely. With the clock stopped completely the core must be reset or an NMI interrupt must occur before the core will continue processing. After reset or NMI the core begins processing at a half the maximum clock rate.

**Instruction Format:**

|  |  |  |  |
| --- | --- | --- | --- |
| 31 16 | 15 8 | 7 0 | |
| Immediate16 | F6h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra[31:0]

**Typical Values For Shift Register**

|  |  |
| --- | --- |
| Value |  |
| 0000 | Stop clock completely |
| 8888 | 25% rate |
| AAAA | 50% rate |
| EEEE | 75% rate |
| FFFF | Full power, max clock rate |
|  |  |

**Exceptions:** none

### STSB – Store String Byte

**Description:**

This instruction stores a byte contained in register Rb to consecutive memory locations beginning at the address in Ra until the loop counter LC reaches zero. Ra is updated with by the number of bytes written. This instruction is interruptible.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | 03 | ~6 | Rb6 | Ra6 | 98h8 | Pn4 | Pc4 |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Ra] = Rb[7:0]

Ra = Ra + 1

LC = LC – 1

### STSC – Store String Character

**Description:**

This instruction stores a character (16 bit value) to consecutive memory locations beginning at the address in Ra until the loop counter reaches zero. The memory address must be character aligned. Ra is updated by the number of bytes written. This instruction is interruptible.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | 13 | ~6 | Rb6 | Ra6 | 98h8 | Pn4 | Pc4 |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Ra] = Rb[15:0]

Ra =Ra+ 2

LC = LC – 1

### STSET – String Set

**Description:**

This instruction stores data contained in register Rb to consecutive memory locations beginning at the address in Ra until the loop counter LC reaches zero. Ra is updated with by the number of bytes written. This instruction is interruptible. The data address must be appropriately aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | 03 | ~6 | Rb6 | Ra6 | 98h8 | Pn4 | Pc4 |

**Execution Units:** Memory

**Operation:**

while LC <> 0

mem[Ra] = Rb

Ra = Ra +/- amt

LC = LC – 1

|  |  |  |
| --- | --- | --- |
| O3 | Assembler Mnemonic |  |
| 0 | STSET.BI | set bytes incrementing |
| 1 | STSET.CI | set characters incrementing |
| 2 | STSET.HI | set half-word incrementing |
| 3 | STSET.WI | set words incrementing |
| 4 | STSET.BD | set bytes decrementing |
| 5 | STSET.CD | set characters decrementing |
| 6 | STSET.HD | set half-word decrementing |
| 7 | STSET.WD | set word decrementing |

### STSH – Store String Half-word

**Description:**

This instruction stores a half-word (32 bit value) to consecutive memory locations beginning at the address in Ra until the loop counter reaches zero. The memory address must be half-word aligned. Ra is updated by the number of bytes written. This instruction is interruptible.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | 23 | ~6 | Rb6 | Ra6 | 98h8 | Pn4 | Pc4 |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Ra] = Rb[31:0]

Ra =Ra + 4

LC = LC – 1

### STSW – Store String Word

**Description:**

This instruction stores a word (64 bit value) to consecutive memory locations beginning at the address in Ra until the loop counter reaches zero. The memory address must be half-word aligned. Ra is updated by the number of bytes written. This instruction is interruptible.

**Instruction Format:**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| 39 34 | | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | 33 | ~6 | Rb6 | Ra6 | 98h8 | Pn4 | Pc4 |

**Execution Units:** Memory

**Operation:**

temp = 0

while LC <> 0

mem[Ra] = Rb[63:0]

Ra =Ra + 8

LC = LC – 1

### SUB - Register-Register

**Description:**

This instruction subtracts one register from another and places the result into a third register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 01h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra - Rb

### SUBI - Register-Immediate

**Description:**

This instruction subtracts an immediate value from a register and places the result into a register. This instruction may cause an overflow exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 49h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra – Imm

### SUBU - Register-Register

**Description:**

This instruction subtracts one register from another and places the result into a third register. This instruction never causes an exception.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 39 34 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| 05h6 | Rt6 | Rb6 | Ra6 | 40h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra - Rb

### SUBUI - Register-Immediate

**Description:**

This instruction subtracts an immediate value from a register and places the result into a register. This instruction never causes an exception.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 39 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Immediate11..0 | Rt6 | Ra6 | 4Dh8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** All ALU’s

**Operation:**

Rt = Ra – Imm

### SW – Store Word

**Description:**

A sixty-four bit value is stored to memory from the source register Rb. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rt6 | Ra6 | 93h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+offset] = Rb

**Exceptions**: DBE, DBG, TLB, LMT

### SWCR – Store Word and Clear Reservation

**Description:**

If there is a reservation present on the memory address then a sixty-four bit value is stored to memory from the source register Rs and the reservation is cleared. If there is no reservation present then memory is not updated. If the update was successful then predicate register zero is set to ‘ne’ status, otherwise the predicate register is set to ‘eq’ status. The memory address is the sum of the sign extended offset and register Ra. The memory address must be word aligned. This instruction relies on the memory system for implementation.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Rs6 | Ra6 | 8Ch8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+offset] = Rb, reservation cleared

**Exceptions**: DBE, DBG, TLB, LMT

### SWS – Store Word Special

**Description:**

A sixty-four bit value is stored to memory from the source special purpose register Spr. The memory address is the sum of the sign extended displacement and register Ra. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3937 | 36 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Sg3 | Displacement8..0 | Spr6 | Ra6 | 9Eh8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra + displacement] = Spr

**Exceptions**: DBE, DBG, TLB, LMT

### SWX – Store Word Indexed

**Description:**

A sixty-four bit value is stored to memory from the source register Rc. The memory address is the sum of register Ra and scaled register Rb. The memory address must be word aligned.

**Instruction Format:**

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| 39 37 | 36 | 3534 | 33 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| Seg3 | ~ | Sc2 | Rc6 | Rb6 | Ra6 | C3h8 | Pn4 | Pc4 |

**Clock Cycles:** 3 (one memory access)

**Execution Units:** All ALU’s / Memory

**Operation:**

memory[Ra+Rb] = Rc

**Exceptions**: DBE, DBG, TLB, LMT

### SXB – Sign Extend Byte

**Description:**

This instruction sign extends a register from bit 8 to 63 and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| C4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = {56{Ra[7]}},Ra[7:0]

**Exceptions:** none

### SXC – Sign Extend Character

**Description:**

This instruction sign extends a register from bit 16 to 63 and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| D4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = {48{Ra[15]}},Ra[15:0]

**Exceptions:** none

### SXH – Sign Extend Half-word

**Description:**

This instruction sign extends a register from bit 32 to 63 and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| E4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = {32{Ra[31]}},Ra[31:0]

**Exceptions:** none

### SYNC – Synchronization Barrier

**Description:**

All instructions before the SYNC command are completed before any following instructions are started. Note that this instruction has an effect even if the predicate is false; this does not affect the correct operation of the program, only performance is affected.

**Instruction Format:**

|  |  |  |
| --- | --- | --- |
| 15 8 | 7 0 | |
| F7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Exceptions:** none

### SYS –Call system routine

**Description:**

This instruction calls a system function located as the sum of the offset times 16 plus code address register 12. The return address is stored in the EPC register (code address register #13). This instruction causes the core to switch to kernel mode.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 24 | 23 20 | 19 16 | 15 8 | 7 0 | |
| Offset7..0 | Ch4 | Dh4 | A5h8 | Pn4 | Pc4 |

**Operation**:

PC = offset \* 16 + c12

if (StatusEXL < 255) StatusEXL = StatusEXL + 1

### TLB – TLB Command

**Description:**

The command is executed on the TLB unit. The command results are placed in internal TLB registers which can be read or written using TLB command instruction. If the operation is a read register operation then the register value is placed into Rt. If the operation is a write register operation, then the value for the register comes from Rb. Otherwise the Rb/Rt field in the instruction is ignored.

This instruction is only available in kernel mode.

**Instruction Format:**

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| 3130 | 29 24 | 23 16 | | 15 8 | 7 0 | |
| ~2 | Rb/Rt6 | Tn4 | Cmd4 | F0h8 | Pn4 | Pc4 |

**Clock Cycles:** 3

Tn4 – This field identifies which TLB register is being read or written.

|  |  |  |
| --- | --- | --- |
| Reg no. |  | Assembler |
| 0 | Wired | Wired |
| 1 | Index | Index |
| 2 | Random | Random |
| 3 | Page Size | PageSize |
| 4 | Virtual page | VirtPage |
| 5 | Physical page | PhysPage |
| 7 | ASID | ASID |
| 8 | Data miss address | DMA |
| 9 | Instruction miss address | IMA |
| 10 | Page Table Address | PTA |
| 11 | Page Table Control | PTC |

**TLB Commands**

|  |  |  |
| --- | --- | --- |
| Cmd | Description | Assembler |
| 0 | No operation |  |
| 1 | Probe TLB entry | TLBPB |
| 2 | Read TLB entry | TLBRD |
| 3 | Write TLB entry corresponding to random register | TLBWR |
| 4 | Write TLB entry corresponding to index register | TLBWI |
| 5 | Enable TLB | TLBEN |
| 6 | Disable TLB | TLBDIS |
| 7 | Read register | TLBRDREG |
| 8 | Write register | TLBWRREG |
| 9 | Invalidate all entries | TLBINV |

Probe TLB – The TLB will be tested to see if an address translation is present.

Read TLB – The TLB entry specified in the index register will be copied to TLB holding registers.

Write Random TLB – A random TLB entry will be written into from the TLB holding registers.

Write Indexed TLB – The TLB entry specified by the index register will be written from the TLB holding registers.

Disable TLB – TLB address translation is disabled so that the physical address will match the supplied virtual address.

Enable TLB – TLB address translation is enabled. Virtual address will be translated to physical addresses using the TLB lookup tables.

The TLB will automatically update the miss address registers when a TLB miss occurs only if the registers are zero to begin with. System software must reset the registers to zero after a miss is processed. This mechanism ensures the first miss that occurs is the one that is recorded by the TLB.

PageTableAddr – This is a scratchpad register available for use to store the address of the page table.

PageTableCtrl – This is a scratchpad register available for use to store control information associated with the page table.

### TST - Register Test Compare

**Description:**

The register test compare compares a register against the value zero and sets the predicate flags appropriately.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 2322 | 21 16 | 15 12 | 11 8 | 7 0 | |
| 02 | Ra6 | 04 | Pt4 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Operation:**

if Ra < 0

Pt.lt = 1

else

Pt.lt = 0

if Ra = 0

Pt.eq = 1

else

Pt.eq = 0

Pt.ltu = 0

**Exceptions:** none

### ZXB – Zero Extend Byte

**Description:**

This instruction zero extends a register from bit 8 to 63 and places the result in a target register. This instruction is typically used to perform an unsigned load operation with the LVB instruction.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| C4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra[7:0]

**Exceptions:** none

### ZXC – Zero Extend Character

**Description:**

This instruction zero extends a register from bit 16 to 63 and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| D4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra[15:0]

**Exceptions:** none

### ZXH – Zero Extend Half-word

**Description:**

This instruction zero extends a register from bit 32 to 63 and places the result in a target register.

**Instruction Format:**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| 31 28 | 27 22 | 21 16 | 15 8 | 7 0 | |
| E4 | Rt6 | Ra6 | A7h8 | Pn4 | Pc4 |

**Clock Cycles:** 1

**Execution Units:** ALU #0 only

**Operation:**

Rt = Ra[31:0]

**Exceptions:** none

## Opcode Map

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | TST / FTST / FSTST | | | | | | | | | | | | | | | |
| 1x | CMP / FCMP / FSCMP | | | | | | | | | | | | | | | |
| 2x | CMPI | | | | | | | | | | | | | | | |
| 3x | BR | | | | | | | | | | | | | | | |
| 4x | {RR} | {R} | {P} |  |  |  | BITI | ADDUI | ADDI | SUBI | MULI | DIVI | ADDUI | SUBUI | MULUI | DIVUI |
| 5x | {logic} | MLO |  | ANDI | ORI | EORI |  |  | {shift} |  |  |  |  |  |  |  |
| 6x |  |  |  |  |  |  |  |  |  |  |  | \_2ADDUI | \_4ADDUI | \_8ADDUI | \_16ADDUI | LDI |
| 7x | NEG | NOT | MUX |  |  |  | {FMAC} | {double r} | {float rr} | {single r} |  |  |  |  |  |  |
| 8x | LB | LBU | LC | LCU | LH | LHU | LW | LFS | LFD |  |  | LVWAR | SWCR | LEA | LWS | LCL |
| 9x | SB | SC | SH | SW | SFS | SFD | STI | CAS | STSET | STMOV | STCMP | STFND |  | LDIS | SWS | CACHE |
| Ax | JSR | JSR | JSR | RTS | LOOP | SYS | INT | {R} | MFSPR | MTSPR | {bitfld} | MOVS | LVB | LVC | LVH | LVW |
| Bx | LBX | LBUX | LCX | LCUX | LHX | LHUX | LWX |  |  |  |  |  |  |  |  |  |
| Cx | SBX | SCX | SHX | SWX |  |  | STIX | INC | PUSH | PEA | POP | LINK | UNLINK |  |  |  |
| Dx |  |  |  |  |  |  | LW |  |  |  |  |  |  |  |  |  |
| Ex |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Fx | {TLB} | NOP | RTS | RTE | RTI | {BCD} | STP | SYNC | MEMSB | MEMDB | CLI | SEI | RTD |  |  | IMM |

40 - {RR} Opcodes –Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | ADD | SUB | MUL | DIV | ADDU | SUBU | MULU | DIVU | 2ADDU | 4ADDU | 8ADDU | 16ADDU |  |  |  |  |
| 1x | MIN | MAX |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

50 - {logic} Opcodes – Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | AND | OR | EOR | NAND | NOR | ENOR | ANDC | ORC |  |  |  |  |  |  |  |  |
| 1x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

F5 {BCD} Opcodes – Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | BCDADD | BCDSUB | BCDMUL |  |  |  |  |  |  |  |  |  |  |  |  |  |

78 - {float -rr} Opcodes –Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x |  |  |  |  |  |  |  | FCMP | FADD | FSUB | FMUL | FDIV |  |  |  |  |
| 1x |  |  |  |  |  |  |  | FCMPS | FADDS | FSUBS | FMULS | FDIVS |  |  |  |  |
| 2x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

77 - Double {R} Opcodes – Func4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | FMOV |  | FTOI | ITOF | FNEG | FABS | FSIGN | FMAN | FNABS |  |  |  | FSTAT | FRM |  |  |

79 - Single {R} Opcodes – Func4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | FMOVS |  | FTOIS | ITOFS | FNEGS | FABSS | FSIGNS | FMANS | FNABSS |  |  |  | FTX | FCX | FEX | FDX |

A7 {R} Opcodes – Func4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | MOV | NEG | NOT | ABS | SGN | CNTLZ | CNTLO | CNTPOP | SXB | SXC | SXH | COM | ZXB | ZXC | ZXH |  |

41 {R} Opcodes – Func4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | CPUID | REDOR | REDAND | PAR |  |  |  |  |  |  |  |  |  |  |  |  |

42 - {Predicate Logic} Opcodes – Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | PAND | POR | PEOR | PNAND | PNOR | PENOR | PANDC | PORC |  |  |  |  |  |  |  |  |
| 1x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 2x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

58 - {shift} Opcodes – Func6

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | SHL | SHR | SHLU | SHRU | ROL | ROR |  |  |  |  |  |  |  |  |  |  |
| 1x | SHLI | SHRI | SHLUI | SHRUI | ROLI | RORI |  |  |  |  |  |  |  |  |  |  |
| 2x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| 3x |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |

AA {Bitfield} Opcodes – Func4

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  | x0 | x1 | x2 | x3 | x4 | x5 | x6 | x7 | x8 | x9 | xA | xB | xC | xD | xE | xF |
| 0x | BFINS | BFSET | BFCLR | BFCHG | BFEXTU | BFEXT | BFINSI |  |  |  |  |  |  |  |  |  |