# ds1626io

## Clocks:

The ds1626io module requires only a single clock source for the WISHBONE bus interface. The ds1626io module derives the clock to the ds1626 from the bus clock clk\_i. The clock high and low times are calculated based on a frequency parameter (pClkFreq) passed to the core when the core is instanced.

## Addressing:

The ds1626io module responds to the word address range: $FFDC03xx.

## Registers:

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Regno | Width | R/W | Description |  |
| 0 | 16 | R/W | Bits [7:0] = command byte for ds1626 |  |
| 1 | 16 | R/W | Bits [11:0] = data to ds1626 or response data from ds1626  Bit [15] = transfer busy status. |  |
|  |  |  |  |  |

## Operation:

Set the data register with any data going to the ds1626 prior to setting the command register. Placing a value in the command register triggers a transfer of both the command and data to the ds1626. The status of the transfer can be determined by polling the data register and checking bit #15. Note that writes to the controller will be ignored while a transfer is taking place. For READ\_ commands the response data is placed back into the data register.

# I/O Ports

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Name | Wid | I/O | Description |  |
| rst\_i | 1 | I | This is the active high reset signal |  |
| clk\_i | 1 | I | system bus clock |  |
| cyc\_i | 1 | I | cycle active |  |
| stb\_i | 1 | I | data strobe |  |
| ack\_o | 1 | O | data transfer acknowledge |  |
| we\_i | 1 | I | write cycle |  |
|  |  |  |  |  |
| adr\_i | 34 | I | decode / register address |  |
| dat\_i | 16 | I | data input |  |
| dat\_o | 16 | O | data output |  |
|  |  |  |  |  |
| rst1626 | 1 | O | This is the reset line going to the ds1626 |  |
| clk1626 | 1 | O | This is the clock signal to the ds1626. |  |
| d1626 | 1 | I | This is data input from the ds1626. This line must be combined with the data output line via a tri-state multiplex controlled by en1626. |  |
| q1626 | 1 | O | This is the data output to the ds1626. This line must be combined with the data input line via a tri-state multiplex controlled by the en1626. |  |
| en1626 | 1 | O | This signal is provided to enable the data output line onto a tri-state buffer driving the ds1626’s dq signal. |  |
|  |  |  |  |  |

## Parameters:

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Default Value | Description |  |
| pClkFreq | 50000000 | This parameter tells the core the WISHBONE bus operating frequency. It is specified as a whole number. Eg. 25000000 means 25MHz. This parameter is used to compute the clock  frequency to the ds1626. |  |
| pTmpNumber | 0 | This identifies which temperature controller is present. There may be up to  16 controllers within the address range. |  |

# WISHBONE Compatibility Datasheet

The DS1626 core may be directly interfaced to a WISHBONE compatible bus.

|  |  |  |
| --- | --- | --- |
| WISHBONE Datasheet  WISHBONE SoC Architecture Specification, Revision B.3 | | |
|  |  | |
| Description: | Specifications: | |
| General Description: | DS1626 Controller | |
| Supported Cycles: | SLAVE, READ / WRITE  SLAVE, BLOCK READ / WRITE  SLAVE, RMW | |
| Data port, size:  Data port, granularity:  Data port, maximum operand size:  Data transfer ordering:  Data transfer sequencing | 16 bit  16 bit  16 bit  Little Endian  any (undefined) | |
| Clock frequency constraints: |  | |
| Supported signal list and cross reference to equivalent WISHBONE signals | Signal Name:  ack\_o  adr\_i(33:0)  clk\_i  dat\_i(15:0)  dat\_o(15:0)  cyc\_i  stb\_i  we\_i | WISHBONE Equiv.  ACK\_O  ADR\_I()  CLK\_I  DAT\_I()  DAT\_O()  CYC\_I  STB\_I  WE\_I |
| Special Requirements: |  | |