OSI_FPGA

Users Guide

Version 10-11-06

General Information

This is the first public alpha release of OSI_FPGA implemented in a Xilinx Spartan 3 FPGA. The FPGA is part of the Spartan 3 Starter board built by Digilent Inc. OSI_FPGA is an implementation of an Ohio Scientific Inc. (OSI) Superboard II / C1P. It is not an accurate implementation. The 32x32 character monochrome video has been modified to display 64 columns x 32 lines of characters. Also, the monochrome video has been extended to include a superset of the model 540 color. The tape interface has been replaced with a standard RS232 serial port. The original monitor ROM has been replaced with a custom monitor based on the CEGMON ROM code.

Processor

The 6502 processor core was written by Daniel Wallner. It implements all 6502 instructions and is cycle accurate to the original 6502. The processor is clocked at the standard speed of 1.0 MHz. There are three non-standard speeds supported, 4.17, 12.5 and 25 MHz. There are switches that control the speed. See Buttons and Switches for the settings.

Memory

The main memory for OSI_FPGA uses 40K of the 1Meg of SRAM built onto the Digilent board. The 8K BASIC in ROM is implemented using the Spartan 3 block RAM and has been write protected to prevent being overwritten. This Block RAM is initialized as part of the FPGA. The 2K CEGMON based monitor ROM is implemented the same way. The 2K video RAM, 2K video color RAM, and 2K video character generator ROM uses the same type of block RAM, but is configured in dual port mode. The processor reading and writing the video memory does not interfere with the video circuitry reading from the same memory.

Video

The video is configured to be 64 columns and 32 lines of characters. This is not standard for the Superboard II / C1P. But it is standard for the540 video board in the C4P and C8P systems. This extension makes it incompatible with some Superboard / C1P software, games, that write directly to the video memory. The 540 video board includes four bits of color information. OSI_FPGA includes a superset of this color information. The color attributes are listed below.

Bits	Attribute
0	Inverse Video
1	Red

2	Blue
3	Green
4	Blink
5	Background Red
6	Background Green
7	Background Blue

The displayed color is user selectable. Writing the desired character color into the USER COLOR memory location will change the colors used to display all subsequent characters. OSI_FPGA uses a VGA monitor to display the video. Each character is an 8 x 8 pixel matrix. This gives a pixel resolution of 512 x 256. OSI_FPGA displays this matrix on a 1024 x 768 VGA screen resolution. Each horizontal pixel is displayed using two screen resolution pixels. This converts a 512 pixel line to 1024 screen pixel line. Each horizontal line is displayed three times. This converts the 256 lines to 768 screen lines.

The Superboard / C1P used a character generator ROM to hold the character set. This limited the video to 256 predetermined characters. OSI_FPGA maps the character generator into the memory map where it can be modified. The maximum number of character is still 256, but the character set is not fixed. A RESET will not force the character set to revert back to the original set. This will require the FPGA be reloaded.

Keyboard

The keyboard on the Superboard / C1P was an 8 row by 8 column switch matrix. OSI_FPGA uses a PS2 keyboard. The scan codes from the keyboard are translated to keys in the matrix. Some keys on the original keyboard had different shifted characters than the PS2 keyboard. OSI_FPGA does not translate these differences. Because of this some keys are labeled differently than read from the keyboard*. These differences are listed below.

Unshifted character	PS2 Shifted character	OSI Shifted character
2	@	“
6	^	&
7	&	‘
8	*	(
9	(	)
0	)	None
-	_	=
;	:	+

The OSI monitor uses a software debounce / repeat algorithm. This algorithm filters out bounce in the switches when the key is pushed or released. It is also responsible for repeating entered characters when the key is held. This algorithm works acceptable when the CPU speed is set at 1 or 4.17 MHz. But then the upper speeds are selected, the algorithm fails. This makes the keyboard unusable at those speeds*.

* The keyboard differencies and the debounce / repeat key issue have been fixed in a modified version of the CEGMON monitor. The CERMON monitor controls the keyboard layout. The CEGMON also controls the debounce / repeat feature of the keyboard. But since the monitor does not know the speed of the CPU, a time base is needed. OSI_FPGA includes a time base that is generated independently of the CPU speed.

Memory Map

0000-9FFF	40K RAM
A000-BFFF	OSI 8K BASIC in ROM
C000-C7FF	2K Video character generator
C800-CFFF	2K tape utility
D000-D7FF	2K Video memory
D800-DEFF	2K-256 TBD
DF00	Keyboard
DF0A	USER COLOR
DF0B	ROM_WR_EN
DF10-DF16	Debounce timer / RTC
E000-E7FF	2K Video Color memory
E800-EFFF	2K Extended Monitor / Disassembler
F000-F001	6850 UART (Tape Interface)
F002-F7FF	2K-2 TBD
F800-FFFF	Monitor

Buttons and Switches

Switch 0-1	CPU Speed
0 0	1 MHz
0 1	4.17 MHz
1 0	12.5 MHz
1 1	25 MHz
Switch 2-3	6850 UART Baud rate

0 0	300 bps
0 1	600 bps
1 0	1200 bps
1 1	9600 bps
Switch 4-5	TBD
Switch 6	Stop
Switch 7	TBD
Button 0-2	TBD
Button 3	RESET