

TRANSFER UNIT

The circuit diagram illustrates a Transfer Unit for a Turing Machine, featuring a central logic core and three peripheral components: a Pulse Generator, a Sending Dekatron, and a Receiving Dekatron.

Central Logic Core:

- IC1A (74LS73N):** A J-K flip-flop with inputs J (pin 14), K (pin 3), and CLK (pin 2). Its outputs Q (pin 12) and \bar{Q} (pin 13) are connected to LEDs LED2 and LED3, respectively, through 330R resistors (R2, R3).
- IC1B (74LS73N):** A J-K flip-flop with inputs J (pin 7), K (pin 10), and CLK (pin 5). Its outputs Q (pin 9) and \bar{Q} (pin 8) are connected to a 330R resistor (R1) and a LED1, respectively.
- IC2C (74S08N):** An AND gate with inputs 9 and 10, and output 8 (labeled COMP).
- IC2D (74S08N):** An AND gate with inputs 12 and 13, and output 11 (labeled ADD).

Peripheral Components:

- Pulse Generator (JP3):** A 10-pin component providing RESET, 10A PULSES, and COMPLEMENT PULSES signals.
- Sending Dekatron (JP1):** A 10-pin component providing VDD and VSS connections.
- Receiving Dekatron (JP2):** A 10-pin component providing VDD and VSS connections.

Control and Output Signals:

- RESET:** A signal line connecting the RESET inputs of IC1A and IC1B.
- ZC(ZERO CATHODE):** A signal line connecting the CLK input of IC1A.
- CL(CLEAR SEND):** A signal line connecting the CLK input of IC1B.
- ADD:** The output of IC2D, connected to pin 1 of JP2.
- COMP:** The output of IC2C, connected to pin 2 of JP2.
- TRANSFER PULSES:** A signal line connecting the output of IC1A (pin 12) to pin 3 of JP2.

Power and Grounding:

- VDD:** The positive supply voltage, connected to pins 1, 5, 7, 9, 11, 13, and 14.
- VSS:** The ground connection, connected to pins 2, 3, 4, 6, 8, 10, 12, and 13.

Capacitors:

- C1, C2, C4, C5:** Capacitors connected to the VDD and VSS lines.
- C3:** A capacitor connected to the output of IC1A (pin 12).