**Project: 4**

**FIR Filter**

**Course: EN605.715**

**Date: 10/09/2019**

**Principal Investigator: Zach Richard**

**Requirements:**

The requirements we derived for this project were to use two instances of the Xilinx FIR Compiler IP Core to create a low-pass filter which passes frequencies below 18KHz and attenuates frequencies above 30KHz.

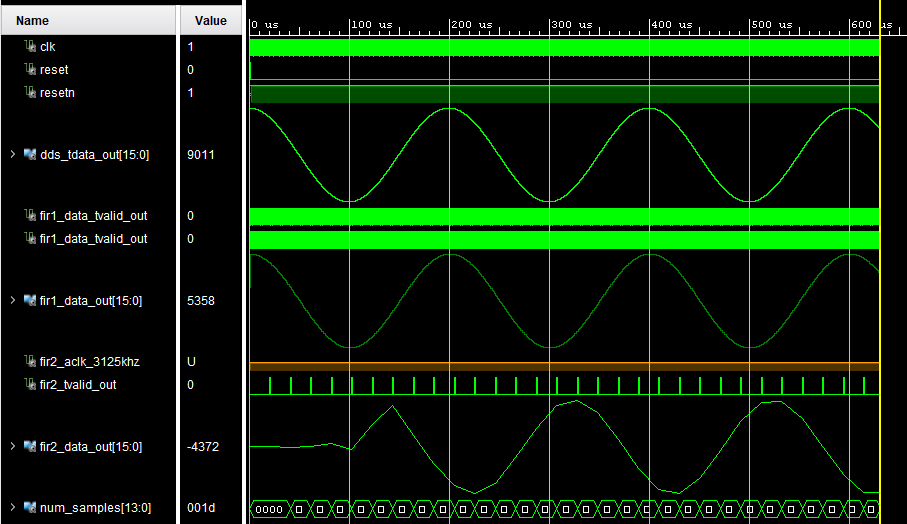
**Equipment Used:**

* Digilent Zedboard
* various micro USB cables
* any headphones around
* Xilinx Vivado 2017.4
* Ryzen 3900X Development PC running Windows 10

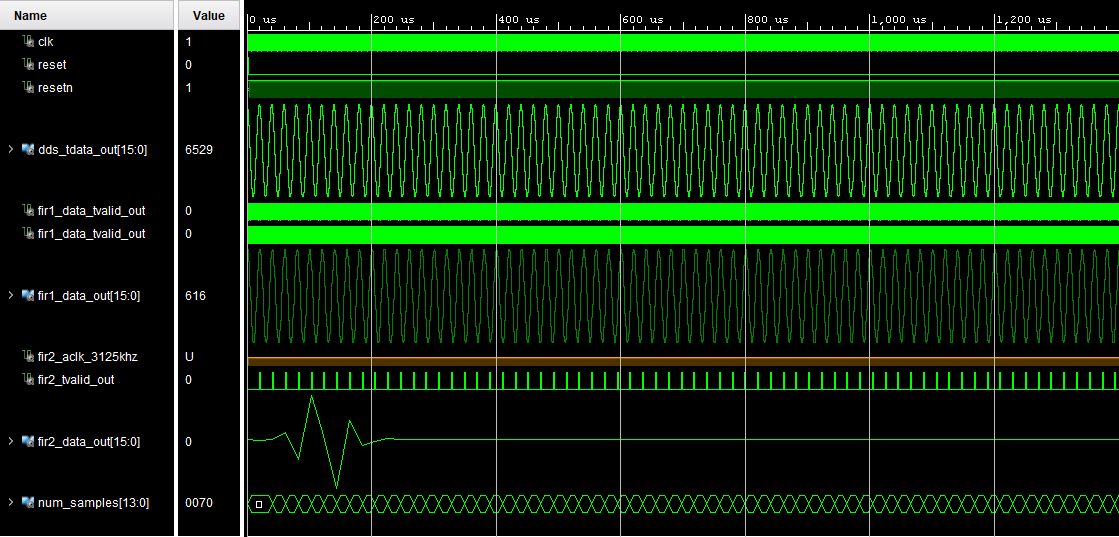
**Data Captured**

I used a methodology similar to Lab 3 to capture the output data from the second filter from my testbed simulation.

5KHz Filter Response



50KHz Filter Response



**Calculated Metrics**

Attenuation = 20\*log10(A1/A2)

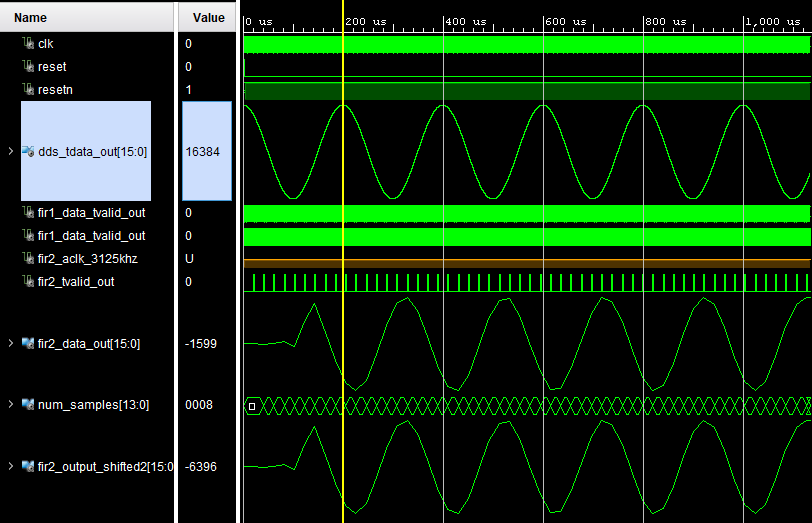
A1 = 4562

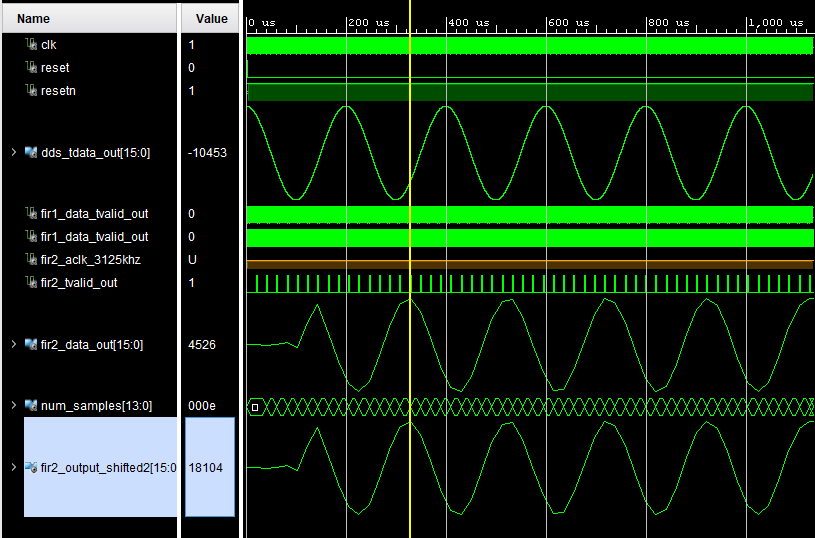
A2 = 1

Attenuation = 73.18dbA

**Calculated Metrics (cont.)**

Unity Gain





Unity Gain Calculation

20\*log10(A1/A2)

A1 Unfiltered Signal = 16384

Filtered Signal= 4526

A2 Filtered Signal Left Shifted 2 bits= 18104

Gain = 0.867

Since the filtered output’s amplitude was lower by a factor of 4, a simple 2 bit left shift seemed appropriate to restore gain.