Digital Logic

CS207 Assignment 4: Theory

Assignment is pledged that you have neither given nor received unauthorized help. All course work should be completed entirely on your own. Students who commit an act of academic dishonesty may receive a zero on the assignment or in the course.

Due on 23:55, Dec. 20, 2022

南方科技大学

SOUTHERN UNIVERSITY OF SCIENCE AND TECHNOLOGY

Assignment Notes

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- Write neatly according to the answer template and submit an e-copy to Sakai on time.
  - You can finish the theory questions on a paper, scan it and paste into the template.
- Do write down all procedures. Only presenting the final answer will lead to a zero, even the answer is correct.
- Do double-check your submitted file. No re-submission is allowed for student reasons, e.g., corrupted file uploaded.
- Box answers when applicable.
- Draw logic diagrams with a pen or any software applicable.
- Turn assignments in early if possible.
- This document accounts for 100% of the assignment.
- Request to regrade will lead to a complete regrade on all questions in the assignment. Final grades may increase or decrease.

Question 1

- (10 points) Implement a full adder with two 4×1 multiplexers. Draw the logic diagram.

Question 2

- (10 points) Design a sequence generator to generate the sequence 110101. Draw the logic diagram.

Question 3

- (10 points) Design a combinational circuit that generates the 9's complement of a BCD digit. Invalid codes are don't-care conditions. Draw the logic diagram.

Question 4

- (20 points) List the eight unused states in a 4-bit Johnson's counter. Determine the next state for each unused state and show that, if the circuit finds itself in an invalid state, it does not return to a valid state. Then modify the circuit so that the circuit reaches a valid state from any one of the unused states. Draw the logic diagram.

Question 5

- (20 points) Design a synchronous counter that has the following sequence: $0010, 0110, 1001, 1000, 1100, 1101$, and repeat. From the undesired states the counter must always go to 0010 on the next clock pulse. Draw the logic diagram.

Question 6

- (15 points) Implement a BCD ripple counter using a four bit binary ripple counter with asynchronous clear and external NAND gates. Draw the logic diagram.

Question 7

- (15 points) Determine the input equations for a BCD counter that uses
  1. only JK flip-flops, and
  2. only D flip-flops.

  Compare these two designs and the one given in the lecture that uses only T flip-flops. Determine which one is the most efficient and why.

Hooray! There is no lab questions in this assignment!

It means that you'd better spend more time on your project, though.