PART 2: DIGITAL DESIGN LAB

INTRODUCTION

In this lab, you are required to use Vivado 2017.4 to design a combinational logic circuit and do the testing.

PREAMBLE

Before working on the coursework itself, you should master the following material.

1. 'Digital design lab4', 'Digital design lab5', 'Digital design lab6' and 'Digital design lab7' in Sakai Board site.

2. Verilog: http://www.verilog.com

EXERCISE SPECIFICATION

Attention :

1) The name and bit-width of input port(s) and output port(s) , the name of modules'(including both design module and test bench module) MUST be same as described in the task, or you will get zero score about the task!!

2) The verilog files' name MUST be same with its module. For example, if the module's name is a1t1_xor, its file's name MUST be a1t1_xor.v.

TASK1(20 marks):

Implement the circuit and test its function: A parity generator circuit has **one input "x" which is 4 bit-width**, and **one output "y" which is 1 bit-width**. The output is 1 if the number of "1" in "x" is odd, else the output is 0. For example if "x" is 4'b0011, the number of "1" in "x" is 2 not an odd, so the output should be 0, if "x" is 4'b1011, the number of "1" in "x" is 3 which is an odd, so the output should be 1.

- Do the design in structure descriptions styles by using primitive gates.

- Using xor gates, the module's name MUST **be a2t1_xor**
- Using nand gates, the module's name MUST be **a2t1_nand**

➢ Build the test bench to verify the function of these 2 modules, the module's name MUST be **a2t1_sim**.

➢ Do the simulation to check if the function of these two modules are ok.

Design in structure descriptions styles by using xor and nand gates respectively.	5*2 marks
Test bench in Verilog, simulation result and its description	5*2 marks
Total	20 marks

TASK2(20 marks):

Implement the circuit and test its function: A combinational circuit has one input "**x**" which is **4 bit-width** , and one output "**y**" which is **1 bit-width**. The output is 1 if the input is a valid BCD coded decimal digit. Otherwise, the output is 0.

➢ Do the design in structure descriptions styles by using primitive gates on Sum-of-Minterms(the module's name MUST be **a2t2_somin**) and Product-of-Maxterms(the module's name MUST be **a2t2_pomax**) respectively.

➢ Build the test bench(the module's name MUST be **a2t2_sim**) to verify the function of these 2 modules(a2t2_somin and a2t2_pomax).

➢ Do the simulation to check if the function of these two modules is ok.

Design in structure descriptions styles by using primitive gates on Sum-of-Minterms and Product-of-Maxterms respectively.	5*2 marks
Test bench in Verilog, simulation result and its description	5*2 marks
Total	20 marks

TASK3(20 marks):

Implement the circuit and test its function: A combinational circuit has **one input "x" which is 4 bit-width, one output "y" which is 4 bit-width**. The output "y" is the 2's complement of input "x".

- Do the design in data-flow(the module's name MUST be **a2t3_df**) and behavioral description styles(the module's name MUST be **a2t3_bd**) respectively.
- Build the test bench(the module's name MUST be **a2t3_sim**) to verify the function of these two modules.
- Do the simulation to check if the function of these four-bit 2's complementers are ok.

Design in Verilog in data flow style and behavioral description style.	5*2 marks
Test bench in Verilog, simulation result and its description	5*2 marks
Total	20 marks

TASK4(40):

Implement the circuit and test its function: A combinational circuit named "one-hot code checker" which has **one input "x"(5 bit-width), one output "y"(1 bit-width)**. The output is 1 if the input is a valid one-hot code. Otherwise, the output is 0.

For example: If the code is 3 bit-width, only 3'b001, 3'b010 and 3'b100 is one-hot code, others are not.If the code is 4 bit-width, only 4'b0001, 4'b0010, 4'b0100 and 4'b1000 are one-hot code, others are not.

- Do the design in behavior description style.
  - Module **d74139** is a decoder with two input ports("**ne**" and "**x**") and one output port ("**y**"): "ne" is the enable port, its bit-width is 1. "x" is another input port which is 2 bit-width. "y" is the output port which is 4 bit-width. The truth-table of this module is as following table:

ne	x	y
1	X	4'hf
0	2'b00	4'b1110
0	2'b01	4'b1101
0	2'b10	4'b1011
0	2'b11	4'b0111

- Module **mux16to1** is a 16-to-1 MUX with two input ports("**x**" and "**sel**") and one output port("**y**"). "x" is 16 bit-width, "sel" is 4 bit-width, "y" is 1 bit-width. The relationship between "x", "sel" and "y" are described as following table:

sel	y	sel	y	sel	y	sel	y
4'h0	x[0]	4'h1	x[1]	4'h2	x[2]	4'h3	x[3]
4'h4	x[4]	4'h5	x[5]	4'h6	x[6]	4'h7	x[7]
4'h8	x[8]	4'h9	x[9]	4'ha	x[10]	4'hb	x[11]
4'hc	x[12]	4'hd	x[13]	4'he	x[14]	4'hf	x[15]

- Do the design in structure description style.
  - Using the decoder(**d74139**) and external gates(gates are optional), the module's name MUST be **a2t4_dc**.
  - Using one 16-to-1 MUX(**mux16to1**) and external gates(gates are optional), the module's name MUST be **a2t4_mux**.
- Build the test bench to verify the function of design modules
  - Verify the function of **d74139 and mux16to1.**
  - Verify the function of **a2t4_dc and a2t4_mux.**
- Do the simulation to check if the function of these modules are ok.

Design the Decoder(74139) and 16-to-1 MUX which would be used in the circuit.	5*2 marks
Design the circuit in structure description style by using the Decoder(74139) and 16-to-1 MUX.	5*2 marks
Test bench to verify the function of the Decoder(74139) and 16-to-1 MUX in Verilog, simulation result and its description.	5*2 marks
Test bench to verify the function of the circuit, simulation result and its description.	5*2 marks
Total	40 marks

SUBMISSION

Submit your assignment report in pdf to the Sakai site by the deadline.

Package source files, then submit it to the Sakai site by the deadline.

Attention :

1) The name and bit-width of input port(s) and output port(s) , the name of modules'(including both design module and test bench module) MUST be same as described in the task, or you will get zero score about the task!!

2) The verilog files' name MUST be same with its module. For example, if the module's name is "a1t1_xor", its file's name MUST be "a1t1_xor.v".

3) All the files MUST be in the same directory with no subdirectory in it.