Digital Design Assignment 3

Part 1: Digital Design Theory

Question1

Implement the following Boolean function F, using the two-level forms of logic:

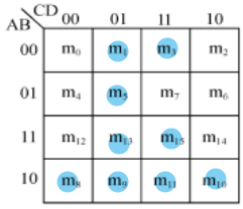
- (a) AND-OR
- (b) OR-AND
- (c) NOR-OR
- (d) NOR-NOR
- (e) NAND-NAND
- (f) NAND-AND

F(A,B,C,D)= ∑(1, 3, 5, 8, 9, 10, 11, 13, 15)

Please note that you only need to write the logic equation, no drawing needed

Answer

The Karnaugh map are as follow



(a)AND-OR

$$F(A,B,C,D) = C'D + B'D + AD + AB'$$

(b)OR-AND

$$F(A,B,C,D) = (A+D)(B'+D)(A+B'+C')$$

(c) NOR-OR

$$F(A,B,C,D) = \overline{C+D'} + \overline{B+D'} + \overline{A'+D'} + \overline{A'+B}$$

(d) NOR-NOR

$$F(A,B,C,D) = \overline{\overline{A+D} + \overline{B'+D} + \overline{A+B'+C'}}$$

(e) NAND-NAND

$$F(A,B,C,D) = \overline{\overline{C'D} \cdot \overline{B'D} \cdot \overline{AD} \cdot \overline{AB'}}$$

(f) NAND-AND

$$F(A,B,C,D) = \overline{A'D'} \cdot \overline{BD'} \cdot \overline{A'BC}$$

Question2

Derive the circuits for a parity generator and a parity checker using an even parity bit

Write the truth table, simplify your logic equation and draw circuit diagram using minimalnumber of gates

The parity generator has 4 inputs, A, B, C, and D

The parity checker has also 4 inputs, A, B, C and P

Truth table

A	B	C	D/P	Parity Bit/Parity Error Check
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1·	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

Simply the equation

$$\bar{A}\bar{B}\bar{C}D + \bar{A}\bar{B}C\bar{D} + \bar{A}B\bar{C}\bar{D} + \bar{A}BCD + AB\bar{C}D + AB\bar{C}\bar{D} + A\bar{B}\bar{C}\bar{D} + A\bar{B}CD$$

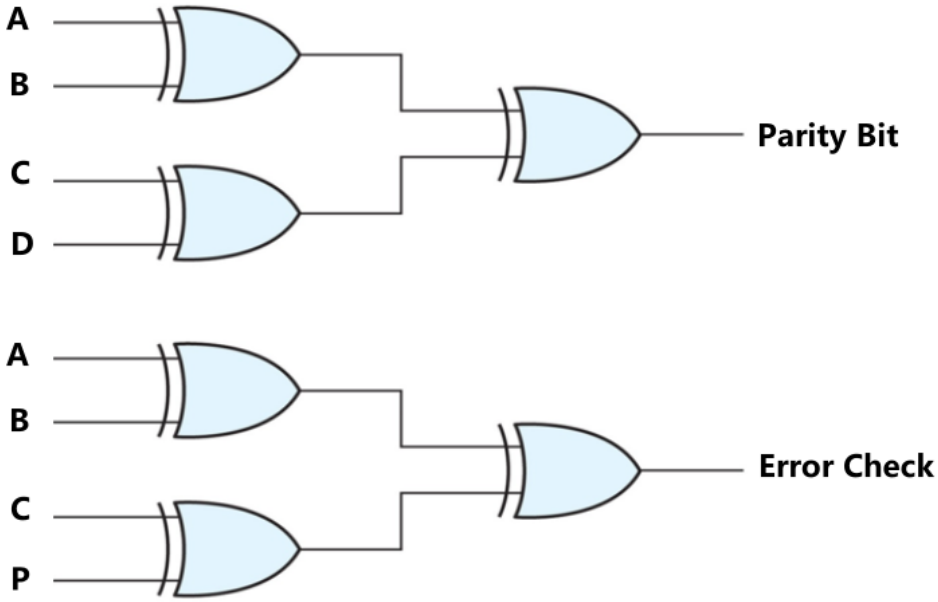
$$= \bar{A}\bar{B}(C \oplus D) + \bar{A}B(\bar{C}\bar{D} + CD) + AB(C \oplus D) + A\bar{B}(\bar{C}\bar{D} + CD)$$

$$= \bar{A}\bar{B}(C \oplus D) + \bar{A}B + AB(C \oplus D) + A\bar{B}$$

$$= C \oplus D(\bar{A}\bar{B} + AB) + A \oplus B$$

$$= (C \oplus D) \oplus (A \oplus B)$$

Circuit diagram



Question3

Design a combinational circuit with three inputs, x, y, and z, and three outputs, A, B, and C

When the binary input is 4, 5, 6, or 7, the binary output is one less than the input

When the binary input is 0, 1, 2 or 3, the binary output is one greater than the input

Write the logic formula and draw circuit diagram

Tip: You may use adders together with gates

x y z

- 0 → 0 0 0
- 1 → 0 0 1
- 2 → 0 1 0
- 3 → 0 1 1
- 4 → 1 0 0
- 5 → 1 0 1
- 6 → 1 1 0
- 7 → 1 1 1

When x = 0, which means the binary input is 0 or 1 or 2 or 3

When x = 1, which means the binary input is 4 or 5 or 6 or 7

We choose 3-bit full adder

So, when x = 0, A = {X,Y,Z}, B = {0,0,1}

So, when x = 1, A = {X,Y,Z}, B = {1,1,1} ,which is represent signed number -1

We ignore the carrier C3, and take C0 = 0

And the output equal to each S2 = A, S1 = B, S0 = C

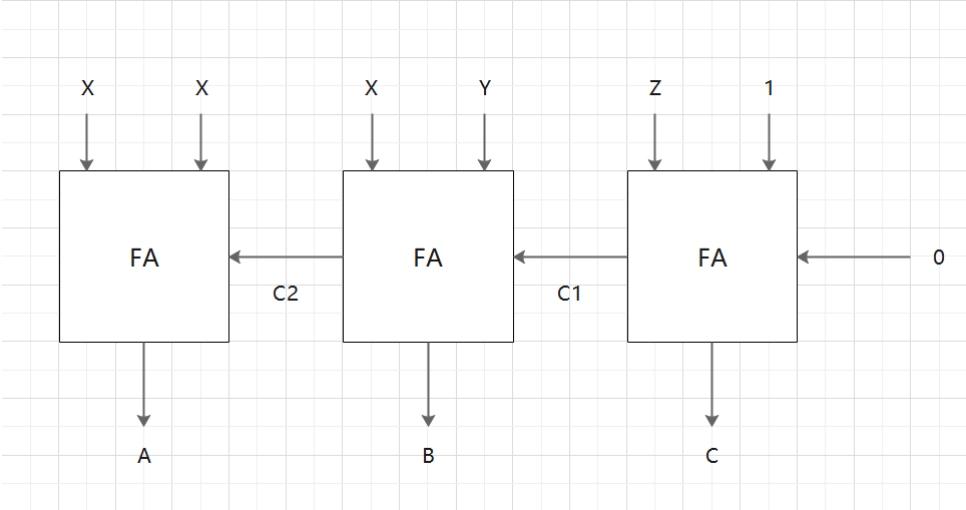
Logic Formula

$C = \overline{Z}$

$B = (X \oplus Y) \oplus Z$

$A = XY + YZ + XZ$

Circuit Diagram



Question4

For a binary multiplier that multiplies two unsigned four-bit numbers, use AND gates and adders, design the circuit

Briefly describe your design and list the logic formulas

Draw the circuit diagram

For adders, you can just use a block diagram with ports to represent them

Tip: You can write the signal name next to ports of gates/adders, to avoid drawing longwires.

Logic Formulas

Initial condition

$p_0 = m_0 q_0$

We define that

$P_{ij} = m_i q_j \oplus (m_i q_{j+1})$

$G_{ij} = (m_i q_j)(m_i q_{j+1})$

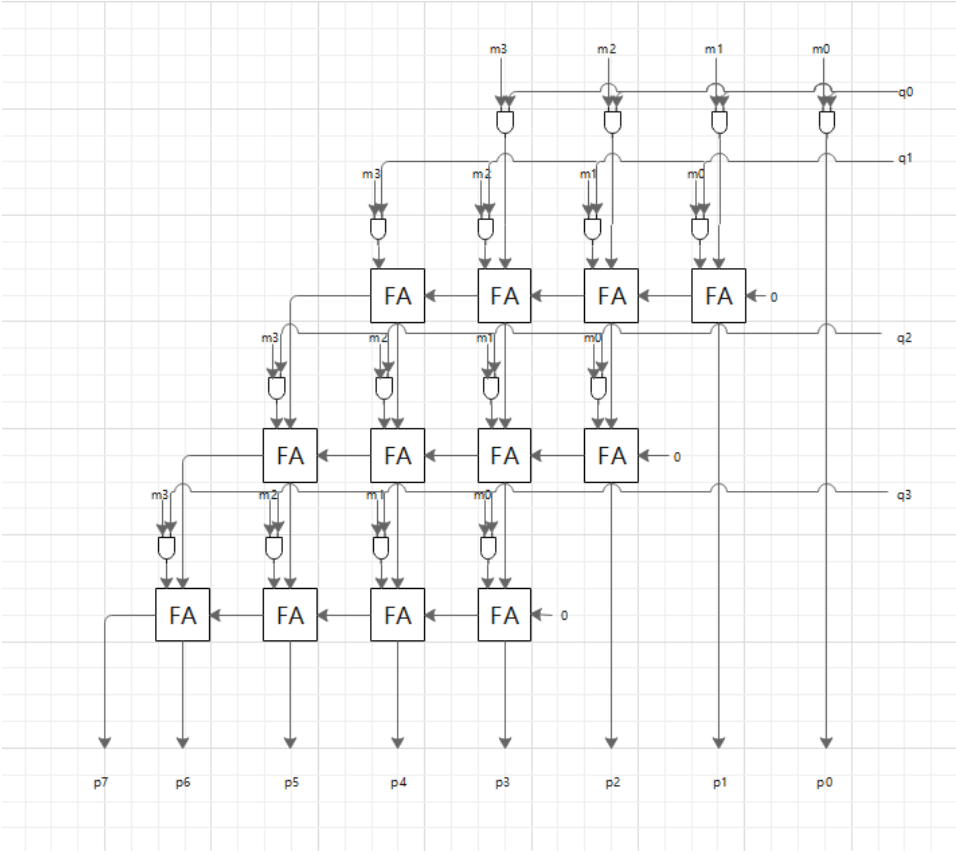
The sum of the output

$S_{ij} = P_{ij} \oplus C_{i+j}$

Thus

$p_{i+j+1} = G_{ij} + P_{ij} \cdot p_{i+j}$

Circuit Diagram



Question5

Implement the following Boolean function with a multiplexer

No drawings needed

(a) F(A, B, C, D) =∑ (1, 2, 5, 8, 10, 14)

(b) F(A, B, C, D) = Π (4, 5, 11)

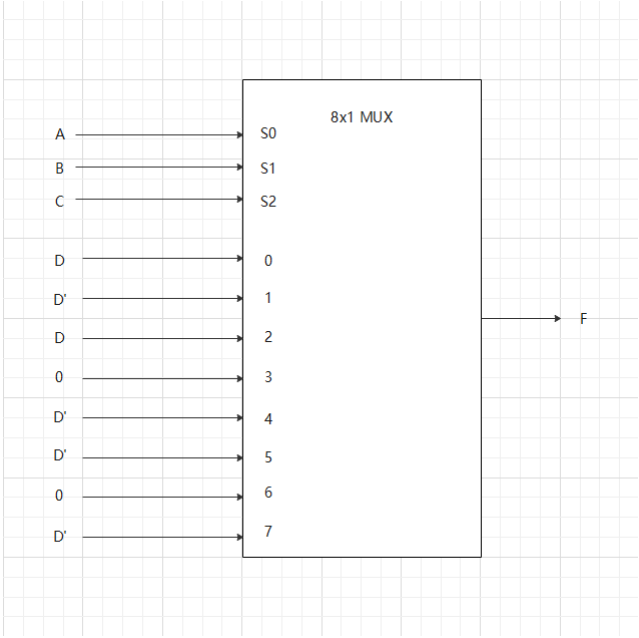
We take A,B,C as selection signal {S0,S1,S2}

(a)

Truth table

A	B	C	D	F
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

- D0 = D
- D1 = D'
- D2 = D
- D3 = 0
- D4 = D'
- D5 = D'
- D6 = 0
- D7 = D'



(b)

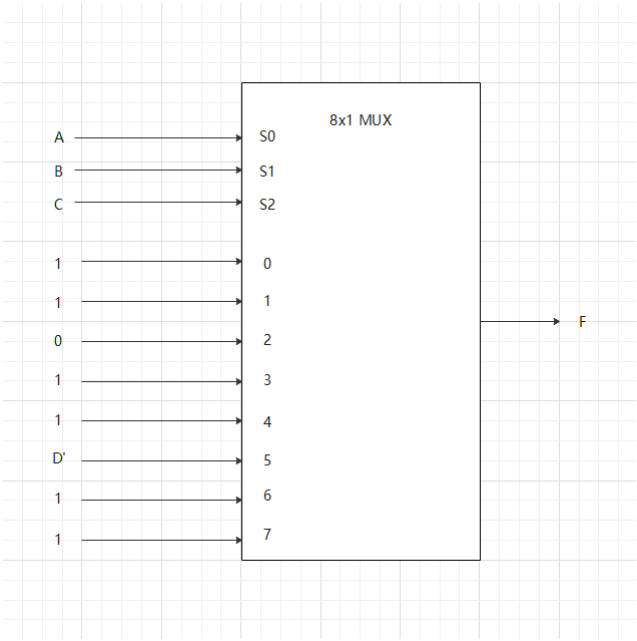
F(A, B, C, D) = Π (4, 5, 11) = ∑ (0, 1, 2, 3, 6, 7, 8, 9, 10, 12, 13, 14, 15)

Truth table

A	B	C	D	F
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	1

- D0 = 1

- D1 = 1
- D2 = 0
- D3 = 1
- D4 = 1
- D5 = D'
- D6 = 1
- D7 = 1



Question6

Implement a full subtractor with two 4x1 multiplexers or an 8x1 multiplexer. Write down your process and draw the circuit diagram

Use two 4x1 multiplexers to form a 8x1 multiplexer

The input are:

- A
- B
- K(borrow-in)

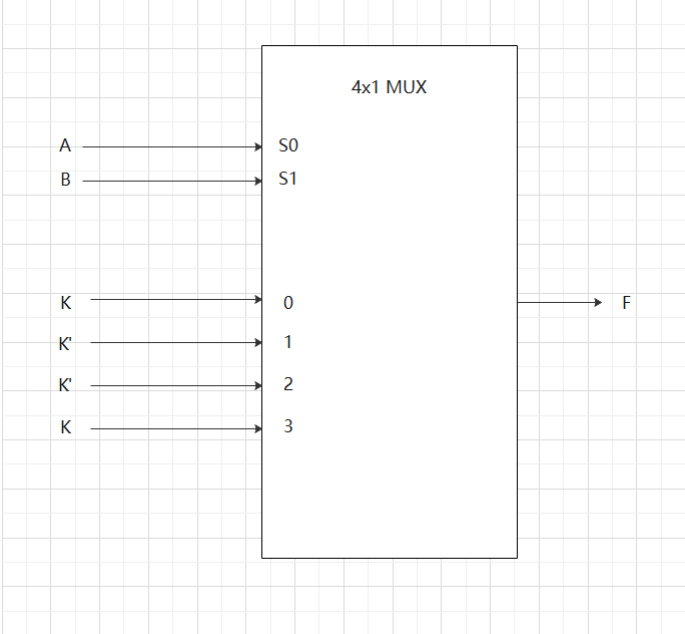
The output are:

- D(difference)
- O(borrow-out)

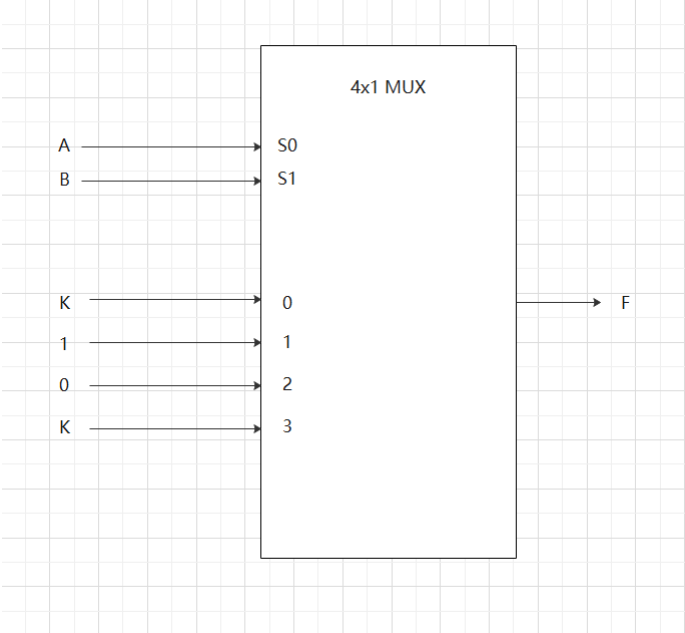
We take A,B as selection signal {S0,S1}

A	B	K	D	O
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

D (Difference)



O (borrow-out)



Part 2: Exercise Specification

Task1

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Task2

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