Tutorial Boolean algebra and circuits: solutions

Solutions

- 1. A NOT gate changes 0 to 1 and 1 to 0.
- a) 00110
- b) 01110000
- c) 010011000111
- 2.
- a) For an OR gate, a 0 is the output only when both outputs are 0, which means
- (i) 111101, (ii) 10111111 and (iii) 101111111101
- b) For an AND gate, a 1 is the output only when both inputs are 1, which means
- (i) 100001, (ii) 00001100 and (iii) 000100001000
- 3. Use the algorithm given in lectures.

$$E = xxy' + xx'y + xy'z$$
 = $xy' + 0 + xy'z$ (complement law and idempotent law) = $xy' + xy'z$ = xy'

4. a) and b) – b) can be done with an OR and NOT gate in place of the NOR gate. Note this is from an older textbook that does not put circles on NOT gates; we do expect NOT gates to have a circle.

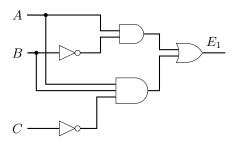


Figure 1: Solution 4a - Circuits from Expressions

5.

Boolean expression: (x' + y')(x + y')(y + z). Size: 7. Depth: 4.

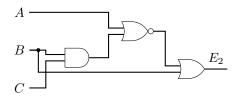


Figure 2: Solution 4b - Circuits from Expressions

$$(x' + y')(x + y')(y + z) = (x'x + x'y' + y'x + y'y')(y + z)$$

$$= (0 + y'(x' + x) + y')(y + z)$$

$$= (y' \times 1 + y')(y + z)$$

$$= (y' + y')(y + z)$$

$$= y'(y + z)$$

$$= y'y + y'z$$

$$= 0 + y'z$$

$$= y'z$$

In some of the above steps, two processes have been combined in a single step. Notice how much simpler the final result is from the initial condition. This implies a single AND gate fed by y' and z. To obtain y' we introduce a NOT gate in the y feed. The simplified circuit diagram is given in figure Solution 5 - Simplified Circuit.

Boolean expression: (y'z) Size: 2. Depth: 2.

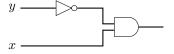


Figure 3: Solution 5 - Simplified Circuit

6.

a)

distributive law	y(x + x'y) = xy + x'yy
idempotent law	=xy+x'y
distributive law	=y(x+x')
complement law	= y

b)

$$(xy'+x')'=(xy')'x$$
 De Morgan's law
$$=(x'+y'')x$$
 De Morgan's law involution law
$$=(x'+y)x$$
 distributive law
$$=x'x+xy$$
 complement law

c)

$$(x+yz)(x'+z)=xx'+xz+x'yz+yzz$$
 distributive law
$$=0+xz+x'yz+yz$$
 complement law
$$=xz+x'yz+yz$$
 absorption law

7. To construct a circuit diagram, identify the input variables and the various gates required, evaluating terms in brackets first. In this case there are two variables, x and y. The expression (x'+ y) means that the variables a fed into an OR gate, however the prime above x (x') means that a NOT gate is required in the x feed going into the OR gate. Similarly the prime above the combined expression (x' + y)' means that a second NOT gate is required after the output of the OR gate. The other bracketed term (x + y) simply means that x and y are fed into another OR gate. The fact that both terms in bracket are multiplied means that the output of these expressions are combined by an AND gate. This is illustrated in figure Solution 7 - Original Circuit.

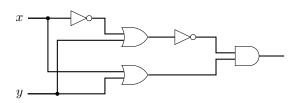


Figure 4: Solution 7 - Original Circuit

Alternatively, the expression can be simplified using the laws of Boolean algebra:

$$(x'+y)'(x+y) = xy'(x+y)$$
 De Morgan's law
$$= xxy' + xy'y$$
 distributive law
$$= xxy' + x0$$
 complement law
$$= xxy'$$
 boundedness
$$= xy'$$
 idempotent law

The circuit diagram is given in figure Solution 7 - Simplified Circuit; and looks rather familiar.

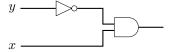


Figure 5: Solution 7 - Simplified Circuit