

Statement of Volatility 1-06-13213

Rev 0

Equipment Information								
Model Name:	Part Number:	rt Number: Manufacturer: Microchip						
Curiosity-	Curiosity-							
PIC64GX1000-Kit PIC64GX1000-Kit		ortji sum s	510 y 5411 0 550					
Model/Part Description: Curiosity-PIC64GX1000-Kit (Contains PIC64GX1000)								
Volatile Memory								
Does the item contain volatile memory (i.e., memory whose contents are lost when power is removed)? ⊠ Yes □ No								
If the answer is 'Yes', please provide the following information for each type (use additional sheets if required) following DSS Clearing and Sanitization Matrix requirements								
Type: L2 Cache (inside	Size: 2MB or	User Modifiable: ⊠ Yes □ No	Function:	Process to Clear/Sanitize:				
PIC64GX1000)	1.875 MB		Inside device	By using device applications/Design				
	LIM with ECC	User Data Access: ⊠ Yes □ No	Runtime reconfiguration between cache and RAM					
		Battery Backup ☐ Yes ⊠ No						
Type:	Size:	User Modifiable:	Function:	Process to Clear/Sanitize:				
E51 RISC V Monitor core		⊠ Yes □ No	Inside device	By using device applications/Design				
L1 iCache	16KB	User Data Access: ⊠ Yes □ No	Cache memory for instruction, it is used for	, and a second property of the second propert				
DTIM	OLD	D-44 Dl	fetching instructions.					
(inside PIC64GX1000)	8KB	Battery Backup ☐ Yes ⊠ No						
Type:	Size:	User Modifiable:	Function:	Process to Clear/Sanitize:				
U54 RISV-Application core L1 icache	28KB	⊠ Yes □ No	Inside device	By using device applications/Design				
L1 dCache	32KB	User Data Access:	Cache memory for					
(inside PIC64GX1000)		⊠ Yes □ No	instruction and Data, it is used for fetching					
(42246 1200 10121000)		Battery Backup ☐ Yes ⊠ No	instructions					
Type:	Size	User Modifiable:	Function:	Process to Clear/Sanitize:				
DDR4 SDRAM MT40A512M16TB-062E:R	8Gbit	⊠ Yes □ No	For DDR4 application design read write	Parallel interface MSS DDR controller issues commands to the DDR				
WITTOASIZWIIOIB-00ZE.K		User Data Access: ⊠ Yes □ No	design read write	PHY, which sends and receives data to/from the DDR SDRAM via the MSS DDR BANK 6 I/O.				
		Battery Backup ☐ Yes ⊠ No						
			atila Marra arra					
Doog the item contain	non volotilo momo		atile Memory	ed when power is removed)?				
Yes		ry (i.e., memory w	nose contents are retain	ed when power is removed):				
If the answer is 'Yes', please provide the following information for each type (use additional sheets if required) following DSS Clearing and Sanitization Matrix requirements								
eNVM	Size:	User Modifiable:	Function:	Process to Clear/Sanitize:				
Boot Flash (inside PIC64GX1000)	128 KB	⊠ Yes □ No	Storing initialization data					
		User Data Access: ☑ Yes ☐ No	for LSRAM and uSRAM	Through JTAG Interface				
EEPROM Memory	2Kbit	User Modifiable:	Function:	Process to Clear/Sanitize:				
93LC56BT-I/OT (External EEPROM)		⊠ Yes □ No	Storing configuration data	USB Interface				
		User Data Access: ⊠ Yes □ No						
Media								
Does the item contain media storage capability (i.e., removable or non-removable disk drives, tape drives, memory cards,								
etc.)?								
∑ Yes								



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If the answer is 'Yes', please provide the following information for each type (use additional sheets if required):							
Type: microSD Card connector MEM2075-00-140-01-A	Size: 9 (8 + 1) Position Card Connector	User Modifiable: ☐ Yes ☐ No User Data Access: ☐ Yes ☐ No Battery Backup ☐ Yes ☐ No	Function: Secure Digital - microSD Surface Mount Gold Connector only (No microSD card along with KIT).	Process to Clear/Sanitize: MSS SD Host controller able to access microSD card (SDUC) inserted into microSD card slot.			
Additional Information:							
Supplier Representative Information							
Name: Himanshu Tewari	Title: Senior Manager – D	Design Engineering	Office Phone: +91 4067-303698	Email: Himanshu.Tewari@Microchip.com			