64-bit RISC-V Embedded Microprocessors

White Paper

Introduction

Compute-intensive applications such as secured embedded vision and AI/ML are pushing the boundaries of power-efficient computing. These applications demand high performance, hardware-level security, secure boot, and reliability at the intelligent edge. To meet these requirements, intelligent edge applications need 64-bit heterogeneous compute solutions capable of running Linux®, Real-Time Operating Systems (RTOSs), and bare-metal in a single processor cluster, a concept known as Asymmetric Processing (AMP). Additionally, embedded system designers require a comprehensive end-to-end solution, from silicon to embedded ecosystem, to accelerate time to market.

Microchip's 64-bit RISC-V MPU products (PIC64GX) address the mid-range intelligent edge compute needs with a 64-bit RISC-V quad-core processor featuring AMP and real-time deterministic processing capabilities. Embedded designers can leverage the rich embedded ecosystem to enable faster design, debug, and verification processes. PIC64GX systems are quickly enabled through a wide range of operating systems, build systems, drivers/middleware, and a variety of open-source and commercial tools.

PIC64GX is a highly power-efficient, Linux-capable processor that serves as an innovative, mid-range embedded compute platform based on the RISC-V ISA. The RISC-V CPU micro-architecture implementation features a simple, 5-stage single-issue, in-order pipeline that is immune to the Meltdown and Spectre exploits found in common out-of-order machines. It includes five RISC-V cores that are coherent with the memory subsystem, allowing a versatile mix of deterministic real-time systems and Linux in a single, multi-core processor cluster. With built-in Secure Boot, innovative Linux and Real-Time modes, a large L2 memory subsystem, and a rich set of embedded peripherals, the RISC-V MPU provides embedded developers with new choices in secure, power-efficient, embedded compute platforms.

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1. Microprocessor System Overview

The microprocessor system is designed to deliver high performance and flexibility for a wide range of applications. It features multiple processing cores, advanced memory subsystems, and a variety of integrated peripherals. The following is a detailed breakdown of the system's key components and capabilities.

Monitor Processor Core

The system includes a 64-bit RV64IMAC monitor processor core with a maximum frequency (Fmax) of 625 MHz, operating within a temperature range of –40 °C to 85 °C. It delivers 3.1 CoreMarks®/MHz and 1.7 DMIPs/MHz:

- 16 KB memory subsystem with SECDED, configurable as a 2-way L1 instruction cache or as a tightly integrated memory
- 8 KB data tightly integrated memory
- PMP unit

Application Processing Cores

The system also features four 64-bit RV64GC application processing cores, each with an Fmax of 625 MHz, operating within a temperature range of –40 °C to 100 °C. These cores deliver 3.1 CoreMarks®/MHz and 1.7 DMIPs/MHz:

- L1 memory subsystem with SECDED
  - 32 KB 8-way instruction cache or optional 28 KB tightly integrated memory
  - 32 KB 8-way data cache
- Physical Memory Protection (PMP) unit
- Memory Management Unit (MMU)

Memory Subsystems

The memory subsystem includes features like 2 MB L2 memory with different modes for access, an integrated memory controller supporting various DDR versions, a Memory Protection Unit (MPU), and embedded non-volatile memory for secure boot options:

- Cache coherent CPU bus matrix
- Flexible 2 MB L2 memory subsystem with SECDED, configurable as:
  - 16-way set associative L2 cache
  - Loosely Integrated Memory (LIM) mode for deterministic access
  - Coherent Scratchpad Memory mode for shared messages across cores
- Integrated 36-bit DDR4/LPDDR4 memory controller with SECDED, supporting DDR4 at 1.6 Gbps with an 8 GB address reach
- Memory Protection Unit (MPU)
- Integrated 128 Kbytes embedded Non-Volatile Memory (eNVM) for boot, with the following boot options:
  - Microchip secure boot
  - User defined, PUF-protected secure boot
  - Boot directly from eNVM

Interrupt Controller

The platform interrupt controller supports:

- Seven priority levels

- Core-based interrupt allocation
- Vectored and non-vectored support
- Direct core interrupt connections

Debug Features

The system includes robust debug features:

- JTAG compatible debug
- Ten hardware triggers per CPU, configurable as breakpoints or watchpoints
- Performance counters

Configurable Peripherals

The system offers a range of configurable peripherals:

- Two GigE MACs
- USB 2.0 OTG
- MMC 5.1 SD/SDIO
- Two CAN 2.0
- Execute in place Quad SPI flash controller
- Five multi-mode UARTs
- Two SPI, two I2C
- RTC, GPIO
- Five watchdog timers
- Timers
- Integrated single x4 PCIe Gen2 Root Port (RP) – depending on the device

Operating Modes

The system supports 1.0V and 1.05V operating modes.

2. Market Segments and Use Cases

64-bit processors are used in various applications across different market segments. Primary use cases include single board embedded computing, motor control, real-time computing, vision, and AI/ML applications.

A sample use case of sensor aggregation & inferencing can be achieved by running a real-time operating system in a single context. Sensors can be easily connected to the PIC64GX using interface peripherals such as SPI and I2C. The real-time operating system can then process sensor data instantly, and communication blocks like UART, GEM, or CAN can be utilized to transmit data or summary data as required based on edge computing.

For embedded computer vision tasks, a separate Linux context can be employed to conduct object identification, classification, and video streaming over interfaces like Ethernet.

By leveraging the AMP capabilities of the device, both the use cases can be accomplished with just a single PIC64GX device.

3. Security Features

The following list outlines the key security features integrated into the system, ensuring robust protection against various threats:

- Integrated dual Physically Unclonable Function (PUF)
- 56 KB of secure Non-Volatile Memory (sNVM)
- 128 KB of embedded Non-Volatile Memory (eNVM)
- Built-in tamper detectors and countermeasures
- Integrity check for sNVM and eNVM
- DPA resistance

4. Key Value Drivers

The following key value drivers highlight the advanced features and benefits of the Microchip RISC-V products. These drivers include configurable memory subsystems, asymmetric multiprocessing capabilities, a range of security features, and the advantage of an existing ecosystem of Microchip solutions.

Configurable L1 Memory Subsystem (for Application Cores)

- Configurable up to 32 KB of L1 instruction and data cache
- Configurable up to 32 KB of L1 Instruction Tightly Integrated Memory (ITIM)

Configurable L2 Memory Subsystem

- Configure up to 2 MB of L2 cache
- Configure up to 1.85 MB of L2 Loosely Integrated Deterministic memory (LIM)
- Configure up to 1.85 MB of L2 scratchpad (high throughput non-deterministic) memory

Asymmetric Multiprocessing Capabilities

- Bring a deterministic RTOS to a Linux system
  - Split tasks between deterministic (RTOS) tasks and non-deterministic (Linux) tasks
- Improve safety and reliability with zero interrupt latency

Range of Security Features

- Use PMPs (Physical Memory Protection) to secure AMP contexts from unintended memory corruption or access of protected address space
- DPA secure
- Secure boot from Microchip secure boot to user-defined secure boot

Existing Ecosystem of Microchip RISC-V Products, Solutions, and Experience

- Take advantage of the existing Microchip solution stack to accelerate time to market

5. Performance Benchmarks

Performance benchmarks are essential metrics used to evaluate the efficiency and capability of a system. The following benchmarks provide a comprehensive view of the system's performance:

DMIPS	1.7/MHz
CoreMarks	3.1/MHz
FPMarks	6.5/MHz
CoreMarkPro	750

6. Tool Chain, OS and Embedded Ecosystems

The following list outlines the supported tool chains, operating systems, and embedded ecosystems. These tools and systems are essential for developing, building, and managing embedded applications.

Tool Chain	MPLabs IDE is the supported primary Integrated Development Environment (IDE).
Boot Loaders	Hart Software Services (HSS): Source code for the HSS zero stage bootloader and system monitor
Real Time Operating Systems (RTOS)	Zephyr: Upstream support within the Zephyr RTOS ecosystem
Linux® Build Systems	• Yocto BSP: Yocto-based Linux build system – Using the Linux4Microchip kernel with device trees being pushed to mainline • Microchip Buildroot External: Buildroot-based Linux build system – Using the Linux4Microchip kernel with device trees being pushed to mainline
Operating Systems (OS)	Ubuntu support from 2024.10
GitHub Repository	For tools and systems, visit the github.com/pic64gx GitHub repository.

7. Mi-V Ecosystem

The Mi-V RISC-V ecosystem is a continuously expanding, comprehensive suite of tools and design resources developed by Microchip and numerous third parties to fully support RISC-V designs. The Mi-V ecosystem aims to increase adoption of RISC-V ISA and Microchip's RISC-V compute products.

8. Conclusion

Microchip's PIC64GX compute solution operates at 625 MHz and is equipped with a Linux-capable quad-core CPU cluster and a monitor processor. The compute solution is built on key value drivers, including an on-chip non-volatile memory designed for secure boot and key management, as well as a flexible memory which is optimized for superior performance and deterministic latency. The CPU cluster offers configurability to support both Linux and real-time operating systems, providing Asymmetric Multi-Processing. It also features a wide range of connectivity options with onboard peripherals and is supported by a comprehensive embedded ecosystem.

9. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision	Date	Description
A	07/2024	Initial revision

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