16337102　　黄梓林

1. Why is it difficult to construct a true shared-memory computer? What is the minimum number of switches for connecting p processors to a shared memory with b words (where each word can be accessed independently)?

2. Consider a memory system with a level 1 cache of 32 KB and DRAM of 512 MB with the processor operating at 1 GHz. The latency to L1 cache is one cycle and the latency to DRAM is 100 cycles. In each memory cycle, the processor fetches four words (cache line size is four words). What is the peak achievable performance of a dot product of two vectors? Note: Where necessary, assume an optimal cache placement policy.

```
/* dot product loop */
for (i = 0; i < dim; i++)
    dot_prod += a[i] * b[i];
```

1. 因为在共享内存的计算机中，多个进程共享同一块内存区域，同一数据可能同时被多个进程访问，修改，因此数据在不同进程中的一致性难以保持；而为了维持数据的一致性，各进程之间需要进行正确的通信，通信机制的建立也是一大难点。
将 P 个处理器连接到一个大小为 b 个字的共享内存，需要的最少开关数 = P + b

2. 当两个向量存在缓存中时，运算时间 = $\frac{\dim}{2*10^9}$s
（dim 为向量的维度；每次相乘运算需要两个字，而每一拍 CPU 能从缓存中抓取四个字，及每一拍 CPU 能进行两次相乘运算）
当两个向量存在 DRAM 时，运算时间 = $\frac{\dim}{2*10^9}+10^{-9}$s
当两个向量存在硬盘中时，运算时间 = $\frac{\dim}{2*10^9}+10^{-9}+10^{-7}$s