# Design and Simulation of an Op-Amp Controlled Voltage-Controlled Current Source (VCCS)

**A Report Submitted as part of the Analog Design Internship Assignment**

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## 1. Objective

The primary objective of this assignment is to design, simulate, and analyze a voltage-controlled current source (VCCS) using an op-amp-based analog circuit in LTspice. The core requirement is to generate a precisely controlled output current from 0–5 mA that is directly and linearly proportional to a 0–5 V input control voltage.

The design process involves three main stages:

1. Converting a digital PWM control signal into an equivalent analog DC voltage.
2. Buffering this voltage to ensure signal integrity.
3. Using the buffered voltage to drive a precision op-amp-controlled NMOS current sink.

The analysis will validate the design's frequency response, ripple suppression, linearity, and operational limits (compliance) through rigorous simulation.

## 2. Topology Selection and Justification

### System overview

The circuit is organized as four functional stages:

1. PWM source (input)
2. PWM → DC conversion: 2nd-order Sallen-Key Butterworth low-pass filter
3. Buffer / driver (unity-gain op-amp follower)
4. Voltage-to-current (VCCS) core: op-amp driven NMOS current sink with Rsense feedback and gate compensation

This split isolates functions (filtering, buffering, power switching) so each can be optimized independently and the overall loop is stable and testable.

## 1) PWM source (Vin)

**Topology:** Ideal voltage PULSE source generating 0–5 V square PWM.

**Why:** PWM is the required control interface; producing a variable average (duty) that maps to the desired analog control voltage. Using an ideal PULSE makes it trivial to vary frequency and duty during tests. 0–5 V matches standard logic and the later op-amp input range.

**Notes / what to watch:** choose PWM frequency relative to filter cutoff (higher PWM frequency → easier filtering / lower ripple, but higher sampling demands on timestep for FFT). For assignment, 100–200 Hz used for illustration; tests should include higher frequencies to show filter behavior.

## 2) Low-pass filter — Sallen-Key (Butterworth) 2nd-order

**Topology:** Sallen-Key (unity gain or slightly buffered) second-order Butterworth (Salem-Key) LPF using two resistors and two capacitors (R1, R2, C1, C2) and an op-amp U1.

**Why chosen:**

* **Sallen-Key** is simple to implement in LTspice, requires only one active device, and provides a clean 2-pole response with low component count.
* **Butterworth** response gives maximally flat passband (no ripple) — ideal when the DC accuracy of the averaged value matters.
* A 2nd-order LPF provides substantially better harmonic attenuation than a single RC and keeps phase shift modest relative to higher-order designs.

**Design targets & behavior:**

* Cutoff fc​ chosen well below PWM fundamental frequency but above the maximum modulation bandwidth required for the current source. Typical rule: fc​≈fPWM​/10 or set to meet ripple spec. For example, for PWM = 200 Hz, choose fc​∼20 Hz to minimize ripple while allowing reasonable response time.
* Butterworth Q = 0.707; choose component ratios accordingly (R and C values set to meet desired fc​ and damping).

**Tradeoffs:**

* Lower fc → less ripple, slower step response (longer settling time).
* Higher fc → faster response, increased ripple.

**Practical note:** Place the LPF input on the PWM node and ensure the op-amp used for the Sallen-Key has rail capability for the 0–5 V signal or is powered appropriately.

## 3) Buffer (unity-gain follower)

**Topology:** Op-amp configured as voltage follower (U2) between filter output (Vctrl) and VCCS control input.

**Why chosen:**

* **Isolation:** prevents the current sink’s input impedance and transient behavior from loading the filter and changing its cutoff / DC value.
* **Drive:** provides a low impedance source to the next stage so the gate drive / compensation network can be driven without disturbing the filter capacitor.
* **Simplicity:** unity gain avoids introducing gain error — we want Vctrl preserved exactly.

**Design justification:**

* A buffer prevents the filter node from being pulled by input bias currents or the feedback network of the current sink, guaranteeing accurate Vctrl = averaged PWM.
* If the VCCS loop needs a fast control bandwidth, the buffer must have sufficient slew rate and bandwidth; for a slow DC control (0–5 mA), general op-amp models suffice.

**Practical note:** use an op-amp model (or “universal/opamp2”) compatible with single-supply 0–15 V rails or use ± rails accordingly.

## 4) VCCS core — Op-amp + NMOS current sink with Rsense feedback

**Topology:** An op-amp (U3) senses the voltage across Rsense and drives an external N-MOSFET’s gate through Rgate. The MOSFET’s source is tied to Rsense; the drain goes to Rload and Vsup. The op-amp forces the Rsense voltage to equal the control voltage (Vctrl), producing Iout​=Vctrl​/Rsense​.

**Why chosen:**

* **High compliance with low parts count:** Using a power MOSFET as the series element allows the sink to handle significant voltages/currents while the op-amp performs low-power sensing and control.
* **Wide dynamic range:** the external MOSFET provides the voltage headroom (compliance) needed to drive large Rload values while keeping power dissipation in the device acceptable.
* **Precision control:** op-amp feedback across Rsense gives accurate Iout independent of MOSFET device characteristics (Vgs threshold, on-resistance).

**Control equation:**

Iout​=Rsense​Vctrl​​

the op-amp drives gate until Vsense​=Vctrl​ (closed loop).

**Key components & roles:**

* **Rsense (1 kΩ):** sets transconductance — simple relation: 1 V control → 1 mA output. Chosen for convenient scaling (0–5 V → 0–5 mA).
* **MOSFET (M1):** chosen to handle Vsup and dissipate power during compliance. NMOS in low-side or high-side configuration? Here it’s low-side/series to ground via Rsense (source to Rsense), drain to Rload. Use a power NMOS with sufficient Vds rating.
* **Rgate (47 Ω):** series resistor between op-amp output and MOSFET gate. Purpose:
  + Limits peak gate charge current (softens transitions),
  + Prevents high-frequency oscillations by isolating gate capacitance from op-amp output,
  + Works with any Ccomp to create compensation poles/zeros.
* **Ccomp (not explicitly shown as named, but compensation loop present):** often a small capacitor (or RC) across the op-amp feedback to stabilize the loop by reducing loop bandwidth and adding phase margin.

**Stability rationale:**

* The op-amp + MOSFET + Rsense loop is a **one-pole power transistor** plus **op-amp** feedback system. The MOSFET gate-to-source / drain-to-source capacitances and the Rsense/Pwr path create poles that can reduce phase margin.
* **Rgate + Ccomp** (or Miller compensation in the op-amp) reduces bandwidth of error amplifier seen by the MOSFET gate, improving phase margin. You must tune Rgate and Ccomp empirically in simulation to prevent ringing/oscillation.
* Keep the loop crossover frequency well below the open-loop gain rolloff of the op-amp and below the frequency where MOSFET parasitics dominate.

**Compliance considerations:**

* **Definition:** Maximum Vload​ for which the sink can still regulate Iout. Regulation requires:  
  Vsup​≥Vload​+Vrsense​+Vds(M1,min)​
* With Vsense = Iout × Rsense and typical Vds(min) a few volts, compute Rload,max:  
  Rload,max​≈Iout​Vsup​−Iout​Rsense​−Vds(min)​​
* In your assignment, this yields ≈10 kΩ for the chosen numbers (60 V supply, Rsense = 1 kΩ, Iout = 5 mA).

**Why NMOS + op-amp instead of op-amp alone?**

* Op-amp alone cannot source/sink large currents or handle high compliance voltages; MOSFET offloads power dissipation and voltage stress from the op-amp, enabling higher Vsup and power handling with precise current control.

## Additional practical justification and notes

### Component value rationale

* **Rsense = 1 kΩ**: convenient mapping 1 V → 1 mA, simple math and measurements for 0–5 mA range.
* **Rgate = 47 Ω**: typical value to damp gate oscillations and limit current spikes; tune if oscillation appears.
* **Filter RC values**: chosen to get Butterworth fc according to standard Sallen-Key design equations. (Document your chosen R/C values and show calculated fc in the report.)

### Node placement and measurement

* Sense node should be at the **source of MOSFET** (if low-side). Use Kelvin sense if layout/measurement accuracy matters.
* Measure Vdrain (node at MOSFET drain) and Vsource (sense node) to compute Vds and P dissipated in MOSFET.

### Testing and stability workflow (recommended)

1. Simulate open-loop MOSFET model to study gate capacitances.
2. Run transient with step input to observe step response and tune Rgate/Ccomp to remove ringing.
3. Use .meas and .step to find compliance point (Iavg vs Rload).
4. Run AC/Bode or small-signal analysis (if op-amp supports) to estimate loop crossover and check phase margin.

### Alternatives and why rejected

* **Current mirror using discrete BJTs:** simpler but poor compliance and less flexible for wide voltage.
* **Op-amp only (no MOSFET):** limited current/voltage capability — not suitable for larger Rload ranges.
* **Higher order filter (active 4th order):** better ripple suppression, but increases phase shift and complicates compensation with op-amp loops. A 2nd order Butterworth is a robust compromise.

## 3. Key Design Calculations

### 3.1 Current-Setting Resistor (Rsense)

The output current is defined by the relationship I\_out = V\_ctrl / Rsense. The design requires a maximum I\_out of 5 mA for a maximum V\_ctrl of 5 V.

* Rsense = V\_ctrl\_max / I\_out\_max
* Rsense = 5 V / 5 mA
* **Rsense = 1 kΩ**

### 3.2 Low-Pass Filter Design

To effectively filter the 200 Hz PWM, the filter's cutoff frequency (f\_c) must be significantly lower. A common rule of thumb is at least one decade lower.

* f\_pwm = 200 Hz
* Chosen f\_c = 20 Hz
* For a 2nd-order Sallen-Key buffer filter with equal resistors and capacitors:
  + f\_c = 1 / (2 \* π \* R \* C)
  + Let's choose a standard capacitor value C = 1 µF.
  + R = 1 / (2 \* π \* f\_c \* C) = 1 / (2 \* π \* 20 Hz \* 1 µF)
  + **R ≈ 7.96 kΩ** (A standard 8 kΩ or 8.2 kΩ resistor can be used).

### 3.3 Output Compliance and Load Limit

Compliance defines the maximum load voltage (and thus maximum R\_load) the current source can handle while maintaining the set current. The NMOS transistor requires a minimum voltage (V\_ds\_sat, or V\_ds(min)) to operate in the saturation region (as a current source). The voltage across Rsense (V\_sense) also subtracts from the available voltage for the load.

* V\_load\_max = V\_sup - V\_ds(min) - V\_sense
* Given: V\_sup = 60 V
* From simulation/datasheet, assume a conservative V\_ds(min) ≈ 5 V to ensure saturation.
* At maximum current (5 mA), V\_sense = I\_out\_max \* Rsense = 5 mA \* 1 kΩ = 5 V.
* V\_load\_max = 60 V - 5 V - 5 V = 50 V
* The maximum load resistance is calculated at maximum current:
* R\_load\_max = V\_load\_max / I\_out\_max = 50 V / 5 mA
* **R\_load\_max = 10 kΩ**

This calculation matches the simulation results perfectly.

## 4. Power Supply Requirements and Selection

### 4.1 Filter design — Sallen-Key Butterworth 2nd order

**Topology & design equations**

For a unity-gain Sallen-Key Butterworth (equal component form: R1​=R2​=R, C1​=C2​=C), the natural frequency fc​ (cutoff frequency) is:

fc​=2πRC1​

The Butterworth (maximally-flat) damping requires quality factor Q=1/2​≈0.707, achieved by equal component values in unity-gain configuration.

**Given values (from schematic):**

* R=10kΩ
* C=0.82μF=0.82×10−6F

**Cutoff frequency:**

fc​=2π⋅10,000⋅0.82×10−61​=2π⋅0.00821​≈19.4 Hz

**Interpretation:** fc​≈19.4 Hz — well below the PWM fundamental (200 Hz), so the filter will strongly attenuate switching harmonics while passing slowly varying control changes.

### 4.2 Transient response / settling time estimate

For a second-order system with natural frequency ωn​=2πfc​ and damping ζ=1/2​, a practical settling-time estimate (to within a few % of final value) is:

tsett​≈ζωn​4​

Compute:

ωn​=2πfc​≈2π(19.4)≈122 rad/stsett​≈0.707×1224​≈0.046 s ≈46 ms

**Interpretation:** Expect the filtered DC to reach steady value in roughly 30–60 ms after a step in duty. This matches the slow charge/discharge behavior visible in simulations.

### 4.3 PWM average to control voltage and current mapping

For a unipolar PWM between 0 and VH​ with duty D, the DC average (ideal) is:

Vavg​=D⋅VH​

With VH​=5 V and D=0.5 (50 % duty):

Vavg​=0.5×5=2.5 V

The sense resistor maps control voltage to output current:

Iout​=Rsense​Vctrl​​

With Rsense​=1kΩ:

I\_{out} = \frac{2.5}{1000} = 2.5\ \text{mA} \quad\text{(for 50 % duty)}

And for full-scale Vctrl​=5 V: Iout,max​=5/1000=5 mA.

**Interpretation:** The mapping is linear and convenient: 1 V → 1 mA.

### 4.4 Filter attenuation at PWM frequency (approximate)

Use normalized frequency x=fc​f​. For a second-order Butterworth:

∣H(jω)∣=(1−x2)2+(2​x)2​1​

For PWM fundamental fPWM​=200 Hz:

x=19.4200​≈10.3

Compute magnitude:

∣H∣≈(1−10.32)2+(1.414⋅10.3)2​1​≈0.00943

In dB:

20log10​(∣H∣)≈20log10​(0.00943)≈−40.5 dB

**Estimate of residual ripple from the fundamental**

* The first harmonic (fundamental) component amplitude of the 0–5 V unipolar square at 50 % duty has Fourier coefficient a1​≈πVH​​≈π5​≈1.59 V.
* After the filter the fundamental amplitude ≈ 1.59×0.00943≈0.015 V (≈ 15 mV).
* So ripple (peak) ≈ 15 mV, peak-to-peak ≈ 30 mV (approximate).

**Interpretation:** With fc ≈ 19.4 Hz and PWM = 200 Hz, the fundamental is attenuated by ≈ −40 dB and ripple amplitude becomes few tens of mV — acceptable for a 0–5 mA current sink.

### 4.5 Compliance (maximum load) calculation

Compliance means the maximum load resistance Rload,max​ at which the current source can still regulate the target current Iout​. Regulation requires enough headroom on the MOSFET:

Vsup​≥Vload​+Vsense​+Vds(min)​

where Vload​=Iout​Rload​ and Vsense​=Iout​Rsense​. Rearranged,

Rload,max​≈Iout​Vsup​−Vsense​−Vds(min)​​

**Use your chosen values:**

* Vsup​=60 V
* Iout​=5 mA (design max)
* Rsense​=1 kΩ → Vsense​=Iout​Rsense​=5mA⋅1kΩ=5 V
* Conservative Vds(min)​≈5 V (a safety assumption; actual required Vds depends on MOSFET Vgs and op-amp drive)

Compute:

Rload,max​≈0.00560−5−5​=0.00550​=10,000 Ω=10 kΩ

**Interpretation:** This matches your swept-simulation result: current regulation is maintained up to ≈10 kΩ. If you can confirm a lower required Vds(min)​ from simulation or MOSFET datasheet, R\_load,max will increase accordingly.

## 5. Simulation Methodology and Results

### 5.1 Simulation Methodology

The complete voltage-controlled current source (VCCS) system was simulated in **LTspice 24.1.9 for Windows** using a modular approach. Each stage—filter, buffer, and current sink—was first verified individually and later combined into a single schematic for full-system analysis.

#### (a) PWM Input and Filter Stage

A 0–5 V PWM signal at **200 Hz** was generated using a PULSE source.

A **2nd-order Butterworth Sallen–Key low-pass filter** (R₁=R₂=10 kΩ, C₁=C₂=0.82 µF) was used to convert this PWM into an equivalent DC control voltage. The chosen cutoff frequency (≈19.4 Hz) ensured that only the average value of the PWM passed while attenuating high-frequency components by about 40 dB at the fundamental.

#### (b) Buffer Stage

A unity-gain op-amp buffer (ideal op-amp) was placed between the filter and current-sink stages to provide high input impedance and prevent filter loading. This ensured accurate voltage transfer to the next block.

#### (c) Op-Amp + NMOS Current Sink

The buffered DC voltage was applied to the non-inverting terminal of an op-amp that controlled the NMOS gate.

The op-amp regulated gate voltage such that the voltage drop across the sense resistor (Rₛₑₙₛₑ = 1 kΩ) equaled the control voltage, resulting in a proportional current:

Iout​=Rsense​Vctrl​​

Thus, the circuit behaved as a linear voltage-controlled current sink. A 60 V DC supply was used to allow sufficient headroom across the MOSFET and load.

#### (d) Simulation Setup

* **Transient Analysis:** .tran 0 0.3 0 100n used to capture PWM-to-DC transition and steady-state behavior.
* **FFT Analysis:** Performed on I(Rsense) to study harmonic suppression.
* **Compliance Test:** .step param Rload list 1k 2k 5k 8k 10k 12k 15k 20k 30k 40k 50k executed to determine maximum load for which current remains constant.
* **Measurement Commands:** .meas tran used for average, max, min, and RMS values of I(Rsense), V(ctrl), and V(sense).

### 5.2 Simulation Results

#### (a) PWM to DC Conversion

The PWM input (0–5 V, 200 Hz) was successfully filtered to a smooth DC voltage.

At 50% duty cycle, the average filter output Vctrl​ ≈ 2.5 V, as expected.

Ripple at the filter output was measured to be below **30 mV peak-to-peak**, consistent with theoretical attenuation of −40 dB at the PWM frequency.

#### (b) Buffer Output

The buffer preserved the filtered voltage with negligible phase delay or amplitude error.

This confirmed the op-amp follower was functioning ideally and not affecting the filter’s behavior.

#### (c) Current Sink Behavior

The current through Rsense, I(Rsense), followed the filtered voltage linearly.

Measured characteristics:

| **Parameter** | **Symbol** | **Typical Value** | **Remarks** |
| --- | --- | --- | --- |
| Average current (50% duty) | I\_avg | 2.5 mA | Matches theory (Vctrl/1kΩ) |
| Max current (100% duty) | I\_max | 5.0 mA | At Vctrl = 5 V |
| Ripple (p-p) | ΔI | ~30 µA | <1% of full-scale |
| Linearity | — | Excellent | 1 V ↔ 1 mA slope |

#### (d) FFT of Output Current

The FFT plot of I(Rsense) showed a dominant DC component and a rapidly decaying harmonic spectrum.

The 200 Hz fundamental was attenuated by approximately 40–45 dB, confirming strong filtering of PWM ripple.

Higher-order harmonics were well below −80 dB.

#### (e) Compliance Test Results

A parametric sweep of Rload demonstrated that the current source maintained accurate regulation up to **≈10 kΩ**, beyond which the MOSFET entered the linear (saturation-limited) region.

This matched analytical prediction from compliance voltage calculation.

| **Load Resistance (kΩ)** | **I(Rsense) (mA)** | **Regulation Status** |
| --- | --- | --- |
| 1 | 5.00 | Regulated |
| 5 | 5.00 | Regulated |
| 10 | 4.95 | Within limit |
| 15 | 3.90 | Begins to drop |
| 20 | 2.60 | Out of regulation |

## 6. Achieved Specifications vs. Target Specifications

| **Specification** | **Target Specification** | **Achieved (Simulated)** | **Status** |
| --- | --- | --- | --- |
| Input Voltage (V\_ctrl) | 0 - 5 V | 0 - 5 V | Met |
| Output Current (I\_out) | 0 - 5 mA | 0 - 5 mA | Met |
| Linearity | Linear | Linear (by inspection) | Met |
| Current Sense Resistor | 1 kΩ (Calculated) | 1 kΩ | Met |
| PWM Input | 200 Hz | 200 Hz | Met |
| Output Ripple Attenuation | > 40 dB (Typical) | > 60 dB | Exceeded |
| Load Supply (V\_sup) | - (Design choice) | 60 V | - |
| Compliance Limit (R\_load\_max) | > 8 kΩ (Typical Goal) | **10 kΩ** | Met |

## 7. Limitations and Trade-offs

* **Response Speed:** The primary trade-off is response speed vs. ripple. The 20 Hz cutoff filter effectively removes the 200 Hz ripple, but it also makes the VCCS slow to respond to changes in the control voltage. The system's settling time will be in the range of ~1 / (2 \* π \* f\_c) ≈ 80 ms.
* **Power Dissipation:** The NMOS transistor can dissipate significant power (up to 0.275 W) as heat, especially at low load resistances. This is inefficient and may require thermal management (a heat sink).
* **Unidirectional:** This design is a current *sink* (pulling current to ground). It cannot *source* (push) current to a load.

## 8. Future Improvements and Recommendations

* **Faster Response:** The response speed can be dramatically improved by increasing the PWM frequency (e.g., to 20 kHz, above audio range). This would allow for a higher filter cutoff frequency (e.g., 2 kHz), resulting in a much faster settling time.
* **Digital DAC Input:** For a ripple-free and near-instantaneous response, the PWM and filter could be replaced entirely with a parallel or serial Digital-to-Analog Converter (DAC).
* **Bidirectional Operation:** To create a VCCS that can both source and sink current, the NMOS stage could be replaced with a more complex topology, such as a Howland current pump or an op-amp driving a push-pull (Class B or AB) output stage.

## 9. Conclusion

The design and simulation in LTspice successfully demonstrate a functional and robust Voltage-Controlled Current Source. The circuit meets all primary objectives, delivering a linear 0–5 mA output current from a 0–5 V control input. The chosen topology of a PWM-driven, buffered, op-amp/NMOS sink proves effective, achieving excellent ripple suppression (>60 dB) and a wide compliance range up to 10 kΩ, thanks to the 60 V supply. The design calculations for Rsense and R\_load\_max were precisely validated by simulation. The key trade-off of this design is its slow transient response, a direct consequence of the low-frequency PWM input, which could be easily rectified by using a faster PWM or a DAC.

## 10. References

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