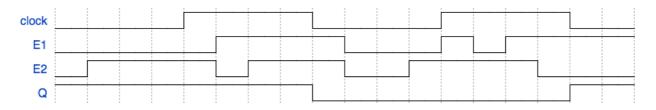


Circuitos Digitais - Prof. Marcelo Grandi Mandelli

Lista de Exercícios 7 – Latches e Flip-flops

1. A forma de onda abaixo descreve o comportamento de um flip-flop sem considerar o atraso. O valor de Q é inicializado em 1.



Qual a tabela verdade para esta forma de onda?

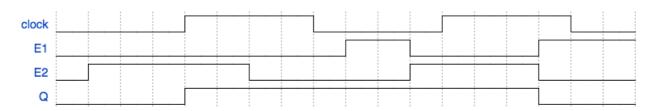
a)				
CLK	E1	E2	Q _{t+1}	
≠↑	Χ	Χ	Q	
↑	0	1	0	
1	1	0	1	
1	1	1	$\overline{Q_t}$	

	b)		
CLK	E1	E2	Q _{t+1}
≠↑	Χ	Χ	Q
↑	1	0	0
↑	0	1	1
↑	1	1	$\overline{Q_t}$

CLK	E1	E2	Q _{t+1}
≠↓	Χ	Χ	Q
\downarrow	0	1	0
\downarrow	1	0	1
\downarrow	1	1	$\overline{\mathbb{Q}_{t}}$

	d)		
CLK	E1	E2	Q _{t+1}
≠↓	Χ	Χ	Q
\downarrow	1	0	0
\downarrow	0	1	1
\	1	1	$\overline{Q_t}$

2. A forma de onda abaixo descreve o comportamento de um latch ou um flip-flop sem considerar o atraso. O valor de Q é inicializado em 0.



Qual a tabela verdade para essa forma de onda?

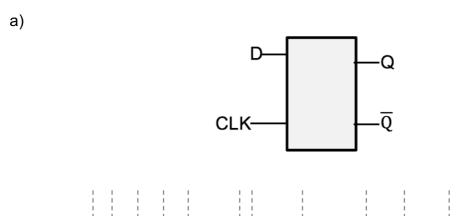
a)				
CLK	E1	E2	Q _{t+1}	
<u>≠</u> ↑	Χ	Χ	Q	
↑	0	0	Q	
\uparrow	0	1	0	
↑	1	0	1	
1	1	1	$\overline{Q_t}$	

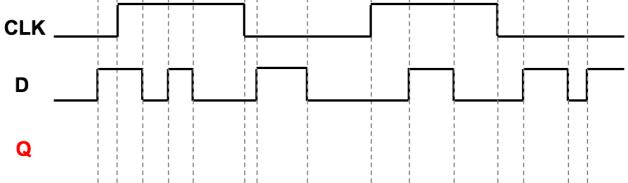
b)				
CLK	E1	E2	Q _{t+1}	
0	Χ	Χ	Q	
1	0	0	Q	
1	1	0	0	
1	0	1	1	
1	1	1	$\overline{Q_t}$	

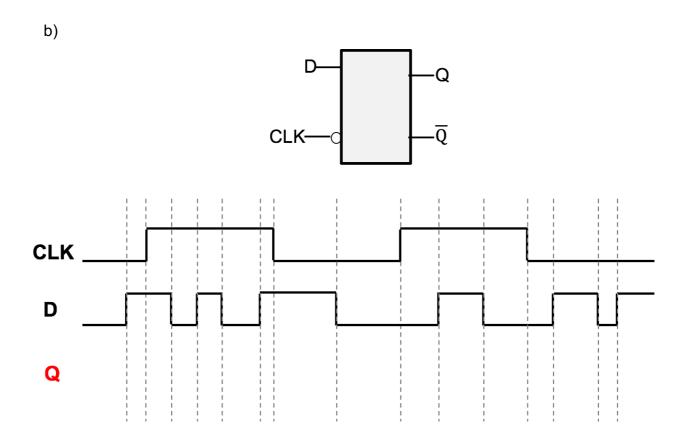
C)				
CLK	E1	E2	Q_{t+1}	
0	Χ	Χ	Q	
1	0	0	Q	
1	0	1	0	
1	1	0	1	
1	1	1	$\overline{Q_t}$	

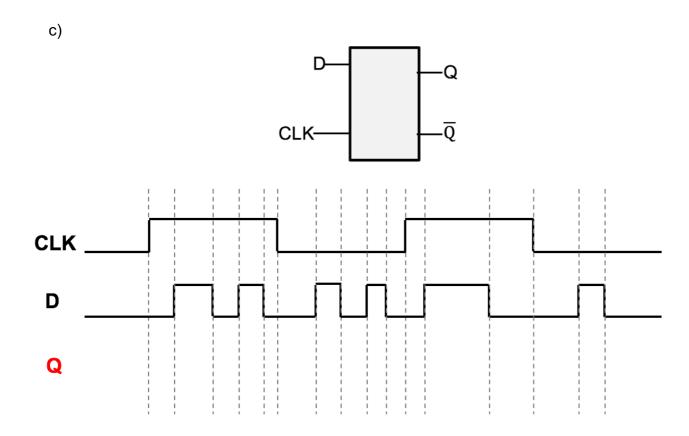
d)				
CLK	E1	E2	Q_{t+1}	
≠↑	Χ	Χ	Q	
1	0	0	Q	
1	1	0	0	
1	0	1	1	
1	1	1	<u>O</u> +	

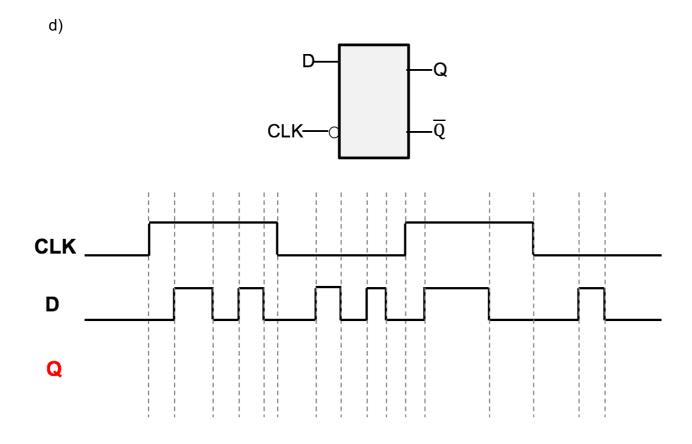
3. Complete as formas de onda dos circuitos a seguir (desconsidere o atraso).

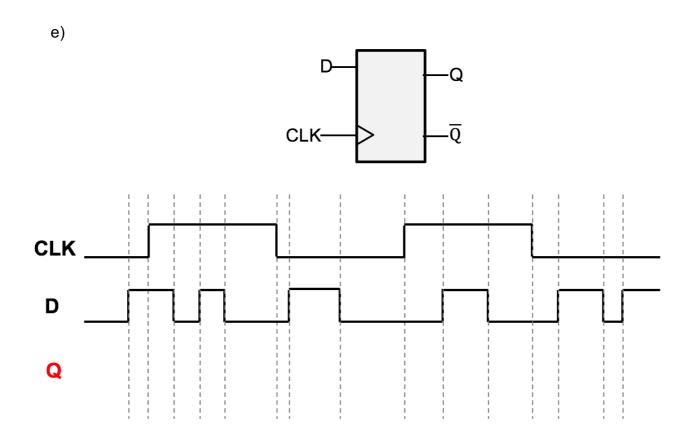


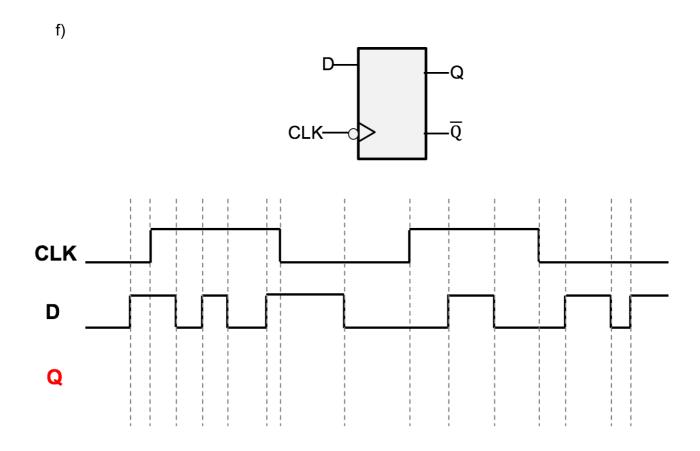


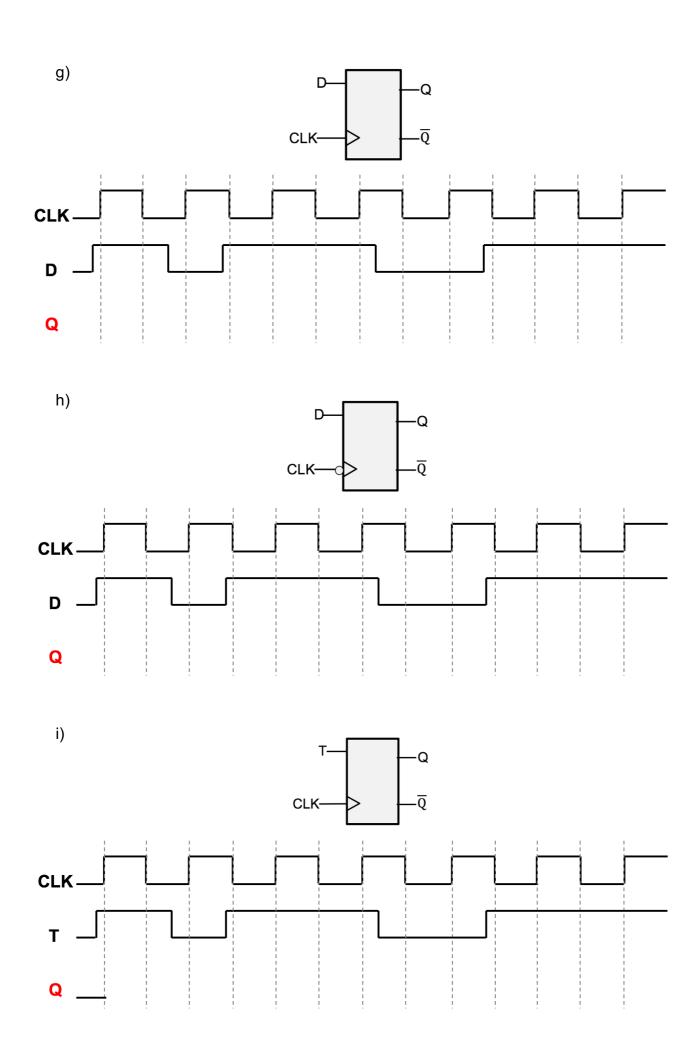


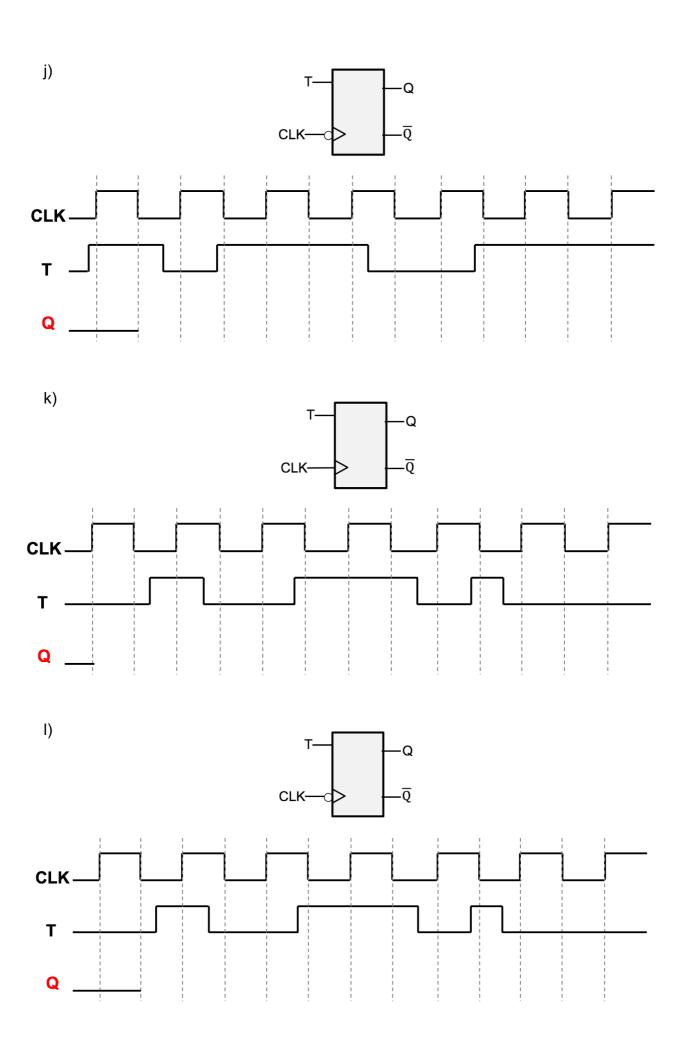


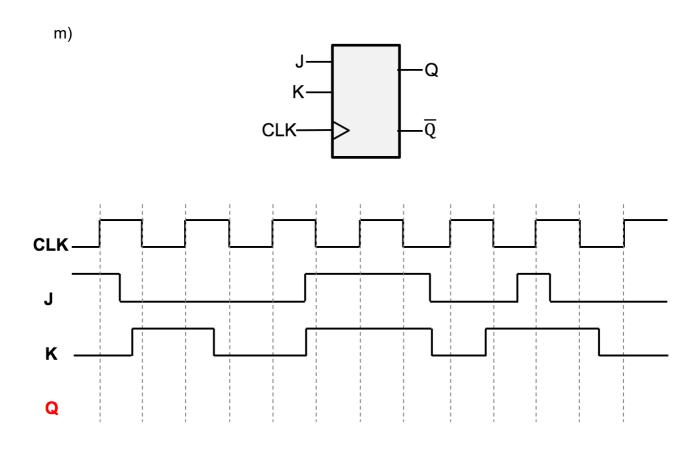


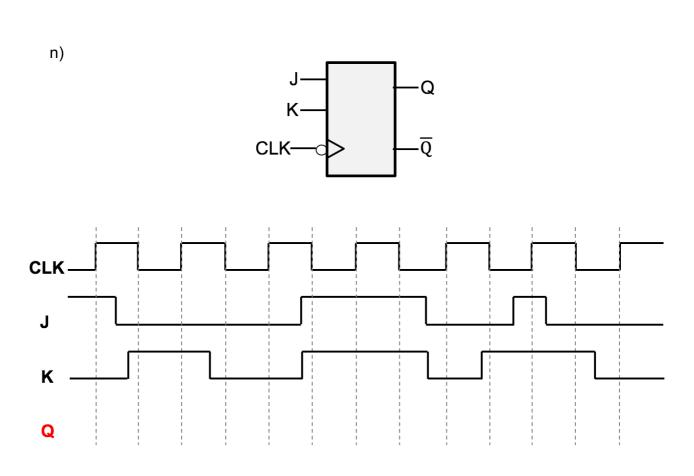


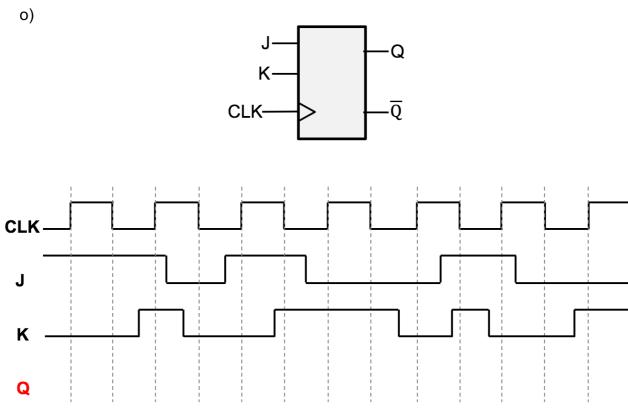


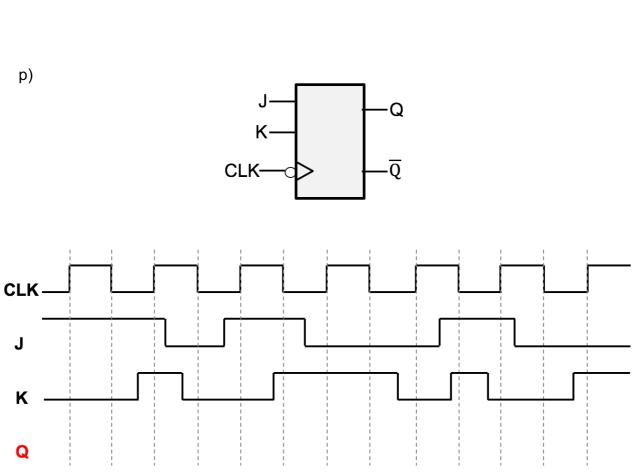




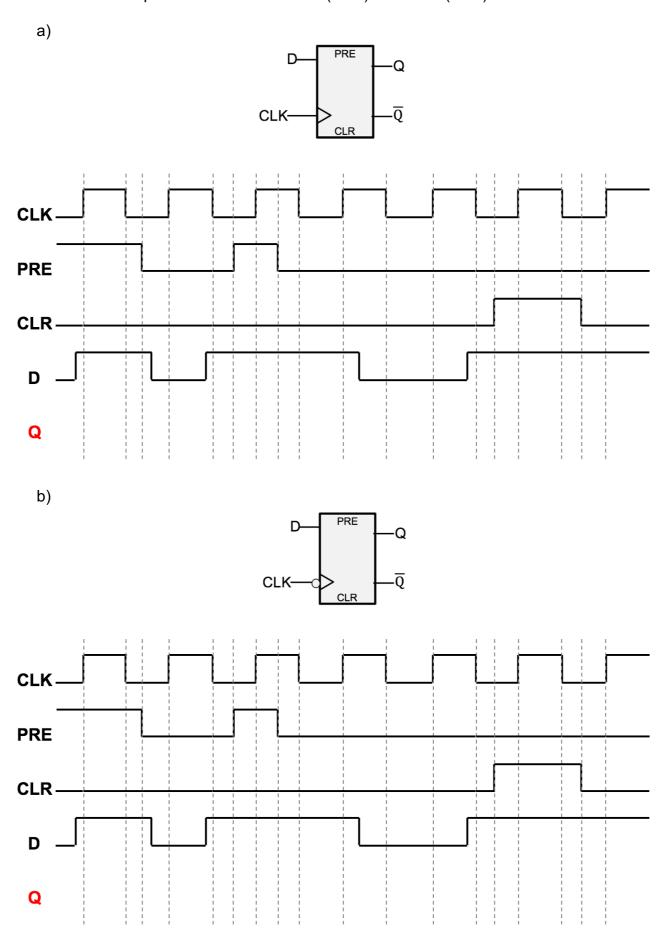


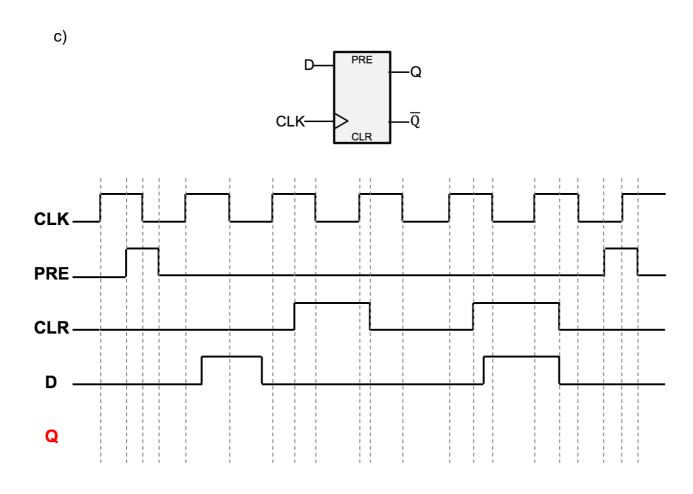


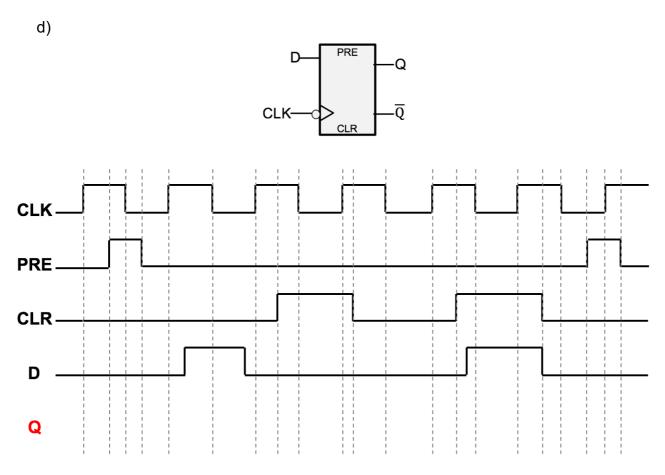


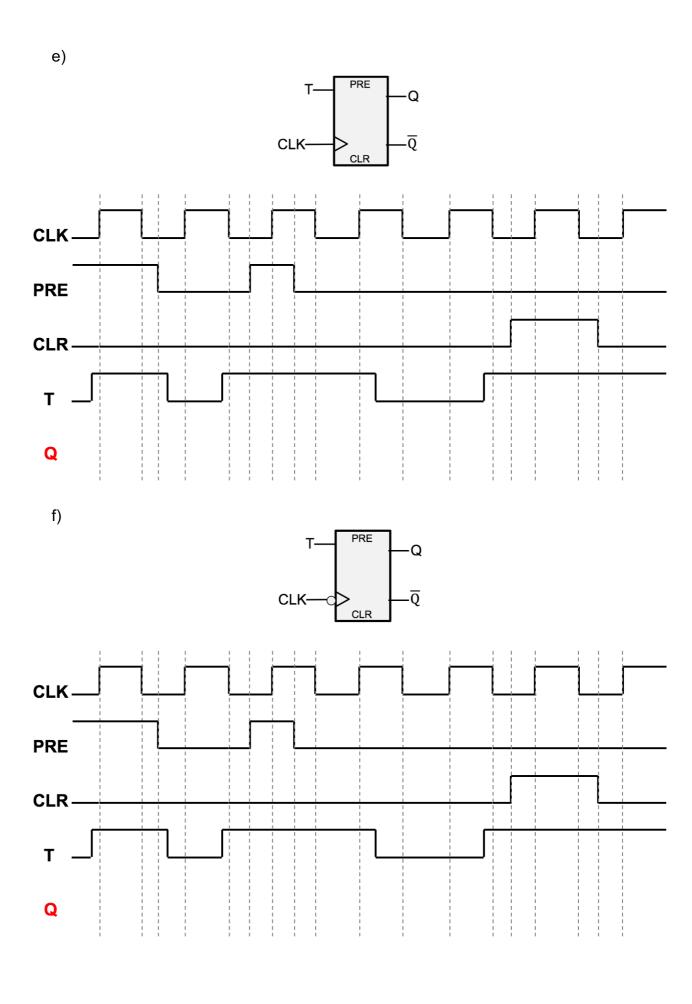


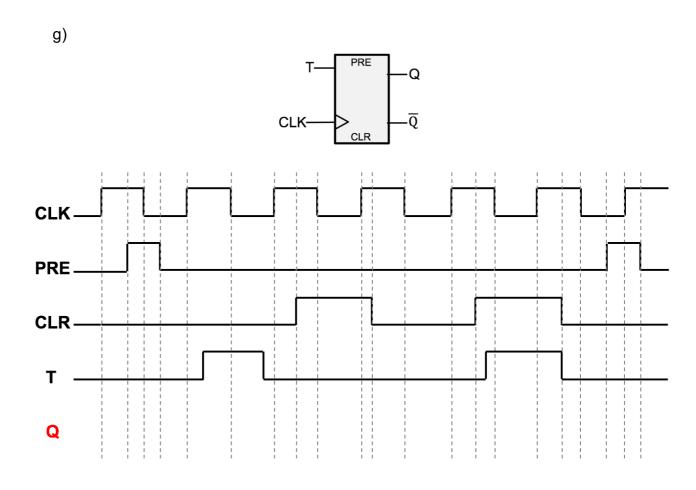
4. Complete as formas de onda dos circuitos a seguir (desconsidere o atraso). Considere que as entradas PRESET (PRE) e CLEAR (CLR) são ativas em 1.

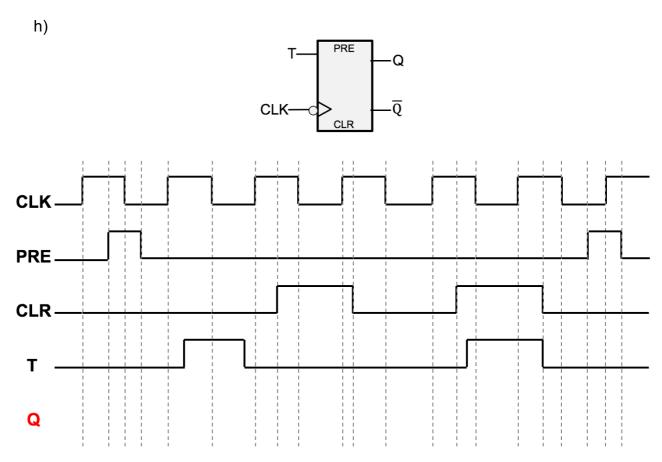


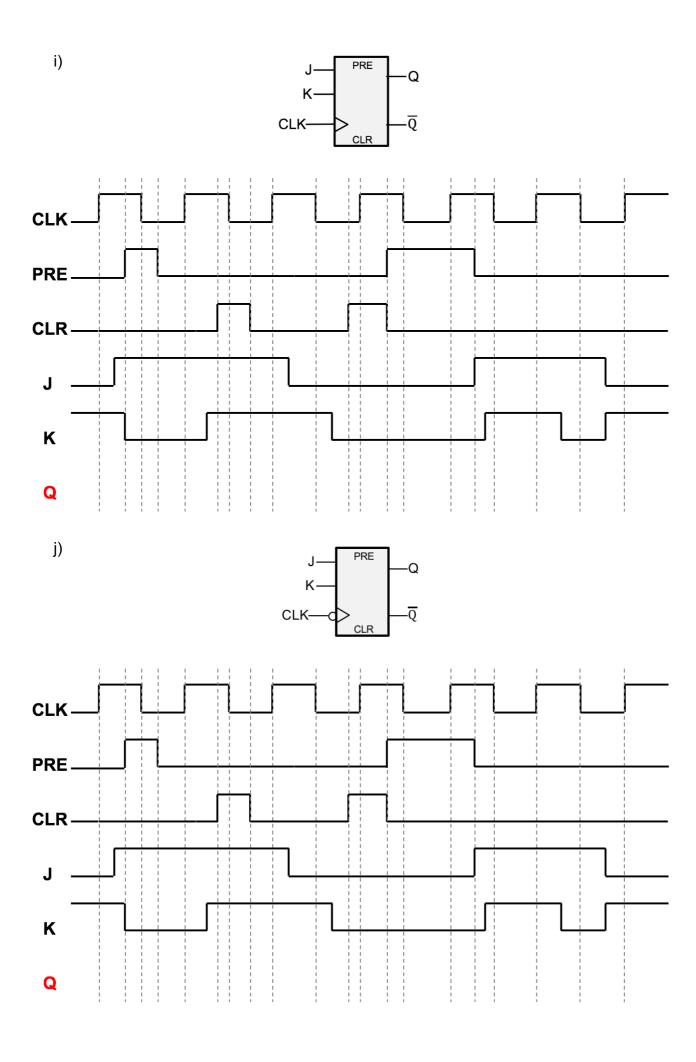


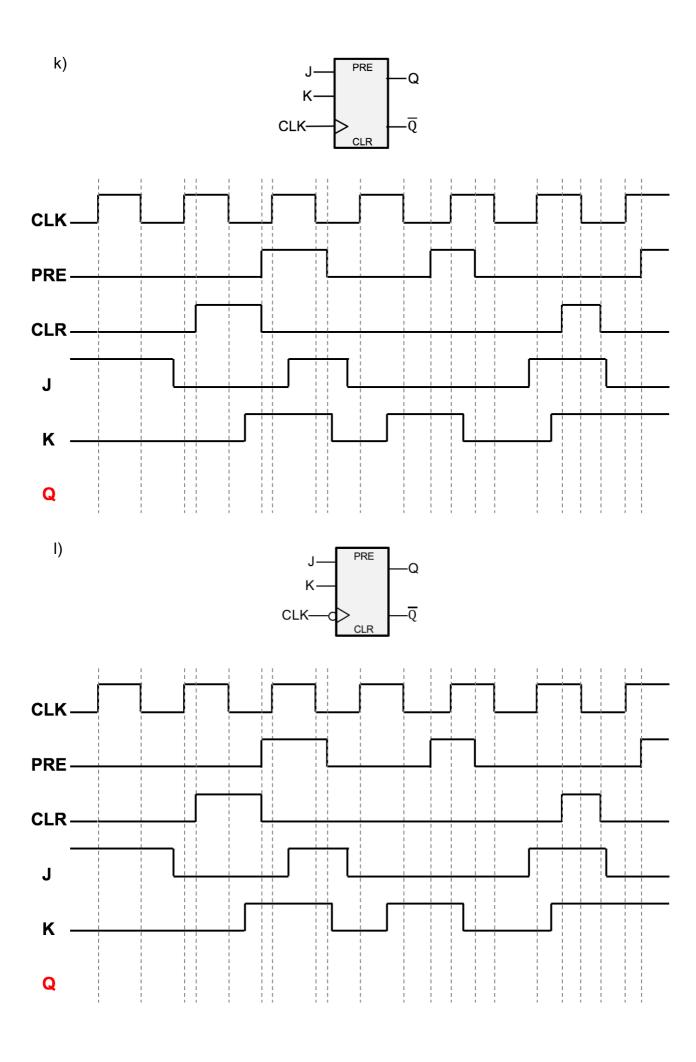








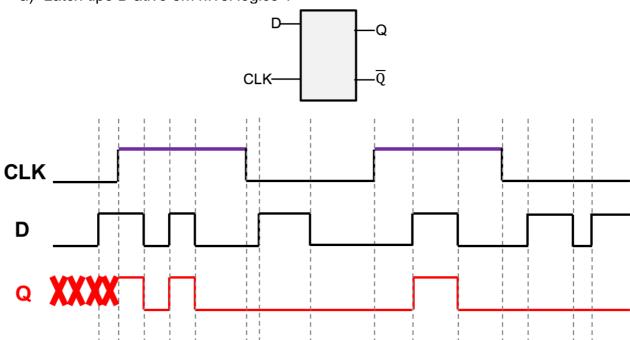




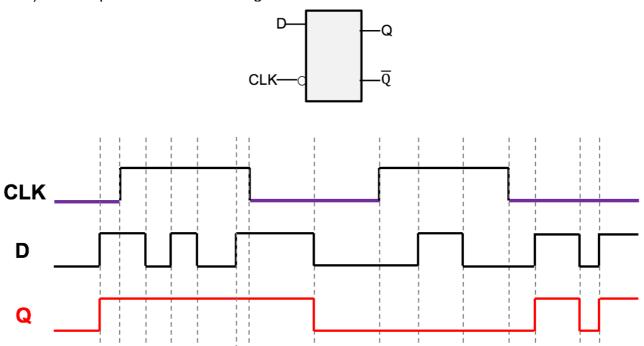
GABARITO

- 1. c)
- 2. b)
- 3.

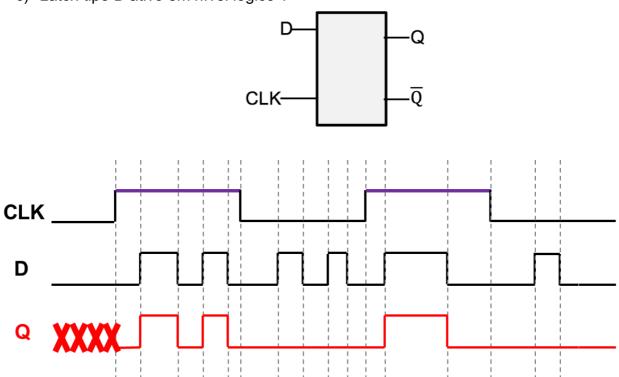
a) Latch tipo D ativo em nível lógico 1



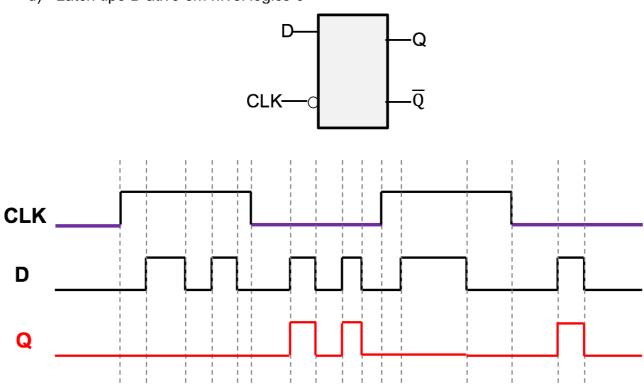
b) Latch tipo D ativo em nível lógico 0



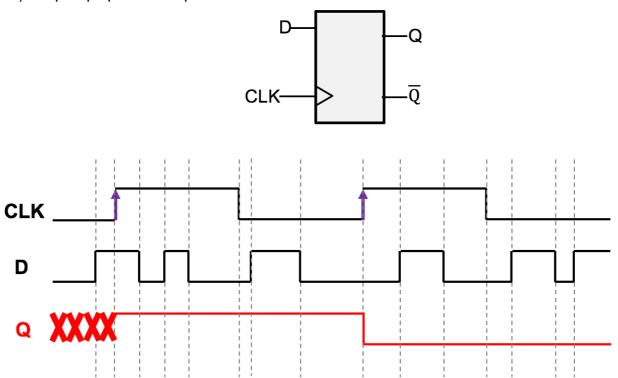
c) Latch tipo D ativo em nível lógico 1



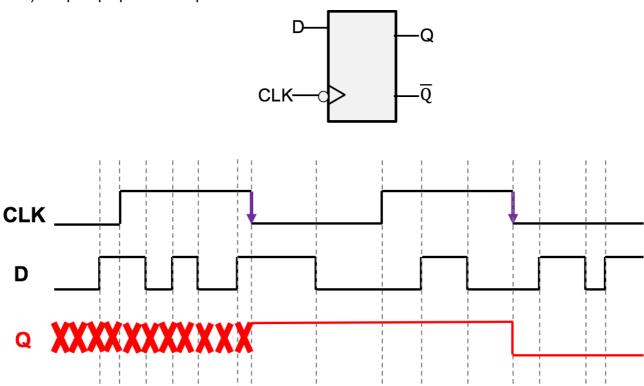
d) Latch tipo D ativo em nível lógico 0



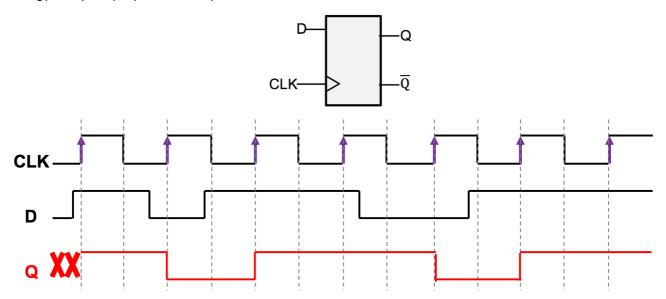
e) Flip-flop tipo D ativo por borda de subida



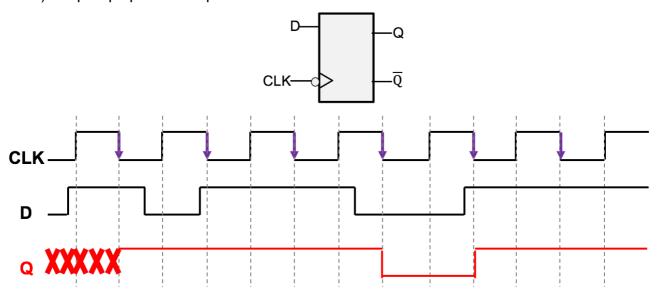
f) Flip-flop tipo D ativo por borda de descida



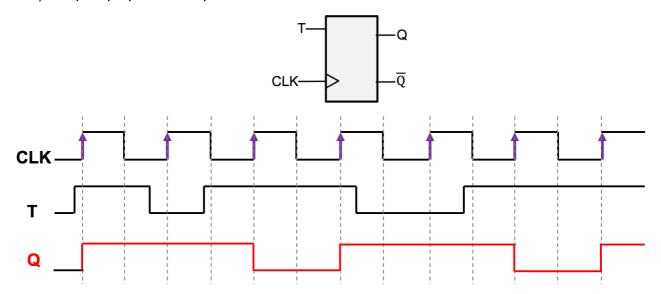
g) Flip-flop tipo D ativo por borda de subida



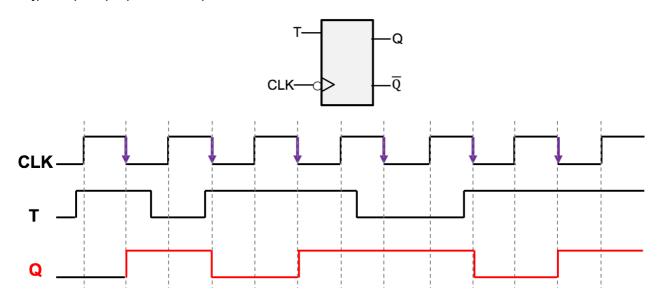
h) Flip-flop tipo D ativo por borda de descida



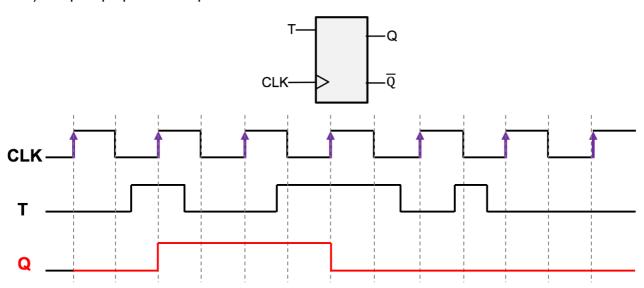
i) Flip-flop tipo T ativo por borda de subida



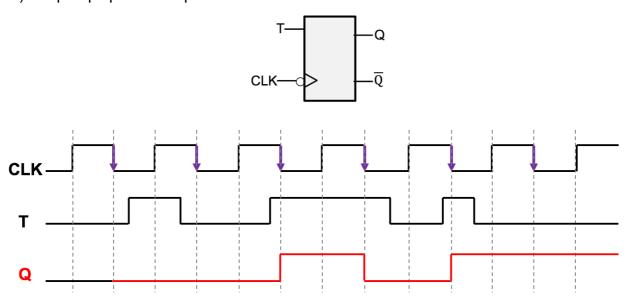
j) Flip-flop tipo T ativo por borda de descida



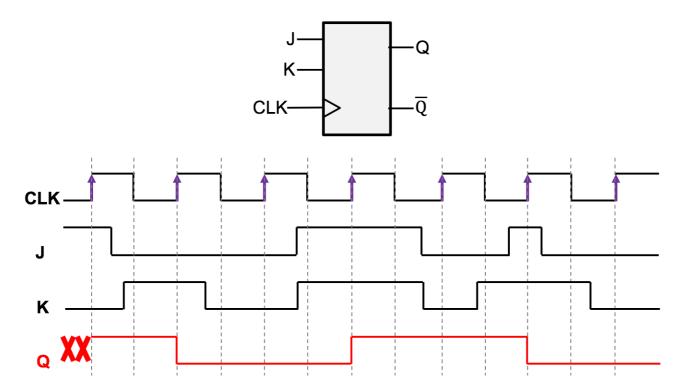
k) Flip-flop tipo T ativo por borda de subida



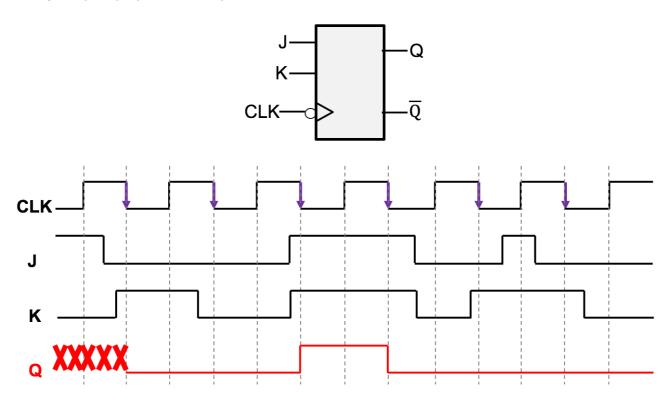
I) Flip-flop tipo T ativo por borda de descida



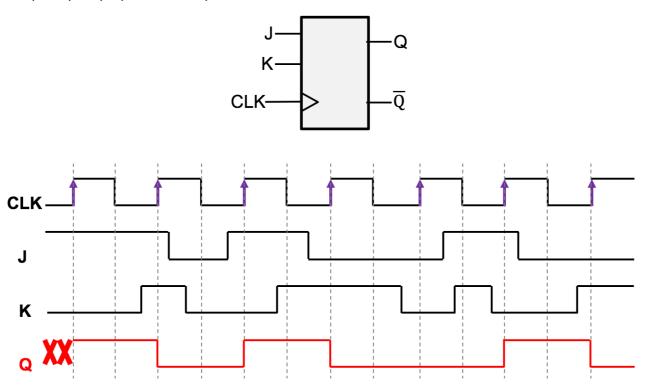
m) Flip-flop tipo JK ativo por borda de subida



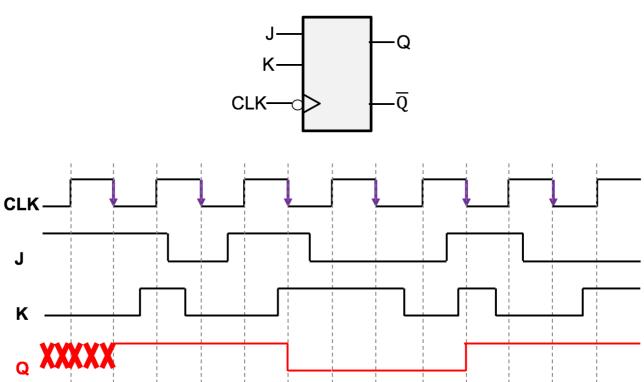
n) Flip-flop tipo JK ativo por borda de descida



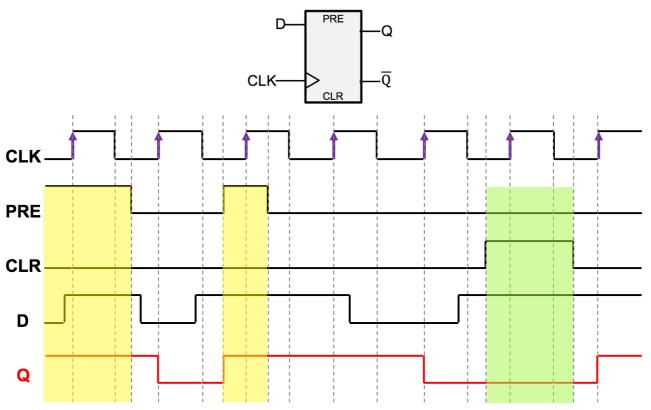
o) Flip-flop tipo JK ativo por borda de subida



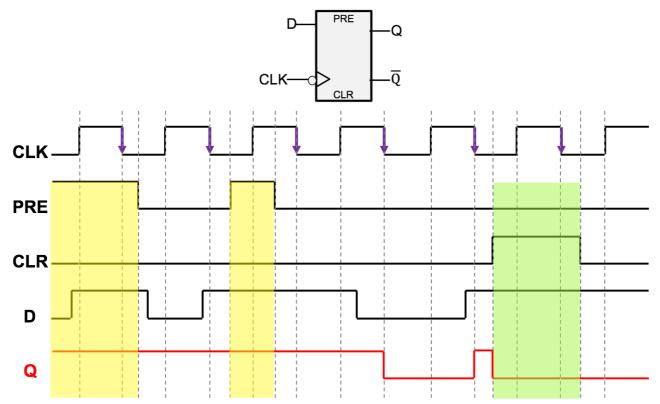
p) Flip-flop tipo JK ativo por borda de descida



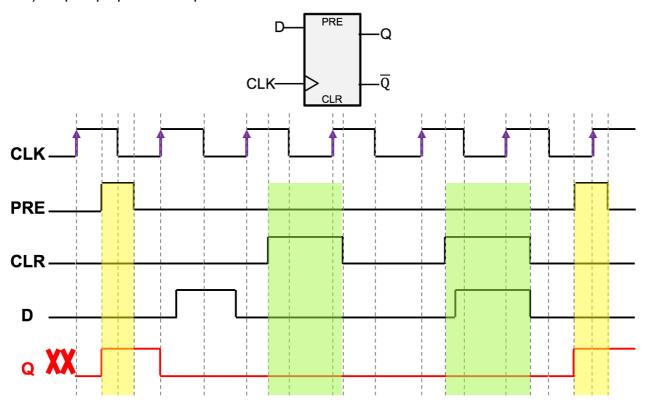
a) Flip-flop tipo D ativo por borda de subida



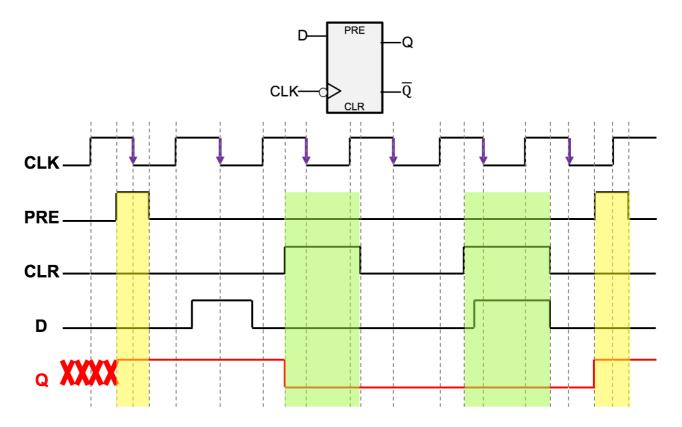
b) Flip-flop tipo D ativo por borda de descida



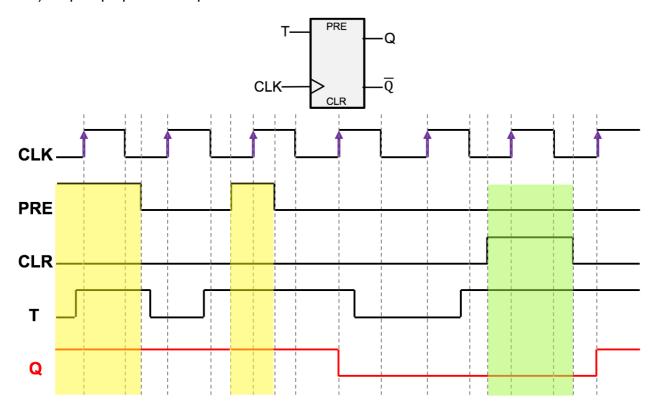
c) Flip-flop tipo D ativo por borda de subida



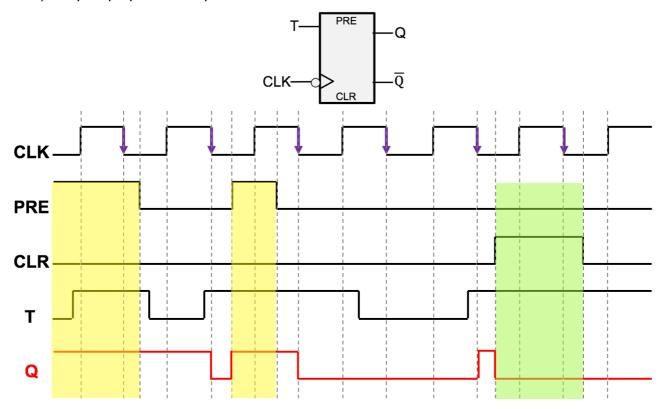
d) Flip-flop tipo D ativo por borda de descida



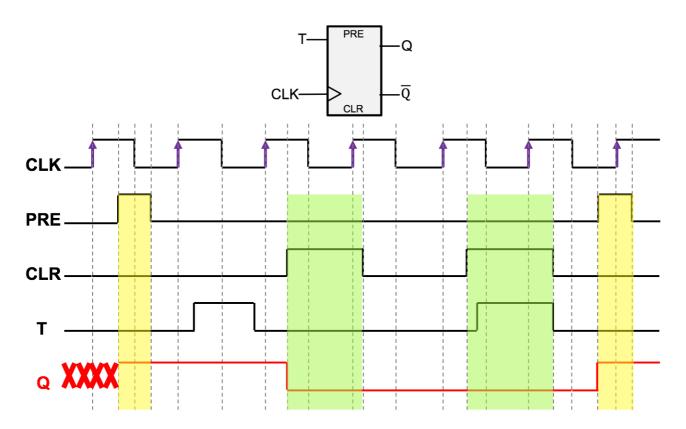
e) Flip-flop tipo T ativo por borda de subida



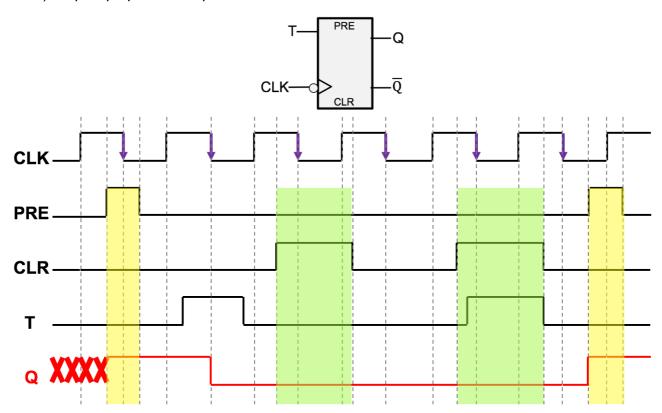
f) Flip-flop tipo T ativo por borda de descida



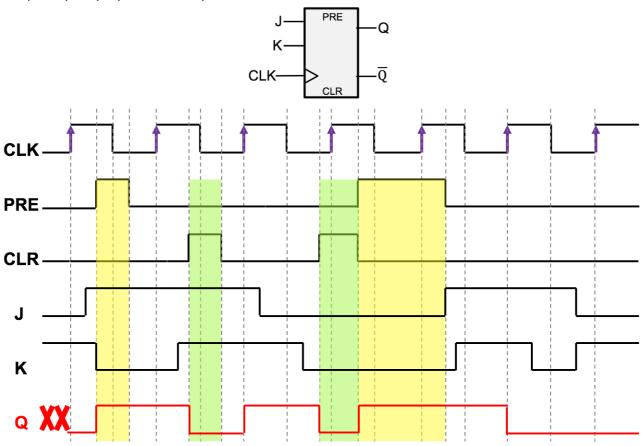
g) Flip-flop tipo T ativo por borda de subida



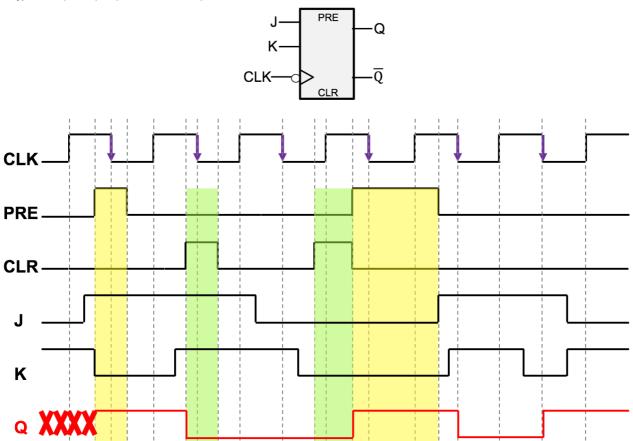
h) Flip-flop tipo T ativo por borda de descida



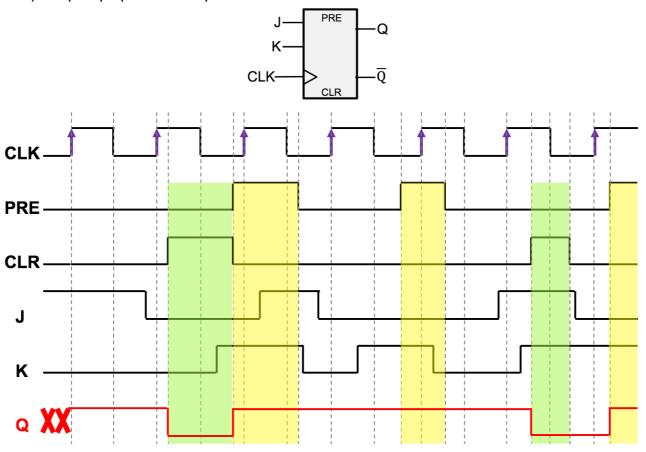
i) Flip-flop tipo JK ativo por borda de subida



j) Flip-flop tipo JK ativo por borda de descida



k) Flip-flop tipo JK ativo por borda de subida



I) Flip-flop tipo JK ativo por borda de descida

