PS-Q RAM:
Bosonic Quantum Memory in a Photonic-Crystal Supersolid

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June 30, 2025

Abstract

We propose PS-Q RAM, a cryogenic bosonic quantum memory based on a Kerr-stabilized polariton cat state in a GaAs photonic-crystal cavity. By engineering two-photon drives and losses, PS-Q RAM stores logical qubits as superpositions of global condensate phases, achieving autonomous error protection, sub-100 µs coherence, and 100 ns-scale SWAP gates to superconducting qubits. This white paper outlines device physics, design architecture, simulation results, and a first-light experimental roadmap.

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1 Introduction

Quantum processors require fast, high-fidelity memory at millikelvin temperatures. Conventional SRAM/DRAM fail below 4 K, and room-temperature quantum memories introduce latency. PS-Q RAM bridges this gap by storing qubit states in an all-optical, bosonic cat code realized within a GaAs photonic-crystal cavity.

2 Operating Principle

PS-Q RAM encodes a logical qubit in the coherent superposition

$$|C_{\pm}\rangle = \mathcal{N}_{\pm}(|\alpha\rangle \pm |-\alpha\rangle),$$

where α is the polariton amplitude. A two-photon resonant drive ϵ_2 and engineered two-photon loss κ_2 autonomously stabilize $|C_\pm\rangle$ against single-photon decay.

3 Device Architecture

3.1 Photonic-Crystal Cavity

A GaAs membrane hosts a high-Q nanobeam cavity (mode volume $V \sim (\lambda/n)^3$, $Q \geq 5 \times 10^6$) etched with elliptical holes. Underneath, a 20.5-pair AlGaAs/GaAs DBR suppresses radiative loss.

3.2 Pump and Loss Engineering

Two laser tones at $\omega_c/2$ drive the two-photon process, while an integrated superconducting nanowire provides engineered κ_2 via photon conversion to quasiparticles.

4 Numerical Simulation

We solve the Lindblad master equation

$$\dot{\rho} = -\frac{i}{\hbar}[H, \rho] + \kappa_1 \, \mathcal{D}[a]\rho + \kappa_2 \, \mathcal{D}[a^2]\rho,$$

with

$$H = \hbar\Delta \, a^\dagger a + \frac{\hbar K}{2} \, a^{\dagger 2} a^2 + \frac{\hbar \epsilon_2}{2} \, (a^{\dagger 2} + a^2),$$

yielding cat-state fidelity $F > 0.9$ within 5 µs and coherence $T_2 \geq 100$ µs for $\alpha \approx 3$.

5 Performance Targets

- **Coherence:** $T_{2,\text{cat}} \geq 100$ µs at 10 mK.
- **Gate speed:** SWAP to transmon in 100 ns with fidelity $\geq 99\%$.
- **Power:** < 1 µW per qubit.
- **Density:** ~ 1000 qubits cm^{-2} on a 10 mm reticle.

6 Experimental Roadmap

1. Fabricate single nanobeam cavity, measure $Q \geq 5 \times 10^6$.
2. Demonstrate two-photon stabilization and cat formation via Wigner tomography.
3. Integrate superconducting qubit swap line; benchmark 100 ns SWAP.
4. Scale to a 4×4 array; verify $T_2 > 100$ µs across all sites.

7 Conclusion

PS-Q RAM offers a path to local, error-protected quantum memory at millikelvin temperatures. Its integration with superconducting processors promises to reduce latency, improve error-correction cycles, and accelerate hybrid quantum-classical algorithms.

References

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