

TRIBHUVAN UNIVERSITY
 INSTITUTE OF ENGINEERING
Examination Control Division
2081 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT,BEI	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.



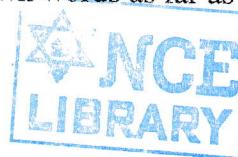
1. Distinguish between computer organization and architecture. Explain instruction cycle state diagram with interrupt handling. [3+3]
2. Write down the code to evaluate $Y=(A-B/C^*[D+(E^*G)])$ in three address, two address, one address and zero address instruction format. [8]
3. Explain the data transfer instruction with example. Differentiate between Immediate and direct addressing modes. [4+4]
4. Write a microprogram for the fetch cycle and addition cycle. Explain the microinstruction format with example. [5+5]
5. What is pipelining? Describe four stage instruction pipeline. Explain the Flynn's classification of computer system. [1+4+4]
6. Draw a flowchart for Booth's multiplication algorithm for signed multiplication. Multiply -6×7 using Booth's multiplication algorithm. [5+5]
7. Explain the floating-point addition and subtraction process with example. [3+3]
8. Describe the cache memory principles. Differentiate between direct mapping and set associative mapping. [3+5]
9. Compare and contrast between programmed I/O and interrupt driven I/O. Explain the CPU and IOP communication channel using diagram. [5+5]
10. Briefly discuss on inter-processor communication and synchronization. [5]

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 2081 Baishakh

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1. Explain instruction cycle state diagram. Describe PCI bus configuration. [3+3]
2. Write program for $N = ((P-Q \times R)/S) + ((T/U) + V \times W)$ using three address, two address, one address and zero address instruction format. Consider N, P, Q, R, S, T, U, V and W as memory locations. [8]
3. Write down the different types of addressing modes and explain each of them with advantages and disadvantages. [8]
4. Explain the micro instruction format. Difference between symbolic and binary micro instruction. [4+4]
5. Construct time-space diagram for four instructions with four-stage pipeline and show how pipelining reduces the execution time? Explain arithmetic pipeline for solving floating-point addition/subtraction. [5+5]
6. Draw the flowchart for Restoring Division. Divide $\frac{11}{5}$ using restoring division. [4+6]
7. Multiply $10 \times (-7)$ using Booth's multiplication algorithm. [6]
8. Explain in briefly the characteristics of a memory system. Differentiate between direct mapping and set associative mapping. [3+7]
9. Why IOP is used in input-output organization? With the help of a neat diagram, explain how DMA technique is used to transfer data in a computer system. [3+7]
10. Discuss about loosely-coupled and tightly-coupled architecture. [4]

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 2080 Bhadra

Exam.	Regular		
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Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

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1. Discuss about the usage of a Multiple Hierarchical Bus Architecture over single bus system. [6]
2. Design a 1-bit ALU which can perform addition, AND, OR, and X-OR operations. Explain the different types of instruction formats. [4+4]
3. What is addressing mode? Explain about the different types of addressing modes with suitable example. [2+6]
4. Explain address sequencing with the help of a block diagram. Describe micro-instruction format in detail. [5+3]
5. Show that the Speedup factor for a Pipelined Processor is equal to the number of stages in a pipeline. Explain about the different types of conflicts that can be seen in a pipeline. [4+6]
6. Explain booth's algorithm. Multiply (9×4) using Booth's multiplication algorithm. [4+6]
7. Compare restoring division algorithm with non restoring division algorithm. [6]
8. Explain direct Cache mapping technique with example. Explain different write policy techniques in cache memory. [7+3]
9. Explain three I/O techniques for input of a block of data. Show the role of I/O processor to assist the operation of the CPU. [6+4]
10. List out the characteristics of a Multiprocessor. [4]

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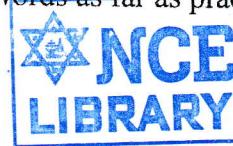
1. Define structure and function of a computer system. Draw instruction cycle state diagram with interrupt. [4+2]
2. Write down the code to evaluate $X = \frac{A - B + C \times (D \times E - F)}{G + H \times k}$ in three address, two address, one address and zero address instruction formats. [8]
3. What are the different types of addressing modes? Compare them with advantages and disadvantages. [2+6]
4. Differentiate between hardwired and micro programmed control unit. Explain with block diagram of micro programmed control unit. [5+5]
5. How can we prove that pipelining improves the performance of a computer? Explain the operation of instruction pipeline for processing four segment instruction cycle with the help of space-time diagram. [4+6]
6. Explain non-restoring division algorithm with flow chart and also divide 12/5 using same algorithm. [5+5]
7. Multiply -6×7 using Booth's multiplication algorithm. [6]
8. What is set associative mapping? Explain how it combines the feature of direct and associated mapping technique. Explain different replacement algorithm techniques used in cache memory. [2+3+3]
9. Explain CPU-IOP Communication with diagram. Explain DMA controller with suitable block diagram. [5+5]
10. Explain the crossbar switch interconnection structure with block diagram. [4]

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2079 Bhadra

Exam.	Regular		
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Subject: - Computer Organization and Architecture (CT 603)

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1. Explain about the structural and functional viewpoint of a computer. Explain different elements of bus design. [4+2]
2. Write a code for $X = ((A+B)/C) + (D - E)$ using three addresses, two addresses, one address and zero address instruction format. [8]
3. List out the different types of addressing modes and explain each of them with suitable example. [8]
4. Describe the operation of hardwired control unit with a typical block diagram. Explain the operation of microprogram sequencer used in microprogrammed control unit. [5+5]
5. Explain arithmetic pipelining with example. Describe different types of pipeline hazards with example. [4+6]
6. Draw the flowchart for Non-Restoring Division. Perform 13/5 using restoring division. [4+6]
7. Explain floating point addition and subtraction algorithm with an example. [6]
8. Describe how Set-Associative Mapping works in Cache memory mapping. Explain different write policy techniques in cache memory. [3+5]
9. Elaborate the roles of I/O interface in a computer system. Explain how data transfer is performed with programmed I/O technique with necessary diagram. [10]
10. Compare and contrast the interconnection structures used in multiprocessing environment. [4]

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2078 Bhadra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BEI, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
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1. Explain different types of bus arbitration and compare them. [6]
2. Explain different types of data manipulation instructions with example. [8]
3. Explain the component of CPU. Comparison between RISC and CISC architecture. [2+6]
4. Explain the organization structure of a microprogram control unit and the generation of control signals using microprogram. [10]
5. What is meant by hazard in pipelining? Explain with example data and control hazards in pipeline conflict. [4+6]
6. Explain the non-restoring division algorithm for division. Divide 10/5 using non-restoring division. [5+5]
7. Explain the floating point addition and subtraction process using flow chart. [3+3]
8. Explain Least Recently Used (LRU) replacement algorithm in case of hit and miss with suitable example. [8]
9. Differentiate between isolated and memory mapped Input-output. Explain with block diagram of DMA transfer in a computer system. [4+6]
10. Compare and contrast the interconnection structures used in multiprocessor system. [4]

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 2078 Kartik

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
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1. Differentiate between computer organization and architecture. Compare and explain the bus structure of typical computer system. [2+4]
2. Write down the code for $Y = (A-B/C) \times (D+E \times G) / F$ using three address, two address, one address and zero address instruction format. [8]
3. Comparison between different types of addressing modes with its advantages and disadvantages. [10]
4. Write down the symbolic microprogram for fetch routine and addition execute routine. Explain with diagram the working of microprogram sequencer for control memory. [4+6]
5. How pipeline processing is done in an instruction pipeline? Explain four segment instruction pipeline with timing diagram. [3+5]
6. Describe the procedure for floating point addition and subtraction with help of flowchart and example. [6]
7. Draw the flowchart of Booth's multiplication algorithm and multiply -7×-10 using Booth's multiplication algorithm. [4+4]
8. Explain various mapping methods used in cache memory organization and compare each of them with example. [10]
9. Explain with block diagram of DMA controller. How DMA techniques is different from programmed Input-Output? [6+4]
10. Differentiate between tightly coupled multiprocessor and loosely coupled multiprocessor. [4]

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 2076 Chaitra

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

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1. Draw the instruction cycle state diagram with example. [6]
2. Write down the code to evaluate $Y = (A - B/C)*[D + (E*G)]$ in three address, two address, one address and zero address instruction formats. [8]
3. Define addressing modes. Mention the different types of addressing modes and comparison between them. [2+6]
4. How address of micro instruction is generated by next address generator in control unit? Explain with suitable diagram. [8]
5. Explain four stage instruction pipeline and also draw a time-space diagram for four segments having six tasks. [10]
6. Explain the Booth's algorithm for multiplication. Multiply $10 \times (-5)$ using Booth's multiplication algorithm. [5+5]
7. Comparison between restoring and non-restoring division algorithms with example. [6]
8. Define cache mapping techniques. Explain direct mapping technique with suitable diagram. Why replacement algorithm is necessary in associative mapping? Justify. [2+4+4]
9. Comparison between program I10, Interrupt driven I10 and direct memory access. Why data communication processor is required in an I10 organization. [8+2]
10. Discuss about hypercube interconnection network with example. [4]

TRIBHUVAN UNIVERSITY
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 2076 Ashwin

Exam.	Back		
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Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

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1. What is PCI? Explain the design goals and performance metrics for a computer system regarding its organization and architecture. [1+5]
2. Write the arithmetic statement $Y=(W+X)*(Y-Z)$ using Zero, One, Two and Three address instruction format. [8]
3. Explain the different types of addressing modes and compare each of them. [8]
4. Explain block diagram of micro-programmed control organization. Describe various fields in micro-instruction format with diagram showing different fields. [4+6]
5. Describe the hazard in a pipeline. Explain the different types of hazards. How can these be overcome? [2+4+2]
6. Write an algorithm of booth multiplication. Perform 8×4 using booth multiplication algorithm. [10]
7. Differentiate between restoring division and non-restoring division and non-restoring division algorithm. [6]
8. Describe cache operation in briefly. Explain about associative mapping technique. Give reasons why replacement algorithm is not required in direct mapping technique. [2+6+2]
9. Explain the DMA operation with block diagram. How does DMA have request over the CPU when both request a memory transfer? [8+2]
10. Discuss about tightly-coupled multiprocessor with block diagram. [4]

TRIBHUVAN UNIVERSITY
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Examination Control Division
2075 Chaitra

Exam.	Regular / Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT 603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
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1. Define computer architecture. Discuss the limitations of using single bus system to connect different devices. What does width of address bus represent in a system? [2+2+2]
2. Design an 2-bit ALU that can perform subtraction, AND, OR and XOR. [8]
3. Write a code for $Y=(A+B)/C + D/(E*F)$ using three address, two address, one address and zero address instruction format. [8]
4. Differentiate hardwired and micro-programmed control unit. Draw and explain block diagram of micro-programmed sequencer for control memory. [10]
5. Derive expression showing speed up ratio equals number of segments in pipeline. Discuss in detail about data dependency problem that arises in pipelining along with its solution. [3+5]
6. Write an algorithm for non restoring division. Perform the 10/3 using restoring division algorithm. [3+7]
7. Multiply -6×-11 using Booth's Multiplication algorithm. [6]
8. Write characteristics of memory system? Suppose main memory has 64 blocks and cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [4+6]
9. Explain three reasons behind the requirement of I/O interfaces. Why memory address spaces are reduced memory mapped I/O? Describe DMA controller with suitable block diagram. [3+2+5]
10. Explain inter-processor synchronization with example. [4]

Exam.	Back		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. Explain the Interconnection structures of computer. [6]
2. Write codes for given operation using zero, one, two and three address instruction format. [8]
3. Differentiate between RISC and CISC architecture. [6]
4. Draw the diagram of Micro-programmed sequencer for a control memory and explain it. [10]
5. Explain six stage instruction pipeline with example. [10]
6. Explain Booth's multiplication algorithm for signed 2's complement numbers in details with a suitable example and give the hardware requirements diagram. [10]
7. Differentiate between restoring and non-restoring division. [6]
8. Explain the various types of elements of cache design and also explain the various mapping techniques used in cache with example. [4+6]
9. Why ILO processor is needed in ILO organization? Explain the CPU-IOP communication with diagram. [3+7]
10. Write down the characteristics of multiprocessors. [4]

Exam.		Regular	
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Subject: - Computer Organization and Architecture (CT603)

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1. Draw instruction cycle, state diagram with interrupt and explain it. [6]
2. Write down the need for addressing modes. Explain the various addressing modes with example. [8]
3. Write the arithmetic statement
 $X = (P+Q) \times (R+S)$ using zero, one, two and three address instruction format [8]
4. Compare and contrast between hardwired and microprogrammed control unit. Explain the micro program sequencer used in microprogrammed control unit. [4+6]
5. What is pipeline? How performance of computer is increased using pipelining? Explain with example. [2+6]
6. Perform multiplication - 7×3 using booth algorithm. [6]
7. Explain the process of floating point number addition and subtraction with flowchart and example. [10]
8. Write down the characteristics of memory system. Suppose main memory has 32 blocks and cache memory has 8 blocks when 12 blocks of main memory are used, show how mapping is performed in direct mapping. [4+6]
9. Explain I/O Interface. Compare programmed I/O, Interrupt driven I/O and direct memory access (DMA). [2+8]
10. Explain various configurations of OS in multiprocessor system. [4]

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
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1. What do you mean by interconnection structure? Explain different types of interconnections indeed required in Computer Architecture. [2+4]
2. Write a code for $Y = A * (B + D/C) + (G * E)/F$ using three addresses, two address, one address and zero address instruction format. [8]
3. Following instructions are given: [10]
 - i) LDA 2000H
 - ii) MVI B, 32H
 - iii) STAX D
 - iv) MOV A, B

Which addressing modes are used in the above instructions? Explain briefly about them.

4. Explain microinstruction format used in microprogramming Control unit and write micro program for fetch cycle. [6+4]
5. Explain in detail how the arithmetic pipeline increases the performance of a system. [7]
6. "RISC has the ability to use efficient instruction pipeline". Justify the statement. [3]
7. Explain signed binary division algorithm. Use the non-restoring division algorithm to devide 15 by 4. [8]
8. Explain floating point addition and subtraction algorithm with example. [6]
9. Describe how set associative mapping combines the feature of direct and associated mapping technique. Explain different write policy techniques in cache memory. [5+3]
10. Why input-output processor is needed in an input-output organization? How does a computer know which device issued the interrupt; if multiple devices, how does the selection take place? [5+5]
11. Describe how the multiprocessor systems increase the performance level and reliability. [4]

Exam.	Regular		
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Subject: - Computer Organization and Architecture (CT603)

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1. Define computer architecture and computer organization. How can we maintain a performance balance between processor and memory? Discuss the limitations of using single bus system to connect different devices in any given system. [2+2+2]
2. What do you mean by instruction format? Write codes for given operation using 3-,2-,1- and 0- address instruction format. [4+8]

$$X = (A - B * F) * C + D / E$$
3. Differentiate between RISC and CISC. [6]
4. What factors cause micro-programmed control unit to be selected over hardwired control unit. Explain with relevant block diagram, how address of control memory is selected in micro-programmed control unit. [3+7]
5. Describe Flynn's classification. Explain control pipeline hazard and its solutions. [4+6]
6. Explain Booth's multiplication hardware algorithm with diagram. Multiply -5×-9 using Booth's multiplication algorithm. [5+5]
7. Draw the flowchart for division of floating point numbers. [4]
8. Draw the memory hierarchy. Explain direct cache mapping with its merits and demerits. [2+6]
9. Differentiate between Isolated I/O and Memory-mapped I/O. Describe DMA controller with suitable block diagram. [4+6]
10. Discuss about inter process synchronization with the suitable mechanism? [4]

Exam.	New Batch (2066 & Later Batch)		
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Year / Part	III / 1	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

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1. Differentiate between computer architecture and computer organization. Explain the computer functions with different cycles. [3+3]
2. Write a code for $Y = (A+B)*(C+D)+G/E^F$ using three address, two address one address and zero address instruction format. [8]
3. Mention the different types of addressing mode and compare each other. [10]
4. Explain the address sequencer with the help of a block diagram. Explain about microinstruction format in detail. [5+5]
5. Define pipeline and explain its types. Describe different pipeline hazards with example. [4+6]
6. Draw the flowchart for restoring division method. [4]
7. Explain Booth multiplication algorithm. Multiply -6×12 using Booth's algorithm. [4+6]
8. Draw the memory hierarchy. Explain Associative Cache Mapping with example. [2+6]
9. What are the different types of priority interrupt? Explain the communication between CPU and IOP with necessary block diagram. [4+6]
10. Explain about multiprocessor and multiprocessing in brief. [4]

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INSTITUTE OF ENGINEERING
Examination Control Division
2071 Chaitra

Exam.	Regular	
Level	BE	Full Marks
Programme	BEX, BCT	Pass Marks
Year / Part	III / I	Time
		80
		32
		3 hrs.

Subject: - Computer Organization Architecture (CT603)

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- ✓ Attempt All questions.
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1. What are the major differences between computer architecture and computer organization? What does the width of data bus and address bus represent in a system? Why is bus hierarchy required? [2+2+2]
2. Explain the general organization of register in CPU. Describe the operation of LD (load) instruction under various addressing modes with syntax. [6+4]
3. What are the different types of instructions? How can you perform $X = (A+B) \times (C+D)$ operation by using zero, one, two and three address instruction format. Assume A, B, C, D, X are memory address. [3+5]
4. What is address sequencing? Explain the selection of address for control memory with its block diagram. [3+7]
5. Explain the Arithmetic pipeline and instruction pipeline with example. [10]
6. Draw the flowchart for floating point Division. [4]
7. Design a booth multiplication algorithm hardware. Multiply 5 and -6 using booth multiplication algorithm. [4+4]
8. Explain cache organization. Explain the cache mapping techniques with example. [4+6]
9. Highlight the role of I/O interface in a computer system. Describe the drawbacks of programmed I/O and interrupt driven I/O and explain how DMA overcomes their drawbacks. [4+6]
10. How can multiprocessor be classified according to their memory organization? Explain. [4]

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Examination Control Division
 2071 Shawan

Exam.	ENAVBTE 2071 EXAMINATION		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

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1. What do you understand by Bus Interconnection? What are the driving factors behind the need to design for performance? [2+4]
2. Explain Instruction Format with its types? Illustrate the code to evaluate to evaluate: $Y = (A+B) * (C+D)$ using three address, two address, one address and zero address instruction formats. [2+6]
3. Describe the instruction cycle state diagram? Design a 2-Bit ALU that can perform addition, AND, OR operations. [3+3]
4. Explain the organization of a control memory. Discuss the microinstruction format with the help of a suitable example. [4+6]
5. Discuss about parallel processing? How parallel processing can be achieved in pipelining, explain it with time-space diagram for four segments pipeline having six tasks. [4+6]
6. Write down the detail algorithm of Booth Multiplication. Illustrate the multiplication of (9) and (-3) using 2's complement method. [5+5]
7. What is Memory Hierarchy and why it is formed in computer system? Explain the Direct cache memory mapping technique using organization diagram and appropriate example. [2+6]
8. What are the functions of I/O Module? What is the purpose of priority interrupt; explain priority interrupt types with key characteristics. [3+7]
9. Differentiate the following [4x3]
 - a. RISC and CISC
 - b. Restoring and Non-Restoring Division
 - c. Crossbar Switch and Multistage Switching Network

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1. What are the major differences between computer architecture and computer organization?
 What does the width of data bus and address bus represent in a system? Why is bus hierarchy required? [2+2+2]
2. Explain the general organization of register in CPU. Describe the operation of LD (load) instruction under various addressing modes with syntax. [6+4]
3. What are the different types of instructions? How can you perform $X = (A+B) \times (C+D)$ operation by using zero, one, two and three address instruction format. Assume A, B, C, D, X are memory address. [3+5]
4. What is address sequencing? Explain the selection of address for control memory with its block diagram. [3+7]
5. Explain the Arithmetic pipeline and instruction pipeline with example. [10]
6. Draw the flowchart for floating point Division. [4]
7. Design a booth multiplication algorithm hardware. Multiply 5 and -6 using booth multiplication algorithm. [4+4]
8. Explain cache organization. Explain the cache mapping techniques with example. [4+6]
9. Highlight the role of I/O interface in a computer system. Describe the drawbacks of programmed I/O and interrupt driven I/O and explain how DMA overcomes their drawbacks. [4+6]
10. How can multiprocessor be classified according to their memory organization? Explain. [4]

Exam.	New Back (2066 & Later Batch)		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. What is performance balance and why is it required? Explain different elements of bus design. [6]
2. Define the addressing mode and explain the different types of addressing modes with example. [10]
3. What are the stages of ALU design? Explain with the example of 2-bit ALU performing addition, subtraction, OR and XOR. [8]
4. What are the differences between hardwired implementation and micro-programmed implementation of control unit? Explain with steps involved when you are designing micro-program control unit. [4+6]
5. What is instruction hazard in pipeline? What is the four segment instruction pipeline? Explain with example. [2+8]
6. How division operation can be performed? Explain with its hardware implementation. [10]
7. Draw a flowchart of floating point subtraction. [4]
8. What are the major differences between different cache mapping techniques? Suppose main memory has 32 blocks and Cache memory has 8 blocks when 10 blocks of main memory are used, show how mapping is performed in direct mapping technique. [6+2]
9. Differentiate between programmed I/O, interrupt-driven I/O and direct memory access (DMA). [10]
10. Explain the interprocessor synchronization with example. [4]

Exam.	Regular		
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Organization and Architecture (CT603)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. Explain the interconnection of CPU with Memory and I/O devices along with different operations over them. [3+3]
2. Write down the $Y = A/B + (C \times D) + F(H/G)$ equation in three address, two address, one address and zero address instruction. [8]
3. Mention the different types of addressing modes. Compare each of them with algorithm as well as advantages and disadvantages. [10]
4. Differentiate between hardwired and micro-programmed control unit. How does a sequencing logic work in micro-programmed control unit to execute a micro-program? [4+6]
5. Explain the arithmetic pipeline and instruction pipeline with example. [10]
6. Explain the non-restoring division along with its algorithm, flowchart and example. [8]
7. Explain the Booth algorithm and multiply $Y = 8 \times 9$ using Booth algorithms. [6]
8. Mention the characteristics of computer memory. Differentiate between associative mappings and set associative mapping with example. [3+5]
9. How does DMA overcome the problems of programmed I/O and interrupt-driven I/O techniques? Explain. [5]
10. Why IOP is use in I/O organization? Explain. [5]
11. Explain the characteristics of multiprocessors. [4]

Exam.		Regular	
Level	BE	Full Marks	80
Programme	BEX, BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: -Computer Organization and Architecture (*CT 603*)

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. Explain the functional view and four types of operations used in computer. [6]
2. What are most common fields in an instruction? How can you perform $X=(E+F)*(G+H)$ operation by using zero, one, two and three address instruction format. Assume that E, F, G, H and X are memory addresses. [8]
3. Define addressing mode. Explain different types of addressing modes with example. [10]
4. Explain various fields in micro-instruction format with neat and clean block diagram. Describe how address of control memory is selected. [3+7]
5. What are the hazards in instruction pipelining? How can they be resolved? Explain. [10]
6. Explain Booth algorithm. Use the Booth algorithm to multiply 23(multiplicand) by -21(multiplier), where each number is represented using 6 bits. [8]
7. Explain floating point division algorithm. [6]
8. Explain cache read operation. What are the demerits of direct mapping technique used in cache design and describe in details any one of the mapping technique that solves these problems. [8]
9. Why input-output processor is needed in an input-output organization? Explain with block diagram. [10]
10. Define the multiprocessor and its characteristics. [4]

Exam.		Regular / Back	
Level	BE	Full Marks	80
Programme	BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Architecture and Design

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. Write down the following equation in three addresses, two addresses, one address and zero address instruction. If necessary, use temporary location T to store intermediate result. $Y = A + (B*C) + D$. [8]
2. What are the different types of addressing modes? Compare each of them with algorithm as well as advantages and disadvantages. [8]
3. Differentiate between restoring division and non restoring division with example. [8]
4. What are the three types of control signals? Explain the key steps of hardware implementation of control unit. [3+7]
5. What do you mean by mapping process? Differentiate between direct, associative and set associative mapping. [2+8]
6. Explain the key characteristics of computer memory systems. [8]
7. Explain the input/output interface with example. [6]
8. Compare between program I/O, interrupt driven I/O and Direct Memory Access (DMA). [8]
9. What are the steps to configure the plug and play device? Explain. [6]
10. What are the main goals of the plug and play BIOS specification? Explain. [8]

Exam.	Regular/Back		
Level	BE	Full Marks	80
Programme	BCT	Pass Marks	32
Year / Part	III / I	Time	3 hrs.

Subject: - Computer Architecture and Design

- ✓ Candidates are required to give their answers in their own words as far as practicable.
- ✓ Attempt All questions.
- ✓ The figures in the margin indicate Full Marks.
- ✓ Assume suitable data if necessary.

1. Write down the $Y=AB+ (F/G) +CD$ equation in three-address, two address, one address and zero address instruction. (8)
2. What are the three types of data manipulation instructions used in computer? Explain. (8)
3. Explain the Booth algorithm and its hardware implementation. Multiply the 6×7 using Booth algorithm. (4+4)
4. What do you mean by address sequencing? Explain the address sequencing capabilities required in a control memory. (3+5)
5. Why replacement algorithm is used when designing the cache? Explain with example. (8)
6. Why cache management is necessary in mapping process? Differentiate between direct mapping address structure and associative mapping address structure. (2+6)
7. What are the four types of I/O commands that an interface receive during the communication link between the processor and peripherals? Explain the I/O bus and interface modules. (4+4)
8. Mention the three possible configurations of DMA and compare them. (8)
9. Explain the PnP device configuration with example. (8)
10. Define the terms. (4×2=8)
 - a) ISA
 - b) PnP Post
