VLSI Design Automation
Lecture-1

By

Dr. Swagata Mandal

Assistant Professor, Electronics and Communication

Jalpaiguri Government Engineering College

Introduction to Reconfigurable System

- ***Reconfigurable system* (*RS*):** Any system whose sub-system configurations can be changed or modified after fabrication.

- ***Reconfigurable computing (RC):*** is commonly used to designate computers whose processing elements, memory units, and/or interconnections can change function and/or (spatial) configuration after fabrication, prior or during the run-time of a particular program or part of a program.

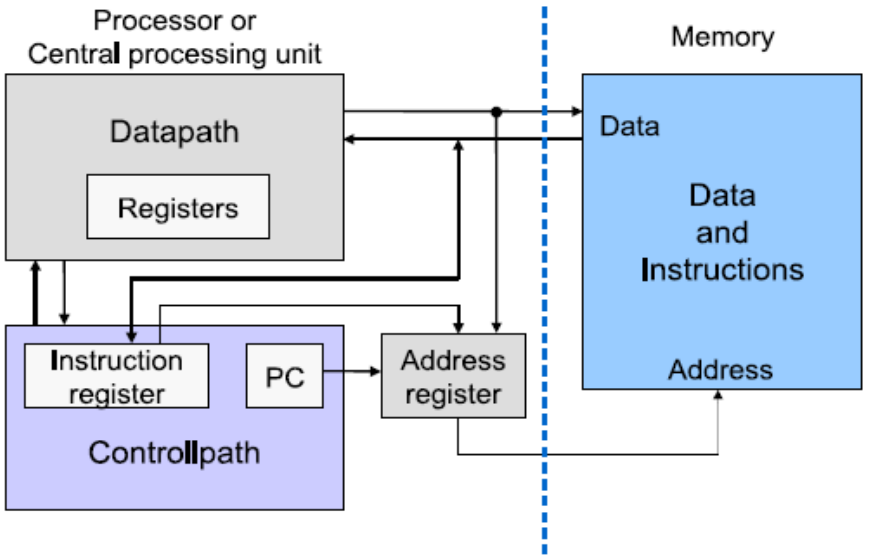
- RS use FPGAs, CPLD or other programmable hardware to accelerate algorithm execution by mapping compute-intensive calculations to the reconfigurable substrate.

General purpose computing

- In order to perform computation we need processing unit. There are various kind of processing unit as follows:

General Purpose Computing:

- A memory for storing program and data.
- A control unit (also called control path) featuring a program counter that holds the address of the next instruction to be executed.
- An arithmetic and logic unit (also called data path) in which instructions are executed.



Architecture of general purpose computer

Domain specific processor

- A domain specific processor is a processor tailored for a class of algorithms.
- The data path is tailored for an optimal execution of a common set of operations that mostly characterizes the algorithms in the given class.
- Memory access is reduced as much as possible.
- DSPs (Digital Signal Processor) belong to the most used domain specific processors.
- DSP is a specialized processor used to speed-up computation of repetitive, numerically intensive tasks in signal processing areas like telecommunication, multimedia, automobile, radar etc.
- The main feature of the DSPs is their ability to perform one or more multiply accumulate (MAC) operations in single cycle.

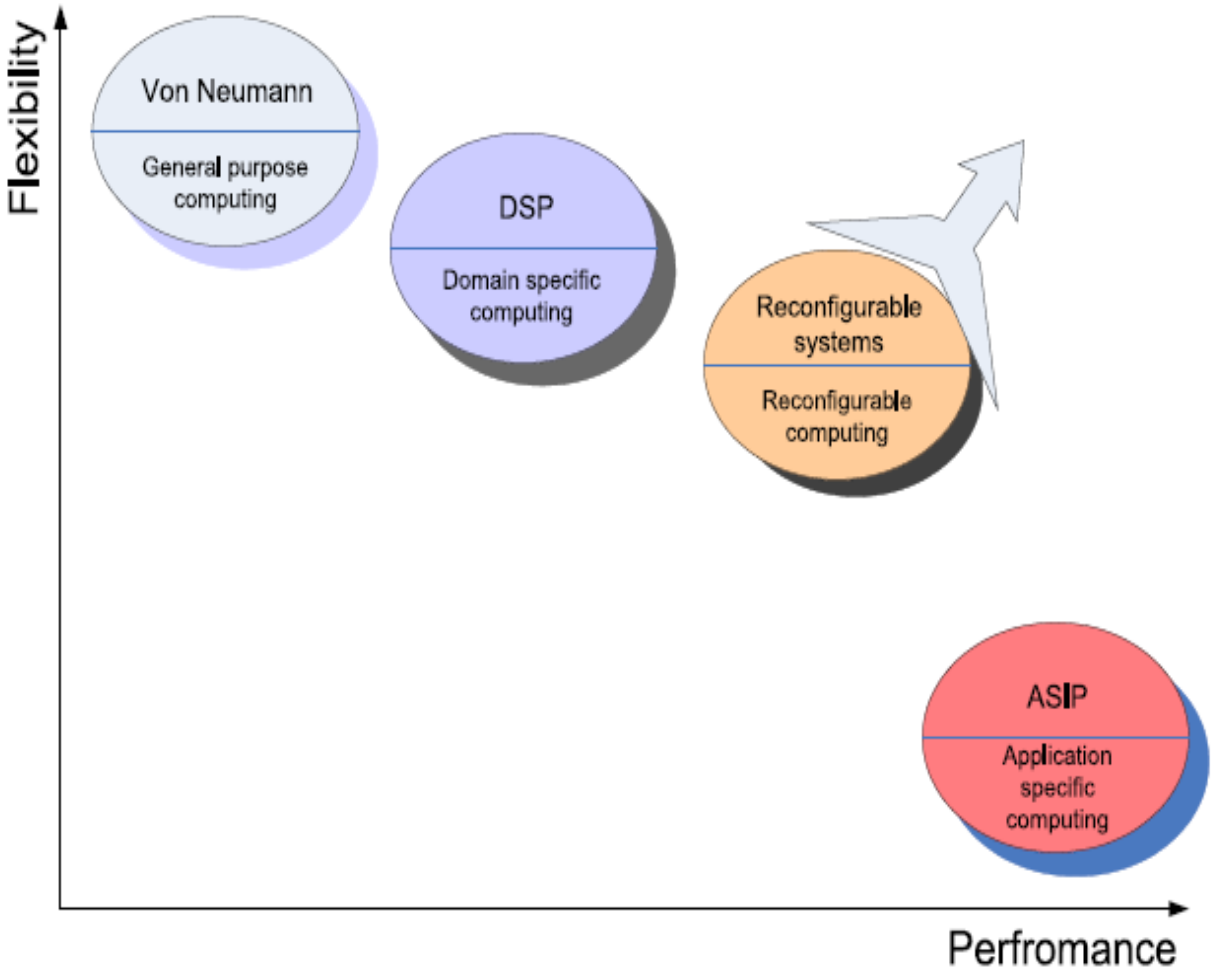
Application Specific Processors

- Although DSPs incorporate a degree of application specific features like MAC and data width optimization, they still incorporate the Von Neumann approach and, therefore, remain sequential machines. Hence their performance is also limited.
- If a processor has to be used for only one application, which is known and fixed in advance, then the processing unit could be designed and optimized for that particular application.
- A processor designed for only one application is called an *Application Specific Processor (**ASIP**)*.
- ASIPs are usually implemented as a single chips called *Application Specific Integrated Circuit (**ASIC**)*
- ASIPs use a spatial approach to implement only one application
- It can not be used for the tasks other than those for which it has been originally designed.

Performance of the Processor

- There are two points based on which processors can be classified: Flexibility and performance

- We want flexibility of the GPP and the performance of the ASIP in the same device.



Flexibility vs performance of processor classes

- Such devices are known as reconfigurable devices or reconfigurable processing unit

Application of RC

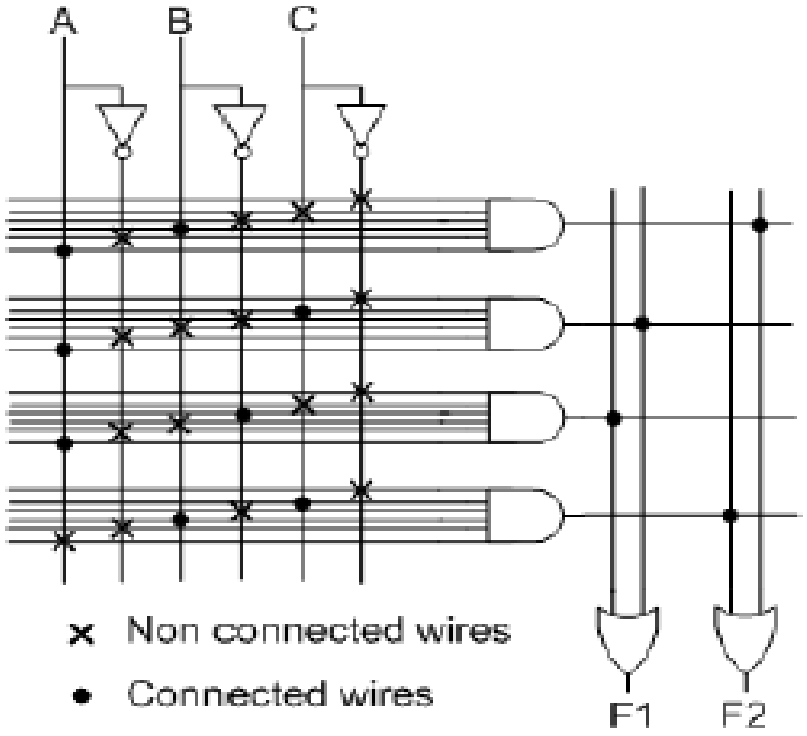
- **Rapid Prototyping:** Low NRE cost, easy time to market
- **In System Customization:** Various functionalities can be easily added, upgraded
- **Multi modal Computation:** Multiple operation can be performed into spatiotemporal fashion.
- **Adaptive Computing Systems:** Reconfiguration can provide a good way for the realization of adaptive systems, because it allows system to quickly reacts to changes by adopting the optimal behaviour for a given run-time scenario.

History of RC

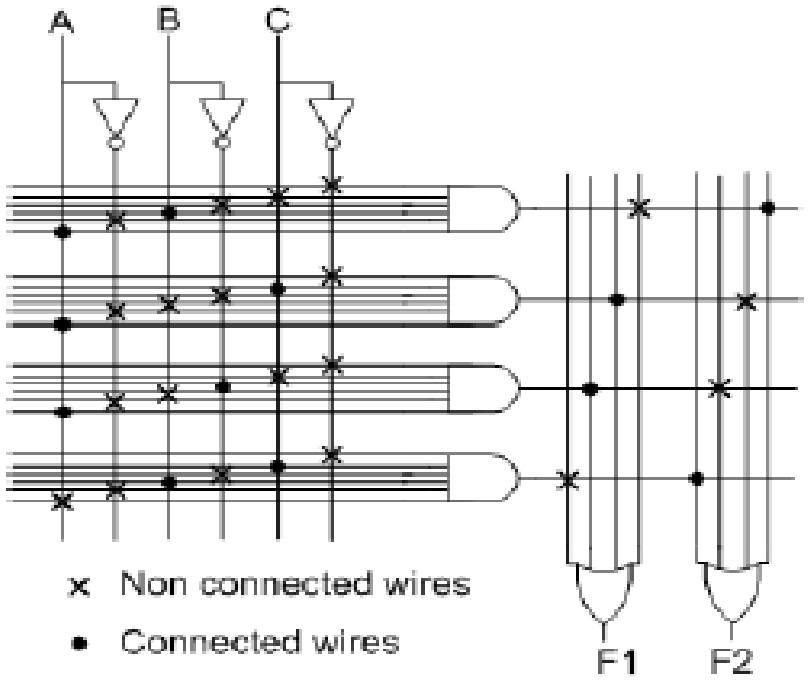
- **The Estrin Fix-plus machine(1959)**
- **The Rammig Machine(1977)**
- **Hartenstein's *Xputer***
- **The PAM Machine:** Programmable Active Memory Machine
- **The *SPLASH II***
- **The *PRISM* Paradigm :** Processor Reconfiguration through Instruction Set Metamorphosis
- **The *Garp* Approach**
- ***DISC:*** Dynamic Instruction Set Computer
- ***DPGA***: Dynamically *Programmable Gate Array*
- ***FPGA****:* Field programmable Gate array

Programmable Logic Devices

- Programmable logic arrays (PLA) and programmable array logic (PAL) consists of a plane of AND-gates connected to a plane of OR-gates
- The inputs signals as well as their negations are connected to the inputs of the AND-Gates in the AND-plane.



(a) PAL: The OR-connections are fixed



(b) PLA: Programmable OR-connections

Programmable Logic Devices(cont'd)

- The outputs of the AND-gates are use as input for the OR gate in the OR-plane whose outputs correspond to those of the PAL/PLA.
- In PLA both AND and OR planes can be programmed by the user.
- In PAL only AND field is programmable but OR field is fixed.
- The main limitation of PLAs and PALs is their low capacity, which is due to the nature of the AND-OR-plane.
- The size of the plane grows too quickly as the number of inputs increases.
- Due to their low complexities, PALs and PLAs belong to the class of devices called *simple programmable logic devices* (SPLD).

Complex Programmable Logic Device

- A CPLD consist of a set of *macro cells*, *Input/Output blocks* and an *interconnection network*.

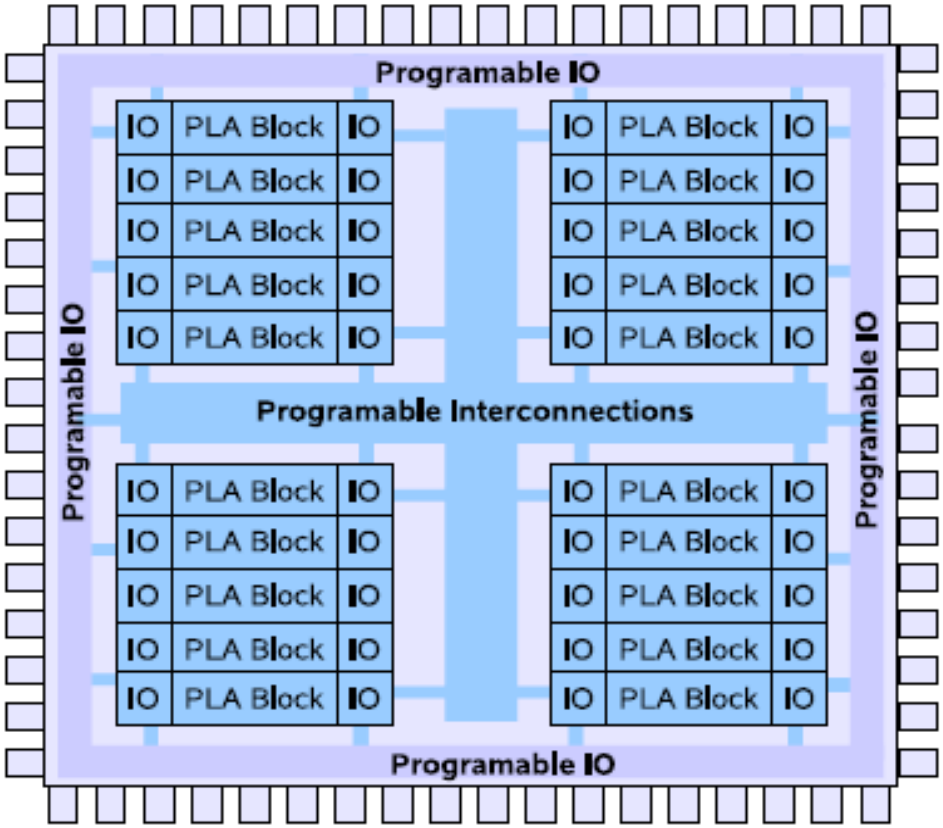
- The connection between the Input/Output blocks and the macro cells and those between macro cells and macro cells can be made through the programmable interconnection network

- A macro cell typically contains several PLAs and flip flops.

- Despite their relative large capacity (few hundreds thousands of logic gates), compared to those of PLAs, CPLDs are still too small for the use in reconfigurable computing devices.

CPLD(Cont'd)

- CPLD are usually used as glue logic, or to implement small functions
- Due to their non volatility, CPLDs are used in many systems for configuration of the main reconfigurable device at power on reset.



Internal Architecture of CPLD

Field Programmable Gate Array

- Introduced in 1985 by the company Xilinx.

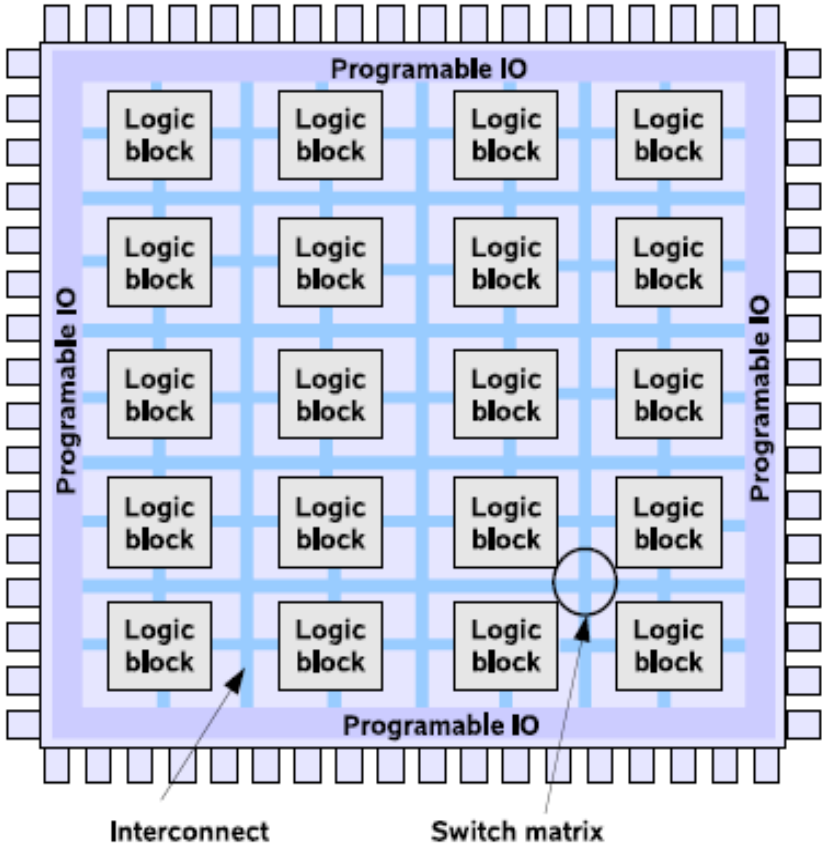
- Field Programmable Gate Array (FPGA) is a programmable device consisting, like the CPLDs, of three main parts: a set of programmable logic cells also called *logic blocks* or *configurable logic blocks*, a *programmable interconnection network* and a set of *input and output cells* around the device.

- A function to be implemented in FPGA is partitioned in modules, each of which can be implemented in a logic block.

- The logic blocks are then connected together using the programmable interconnection

FPGA(Cont'd)

- All three basic components of an FPGA (logic block, interconnection and input output) can be programmed by the user in the field.
- FPGAs can be programmed once or several times depending on the technology used.



Internal Architecture of FPGA

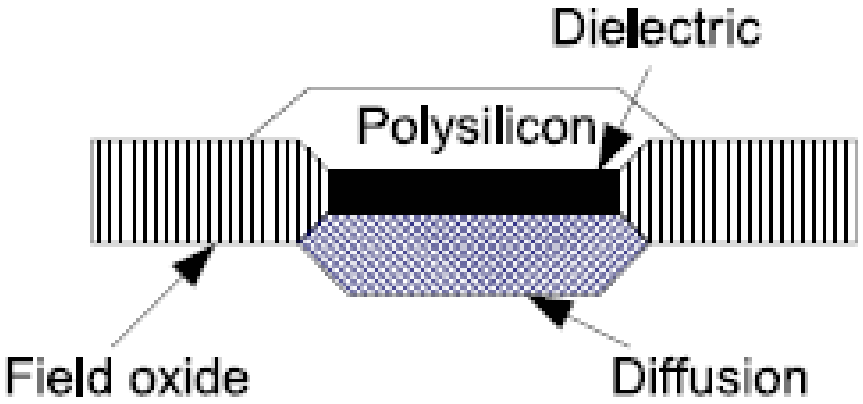
Technology of FPGA

- The technology defines how the different blocks (logic blocks, interconnect, input/output) are physically realized.
- Basically, two major technologies exist: Anti-fuse and memory-based.
- Anti-fuse based technology is limited to interconnection only
- On the other hand the memory-based paradigm is used for the computation as well as the interconnection.
- In the memory-based category, we can list the SRAM, the EEPROM and, the Flash based FPGAs

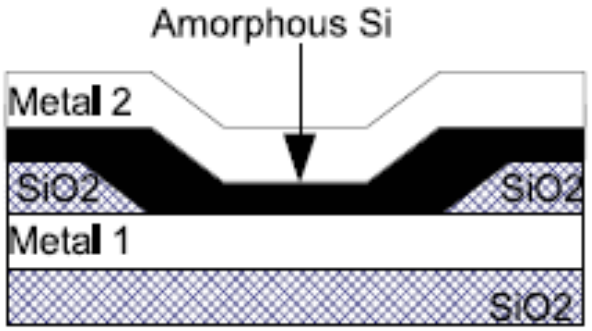
Anti-fuse Technology

- An antifuse based FPGAs use special antifuses included at each connection customization point.
- The two-terminal elements are connected to the upper and lower layer of the antifuse, in the middle of which a dielectric is placed.
- In its initial state, the high resistance of the dielectric does not allow any current to flow between the two layers.
- Applying a high voltage causes large power dissipation in a small area, which melts the dielectric.
- This operation drastically reduces the resistance and a link can be built, which permanently connects the two layers.
- The two types of antifuses actually commercialized are: *PLICE(Programmable Low-Impedance Circuit Element)* and *Metal Antifuse* also called *ViaLink*

Anti-fuse Technology(Cont'd)



Actel PLICE Antifuse



Q-Logic Vialink antifuse

- PLICE is manufactured by Actel
- It consists of an Oxygen-Nitrogen-Oxygen (ONO) dielectric layer sandwiched between a polysilicon and an n+ diffusion layer that serves as conductor.

- The ViaLink antifuse manufactured by Q-Logic.

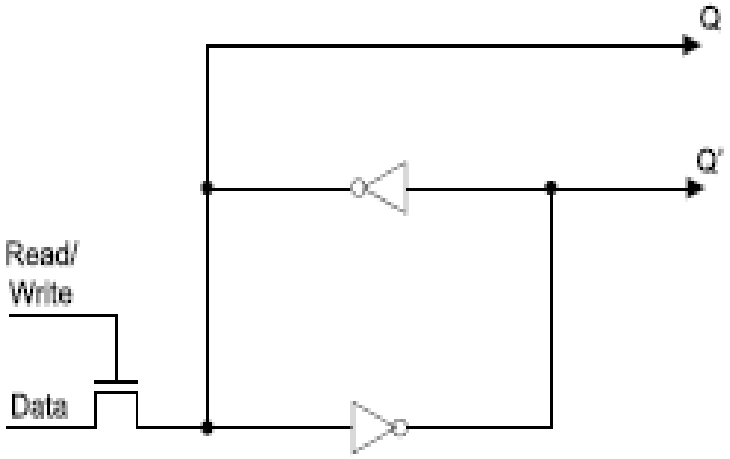
- It is composed of a sandwich of very high resistance layer of programmable amorphous silicon between two metal layers.

Anti-fuse Technology(Cont'd)

- When a programming voltage is applied, a metal-to-metal link is formed by permanently converting the silicon to a low resistance state.
- The main advantage of the antifuse chips is their small area and their significantly lower resistance and parasitic capacitance compared to transistors.
- This help to reduce the RC delays in the routing.
- However, anti-fuse based FPGAs are not suitable for devices which must be frequently reprogrammed, as it is the case in reconfigurable computing.
- Antifuse FPGAs are normally programmed once by the user and will not change anymore.
- For this reason, they are also known as *one-time programmable* FPGAs.

SRAM Technology

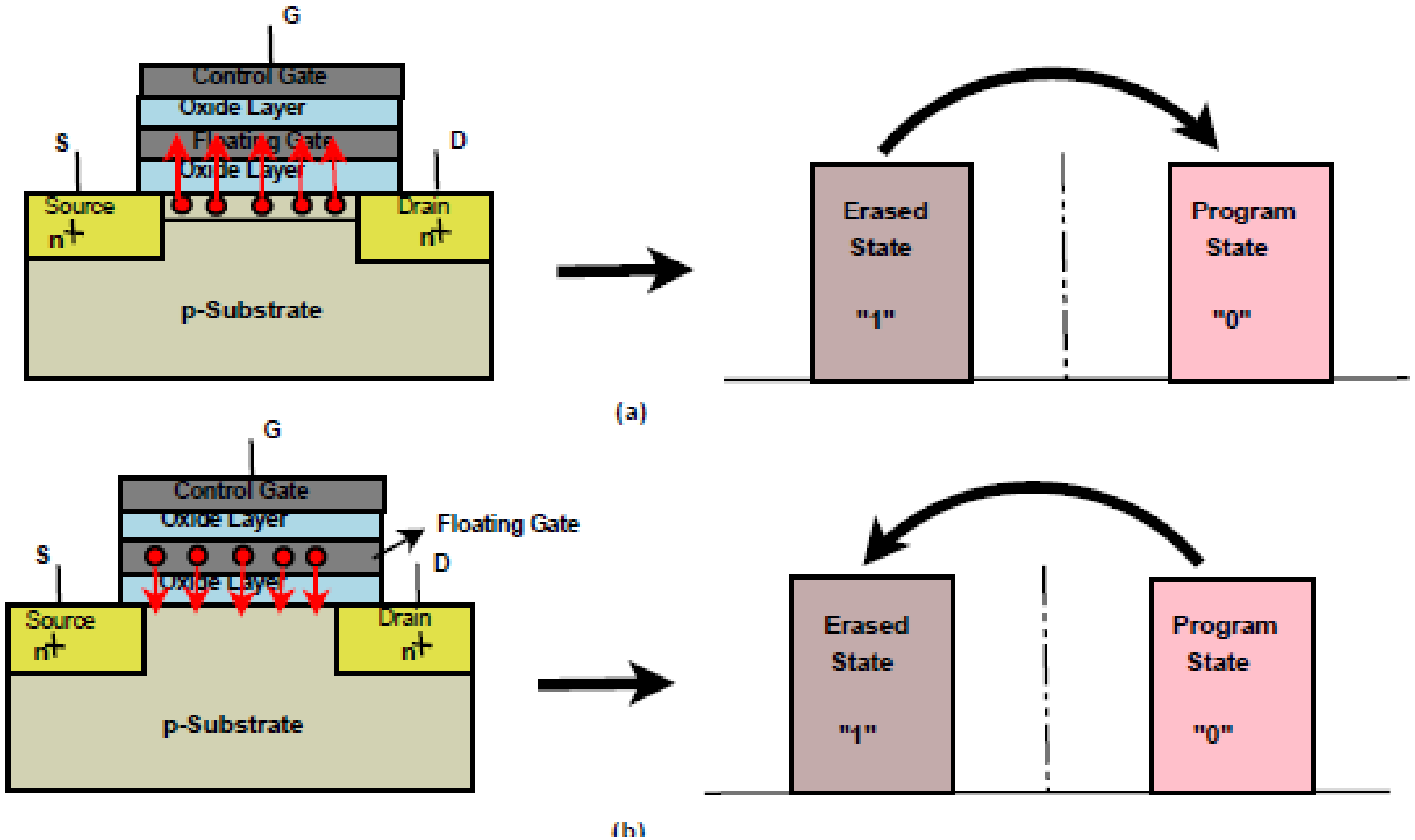
- SRAM-based FPGAs are the most widely used.
- Unlike the antifuse that is used mostly used to configure the connection, a Static RAM (SRAM) is use to configure the logic blocks and the connection as well.
- In an SRAM-based FPGA, the states of the logic blocks, i.e. their functionality bits as well as that of the interconnections are controlled by the output of SRAM Cells



Xilinx SRAM cell Architecture

EPROM Technology

- Erasable Programmable Read Only Memory (EPROM) devices are based on a floating gate technology.
- In floating gate MOSFET two gates are used: control and floating gate



Floating gate technology

- Floating gate is isolated from any electrical connection by oxide layer in both sides and hence any charge within it remains trapped and trapped charge can be altered by either using hot carrier injection mechanism or tunnelling method.

- If no voltage is applied to floating gate, the device operates like normal MOSFET where a positive voltage in control gate above threshold creates channel and conduction can be started between source and drain by proper voltage at source and drain.

- When a high positive voltage is applied to floating gate, electrons from the source, drain and channel tunnel through the oxide and get trapped within the floating gate.

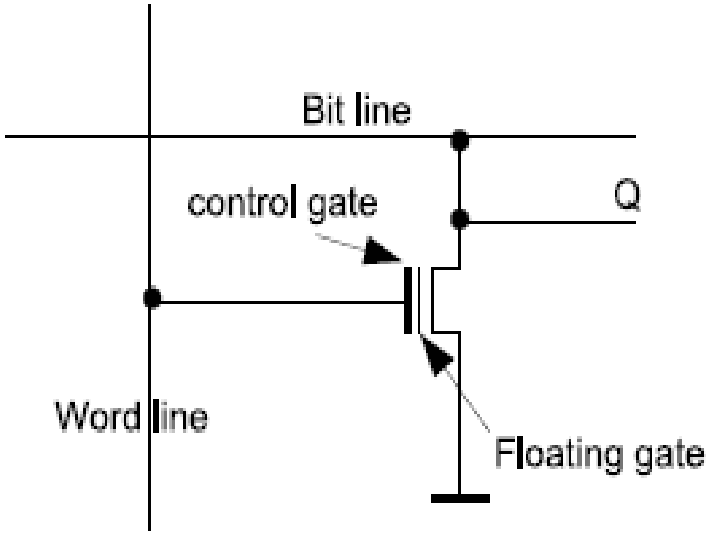
- This state is called programmed state and designated by "0"

Floating gate technology(Cont'd)

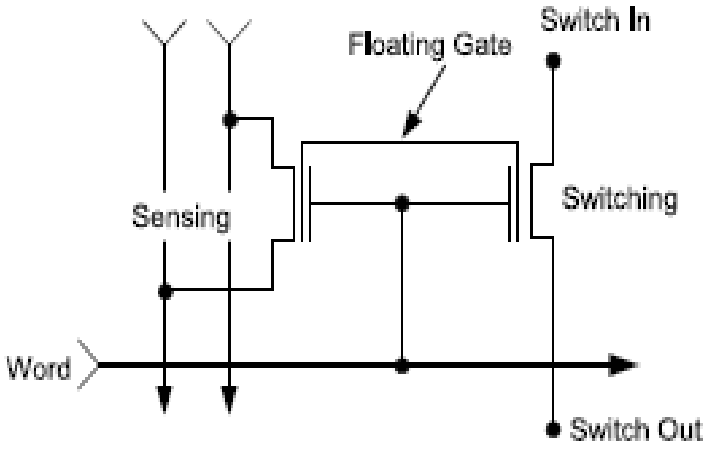
- This in turn increases the threshold voltage to form the channel and on the device.
- When a negative high voltage is applied to push back the trapped electron into the substrate then this operation is known as erase operation.
- The state after the erase operation is known as erased state and designated as "1".
- When threshold voltage of a MOSFET in a NAND cell has only two state it can store only one bit per cell and known as SLC
- On the other hand if threshold voltage has more than two states like four states (two bits per cell) or eight states (three bits per cell) then it is known as MLC.

EEPROM Technology

- In general UV light or electrical pulse is used to provide high voltage to the floating gate



(a) EPROM Cell



(b) Actel Flash-EEPROM

- In EEPROM and Flash-EPROM the erase operation is accomplished electrically rather than by exposure to the UV light

EEPROM Technology(Cont'd)

- Erasing operation using electrical pulse is faster than UV lamp and need not be removed from the system.
- In EEPROM-based devices, two or more transistors are typically used in a ROM cell: one access and one programmed transistor.
- The programmed transistor performs the same function as the floating gate in an EPROM, with both charge and discharge being done electrically.
- In the Flash-EEPROMs two transistors share the floating gate, which stores the programming information.
- The sensing transistor is only used for writing and verification of the floating gate voltage while the other is used as switch.
- This can be used to connect or disconnect routing nets to or from the configured logic.

Thank You