5T-OTA Design

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Part 1: OTA Design

1. Desired Specs

Technology	$180\ nm\ CMOS$
Supply Voltage	$1.8\ V$
Load	$5\ pF$
Open Loop DC Voltage Gain	$\geq 34\ dB$
CMRR @DC	$\geq 74\ dB$
Phase Margin	$\geq 70°$
CM input range - low	$\leq 1\ V$
CM input range - high	$\geq 1.5\ V$
GBW	$\geq 10\ MHz$

Table 1: Desired Specs

At first, we need to identify the topology.

Since the CMIR is near to VDD, therefore the topology we will use is the NMOS input pair 5T-OTA.

2. OTA schematic

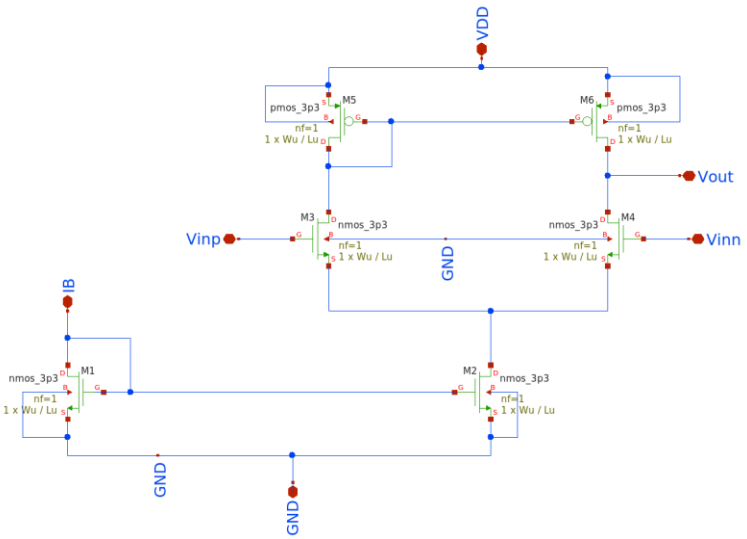

Figure 1: schematic

3. OTA Devices Sizing

$Device$	$M_2\ (tail\ CM)$	$M_{3,4}\ (input\ pair)$	$M_{5,6}\ (load\ CM)$
W	$11.69\ \mu m$	$25.64\ \mu m$	$12.12\ \mu m$
L	$730\ nm$	$450\ nm$	$350\ nm$
g_m	$350\ \mu S$	$315\ \mu S$	$192.5\ \mu S$
I_D	$35\ \mu A$	$17.5\ \mu A$	$17.5\ \mu A$
g_m/I_D	10	18	11
V_{DSsat}	$173.1\ mV$	$85.7\ mV$	$149.4\ mV$
V_{ov}	$144.8\ mV$	$-3.25\ mV$	$132.4\ mV$
V^*	$200\ mV$	$111\ mV$	$181.8\ mV$

Table 2: OTA Devices Sizing

Part 2: Open-loop OTA simulation

1. OP simulation

1) Schematic of the OTA showing sizing of the transistors

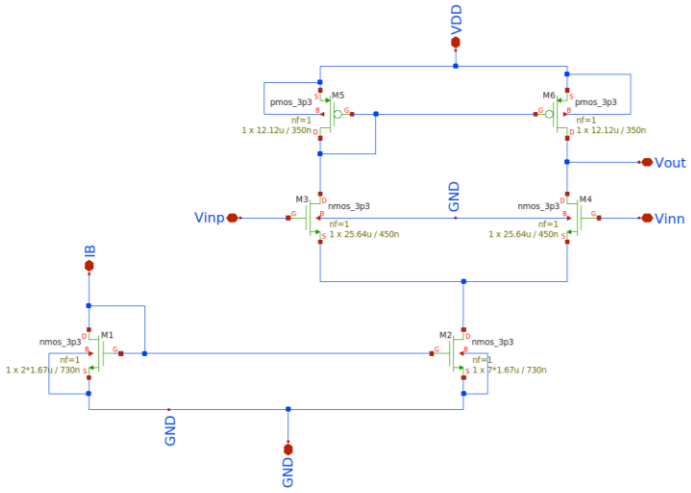

Figure 2: Final design schematic

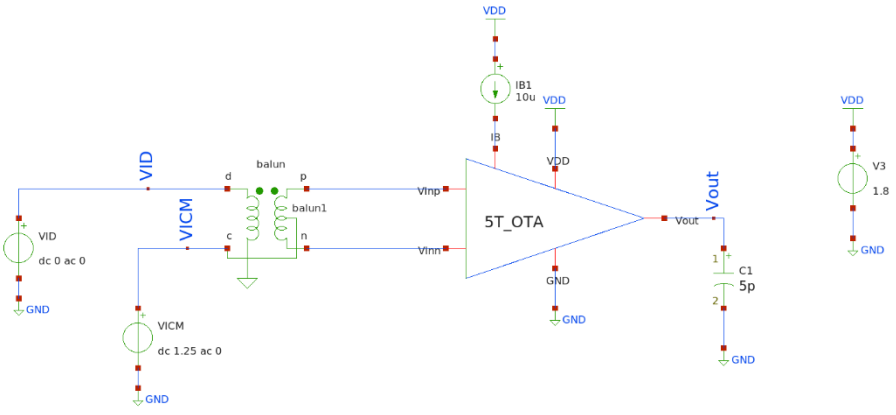

Figure 3: Open-loop testbench

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm1.m0	m.x1.m.xm2.m0	m.x1.m.xm6.m0
model	x1:nmos_3p3.9	x1:nmos_3p3.13	x1:pmos_3p3.12
id	1e-05	3.48193e-05	1.74097e-05
vgs	0.839402	0.839402	0.89634
vth	0.695315	0.698117	0.768305
vds	0.839398	0.424029	0.896338
vdsat	0.172191	0.171438	0.158334
gm	9.94844e-05	0.000348897	0.000194625
gds	4.36439e-07	2.4772e-06	2.22279e-06
gmbs	3.71677e-05	0.000130336	7.55257e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm5.m0	m.x1.m.xm4.m0	m.x1.m.xm3.m0
model	x1:pmos_3p3.12	x1:nmos_3p3.12	x1:nmos_3p3.12
id	1.74097e-05	1.74097e-05	1.74097e-05
vgs	0.89634	0.825963	0.825963
vth	0.768305	0.832767	0.832767
vds	0.896338	0.47962	0.47962
vdsat	0.158334	0.0860522	0.0860522
gm	0.000194625	0.000310268	0.000310268
gds	2.22279e-06	3.00789e-06	3.00789e-06
gmbs	7.55257e-05	8.41838e-05	8.41838e-05

Figure 4: DC OP parameters

The current in M2 is less than desired and that affects gm so the GBW is affected too so, we will increase the mirror ratio into 3.65 (change M1 size to 3.2 μm width instead of 3.34 μm and keep M2 as it is). So the current consumption is 36.4 μA now.

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm1.m0	m.x1.m.xm2.m0	m.x1.m.xm6.m0
model	x1:nmos_3p3.9	x1:nmos_3p3.13	x1:pmos_3p3.12
id	1e-05	3.63829e-05	1.81914e-05
vgs	0.84384	0.84384	0.900259
vth	0.695132	0.698117	0.768285
vds	0.843836	0.422066	0.900257
vdsat	0.175467	0.174656	0.161303
gm	9.76347e-05	0.000357886	0.000199861
gds	4.3265e-07	2.61195e-06	2.29916e-06
gmbs	3.64741e-05	0.000133689	7.75722e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm5.m0	m.x1.m.xm4.m0	m.x1.m.xm3.m0
model	x1:pmos_3p3.12	x1:nmos_3p3.12	x1:nmos_3p3.12
id	1.81914e-05	1.81914e-05	1.81914e-05
vgs	0.900259	0.827925	0.827925
vth	0.768285	0.832248	0.832248
vds	0.900257	0.477664	0.477664
vdsat	0.161303	0.0871732	0.0871732
gm	0.000199861	0.000321304	0.000321304
gds	2.29916e-06	3.12547e-06	3.12547e-06
gmbs	7.75722e-05	8.7256e-05	8.7256e-05

Figure 5: final DC OP parameters values

- The current and gm in the input pair exactly equal because no mismatch nor diff input.
- $V_{outdc} = V_{DD} - V_{DS6} = V_{DD} - V_{GS5} = 899.74\ mV$ as it follows the mirror node because the current in both branches are equal as a result of the above point.

2. Diff small signal ccs

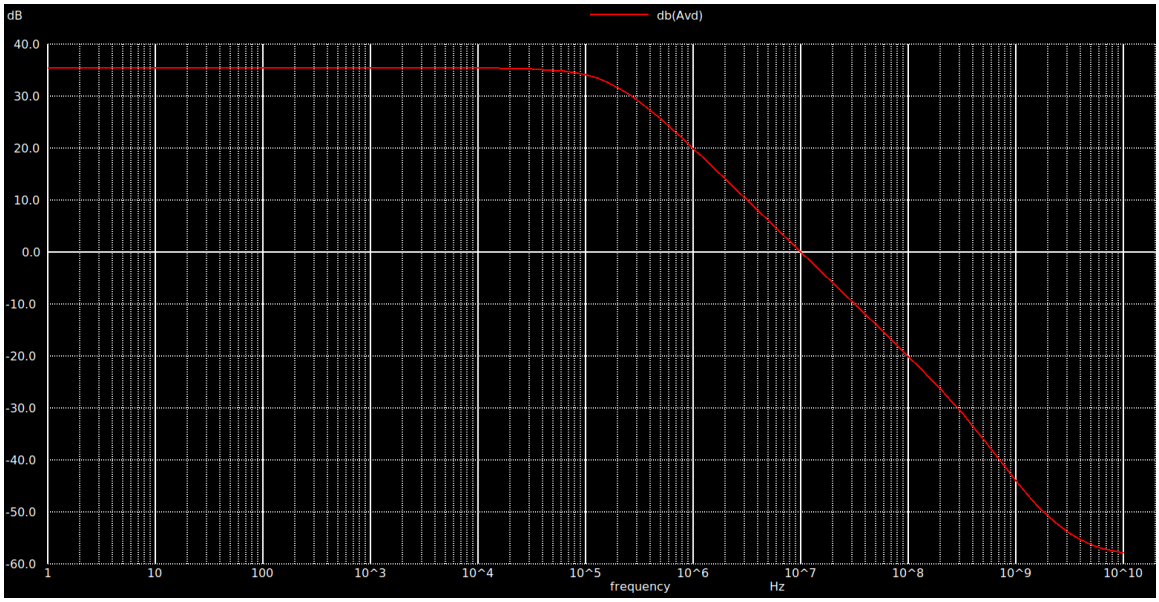

Figure 6: diff gain bode plot (magnitude)

```
peak = 5.889266e+01
f2 = 1.705541e+05
gbw = 1.004438e+07
```

Figure 7: diff small signal results

$$DC\ diff\ gain = g_{m3,4}(r_{o4} \parallel r_{o6}), BW = \frac{1}{2\pi(r_{o4} \parallel r_{o6})C_L}, GBW = \frac{g_{m3,4}}{2\pi C_L}$$

Spec	*Simulation*	*Hand analysis*
$DC\ diff\ gain$	35.4 dB	35.45 dB
BW	170.6 KHz	172.7 KHz
GBW	10 MHz	10.2 MHz

Table 3: simulation vs hand analysis

3. CM small signal ccs

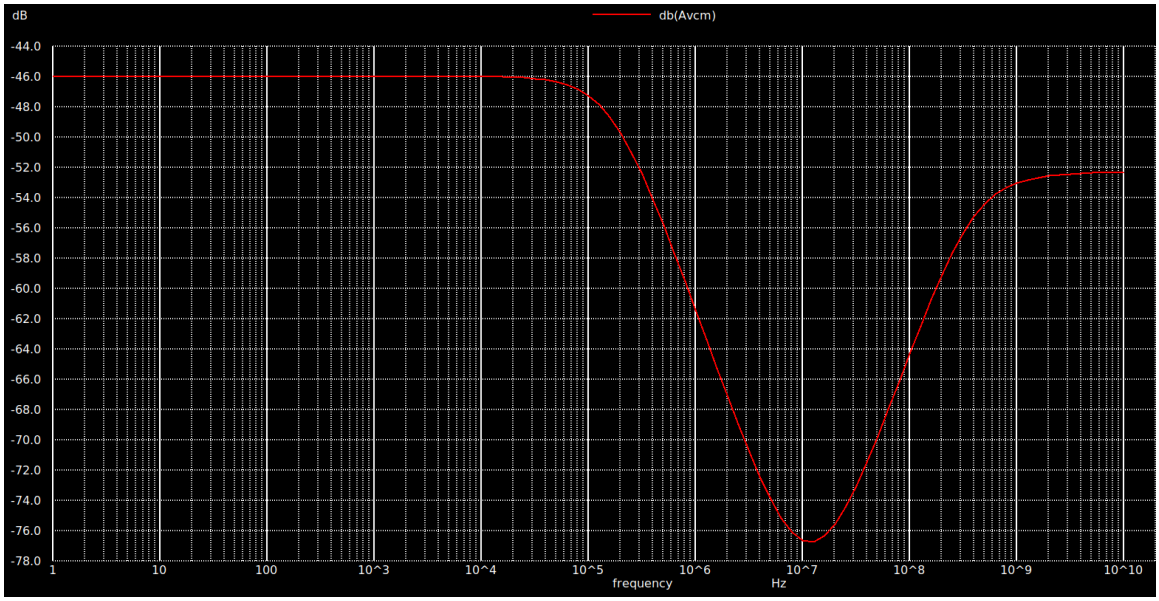

Figure 25: CM gain bode plot (magnitude)

peak = 5.025538e-03

Figure 26: CM gain

$$DC\ CM\ gain \approx \frac{-g_{m1,2}}{2\left(g_{m1,2}+g_{mb1,2}\right)g_{m5,6}r_{o2}}$$

Spec	*Simulation*	*Hand analysis*
DC CM gain	$-46\ dB$	$-45.8\ dB$

Table 4: simulation vs hand analysis

4. CMRR

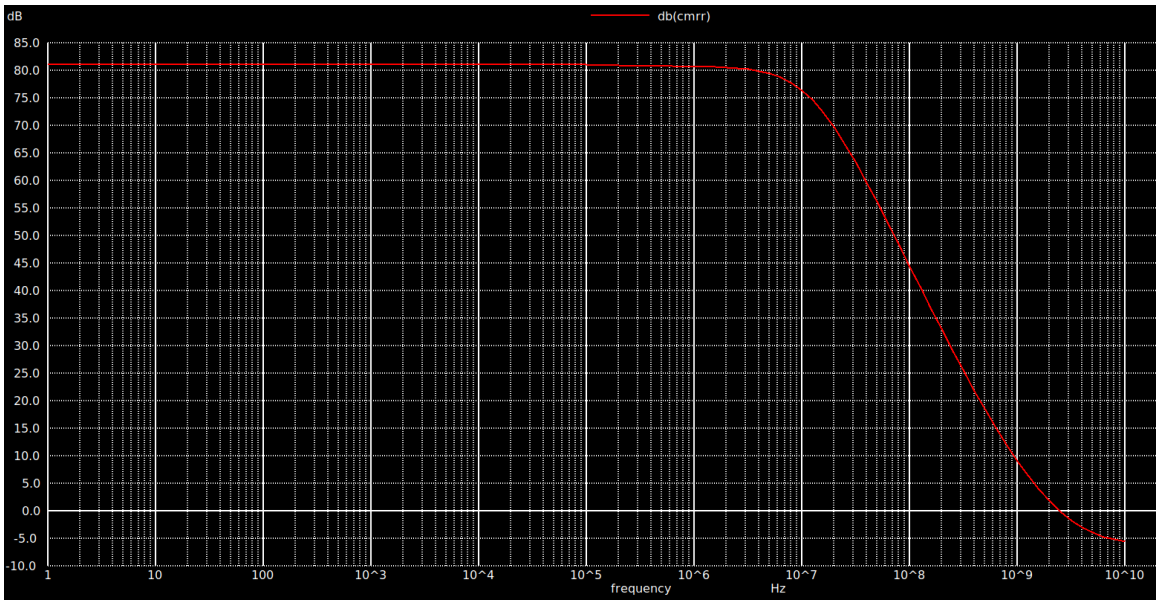

Figure 27: CMRR bode plot (magnitude)

Spec	*Simulation*	*Hand analysis*
CMRR	81.1 dB	$A_{vd} - A_{vCM} = 81.25\ dB$

Table 5: simulation vs hand analysis

5. Diff large signal ccs

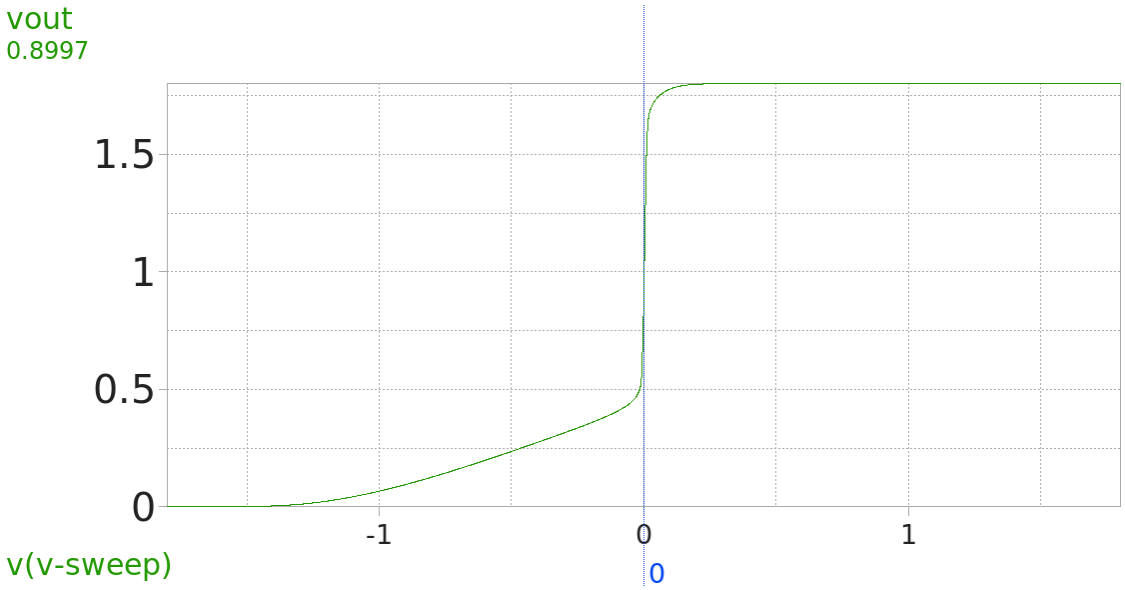

Figure 8: Vout vs VID

$V_{outdc} = 899.7\ mV$ as it follows the mirror node $V_M = V_{DD} - V_{GS5} = 899.74\ mV$ because the current in both branches are equal as there is no mismatch nor diff input.

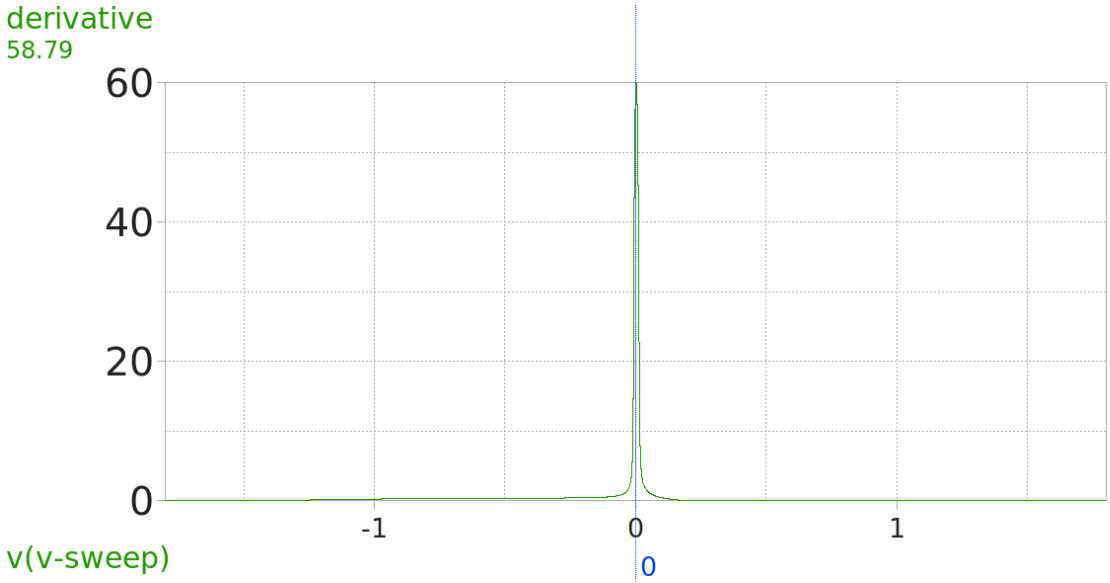

Figure 9: derivative(Vout) vs VID

$A_{vd} = 58.9\ from\ simulation\ and\ the\ peak = 58.8$ as they are two faces for the same coin.

6) CM large signal ccs (GBW vs VICM)

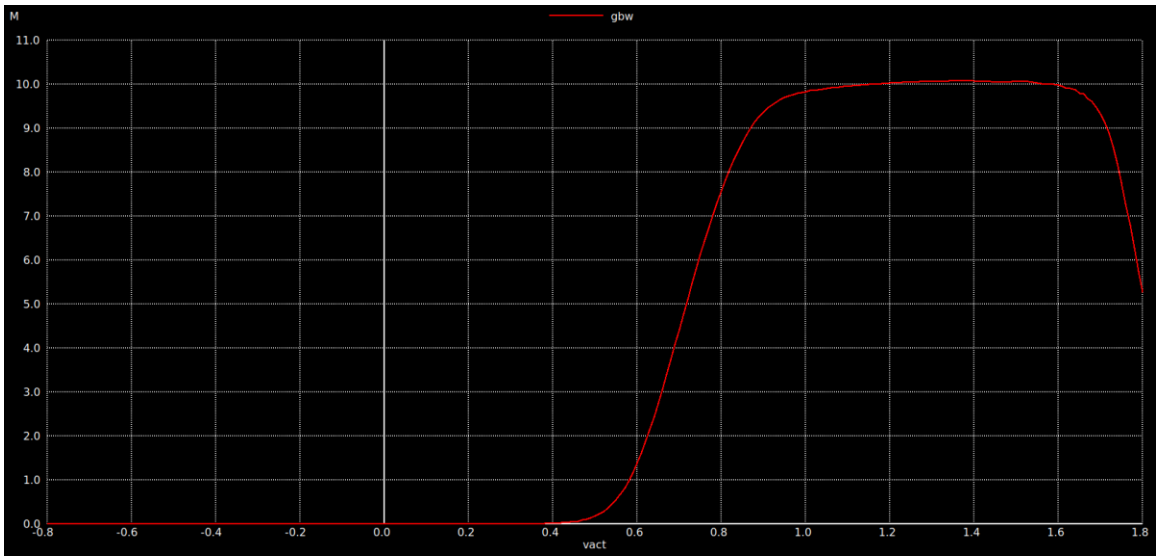

Figure 10: GBW vs VICM

$CMIR_{high} = V_{DD} - V_{GS5,6} - V_{DSsat3,4} + V_{GS3,4}$
$CMIR_{low} = V_{GS3,4} + V_{DSsat2}$

Spec	*simulation*	*analytic*
GBW	10.27 MHz	10.2 MHz
$CMIR_{low}$	870 mV	1 V
$CMIR_{high}$	1.71 V	1.64 V

Table 5: CMIR

The noticeable variance in the $CMIR$ is due to:

- The 90 % change in DC differential gain is not an accurate value to detect the edge of saturation for the Diff Amp devices. The conclusion from the simulation results is that the DC differential gain is higher than 90 % so taking 90 % as our threshold makes the range wider in the simulation results.

Part 3: Closed-Loop OTA Simulation

1. OP simulation

device	m.x1.m.xm1.m0	m.x1.m.xm6.m0	m.x1.m.xm5.m0
model	x1:nmos_3p3.8	x1:pmos_3p3.12	x1:pmos_3p3.12
gm	0.000117183	0.000294736	0.000297304
gmbs	3.71209e-05	0.000120467	0.000121469
gds	1.41041e-06	2.34134e-06	2.26431e-06
vds	0.788241	0.751349	0.836933
vdsat	0.141941	0.108171	0.10834
vgs	0.788245	0.836934	0.836934
vth	0.692487	0.778292	0.778018
id	1e-05	1.94457e-05	1.96427e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm2.m0	m.x1.m.xm4.m0	m.x1.m.xm3.m0
model	x1:nmos_3p3.12	x1:nmos_3p3.12	x1:nmos_3p3.12
gm	0.000460454	0.000310609	0.000312906
gmbs	0.000145956	9.16614e-05	9.2348e-05
gds	1.47446e-05	2.56842e-06	2.67032e-06
vds	0.246287	0.802351	0.716767
vdsat	0.138686	0.0984722	0.0990691
vgs	0.788246	0.802353	0.803703
vth	0.697966	0.782482	0.782696
id	3.90884e-05	1.94457e-05	1.96427e-05

```
gm_mismatch = 4.887051e-06
id_mismatch = 3.463498e-07
```

Figure 11: gm and ID mismatch

The change in g_m *and* I_D $(about\ 1.5\ to\ 1.9\ \%)$ is due to the difference between V_{outDC} and the mirror node level which leads to mismatch in V_{DS3}, V_{DS4} *and* V_{DS5}, V_{DS6}.

2. STB analysis

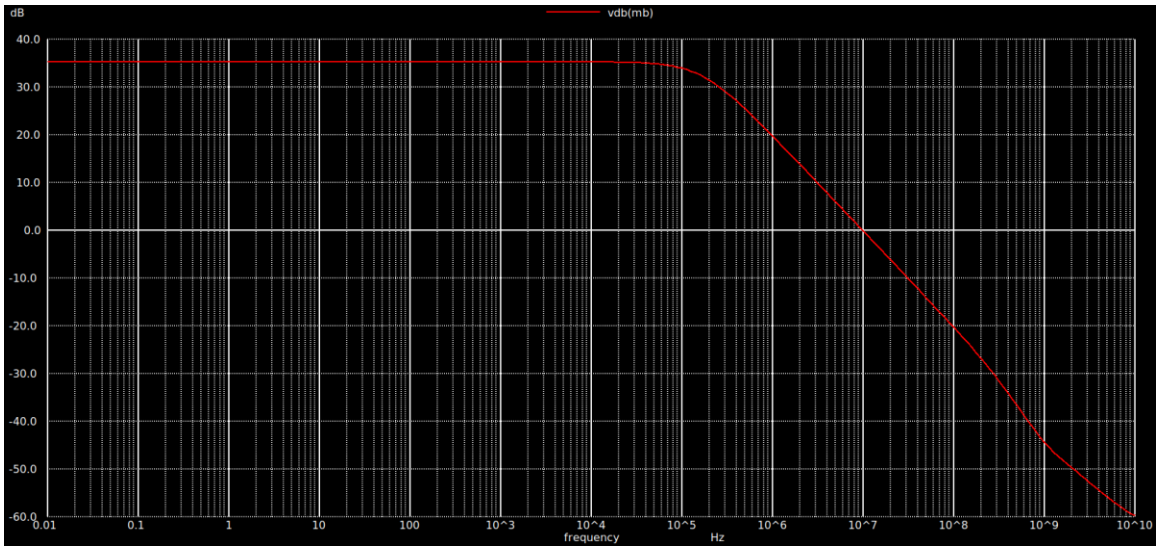

Figure 12: loop gain bode plot (magnitude)

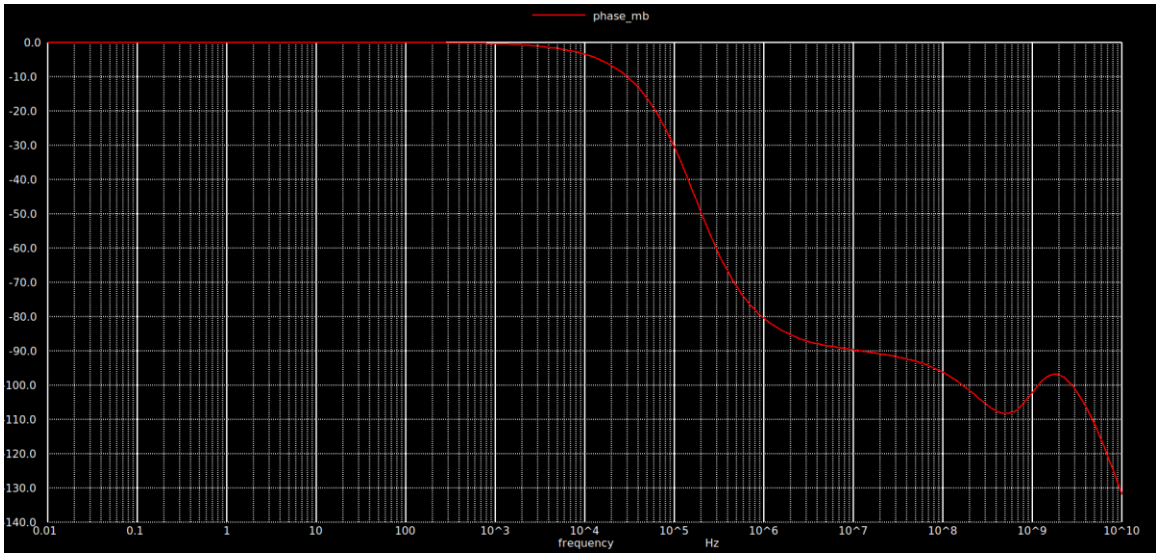

Figure 13: loop gain bode plot (phase)

```
peak                =  5.800454e+01 at=  2.238721e+00

Error: measure  f1  when(WHEN) : out of interval
 meas ac f1 when vmag(mb)=4.101540e+01 rise=1 failed!

bw                  =  1.690970e+05
pm_deg              =  -8.964793e+01
dominant_pole_f     =  9.806458e+06
loop_gain           =  3.526924e+01
gbw = 9.808394e+06
```

Figure 14: STB analysis results

Spec	*open loop simulation*	*closed loop simulation*
DC gain	35.4 dB	35.27 dB
BW	170.6 KHz	169 KHz
GBW	10 MHz	9.8 MHz

Figure 15: open loop vs closed loop simulation

The specs variance between open and closed loop simulations is because V_{outDC} - which controls the values of $V_{DS4,6}$ - is 1.25 V not 960 mV as the mirror node so the OP parameters are changed.

$PM = 89.6°$

device	m.x1.m.xm1.m0	m.x1.m.xm2.m0	m.x1.m.xm6.m0
model	x1:nmos_3p3.9	x1:nmos_3p3.13	x1:pmos_3p3.12
gm	9.76347e-05	0.000357856	0.00019467
gmbs	3.64741e-05	0.000133678	7.57603e-05
gds	4.3265e-07	2.62054e-06	2.7977e-06
vds	0.843836	0.420997	0.555788
vdsat	0.175467	0.174656	0.161603
vgs	0.84384	0.84384	0.902408
vth	0.695132	0.698117	0.77004
id	1e-05	3.63801e-05	1.7751e-05

BSIM4v5: Berkeley Short Channel IGFET Model-4

device	m.x1.m.xm5.m0	m.x1.m.xm4.m0	m.x1.m.xm3.m0
model	x1:pmos_3p3.12	x1:nmos_3p3.12	x1:nmos_3p3.12
gm	0.000202731	0.00031534	0.000327416
gmbs	7.86943e-05	8.56532e-05	8.89592e-05
gds	2.34151e-06	2.59929e-06	3.19107e-06
vds	0.902406	0.823201	0.476583
vdsat	0.162938	0.0855844	0.0877921
vgs	0.902408	0.823202	0.828994
vth	0.768274	0.831039	0.831965
id	1.86291e-05	1.7751e-05	1.86291e-05

Figure 16: OP parameters

Spec	*closed loop simulation*	*hand analysis*
DC gain	35.4 dB	35.33 dB
BW	169 KHz	171.8 KHz
GBW	9.8 MHz	10 MHz

Figure 17: closed loop hand analysis

$$DC\ diff\ gain = g_{m4}(r_{o4} \parallel r_{o6}), BW = \frac{1}{2\pi(r_{o4} \parallel r_{o6})C_L}, GBW = \frac{g_{m4}}{2\pi C_L}$$

Spec	*Required*	*Achieved*
Supply Voltage	1.8 V	1.8 V
Load	5 pF	5 pF
Open Loop DC Voltage Gain	$\geq$ 34 dB	35.27 dB
CMRR @DC	$\geq$ 74 dB	81.1 dB
Phase Margin	$\geq$ 70°	89.6°
CM input range – low	$\leq$ 1 V	1 V
CM input range – high	$\geq$ 1.5 V	1.64 V
GBW	$\geq$ 10 MHz	10 MHz
Area	–	42.43 μm^2.
Curren consumption	–	36.4 μA

Table 6: Design specs