

Fast-Transient Low-Dropout Regulator

Main Points



- Introduction
- Design specs
- Design methodology
- Simulation results
- Design challenges

Introduction



- 1. Who are we
- 2. Our goals
 Robust power management unit
- 1. What is an LDO Is it really an LDO?

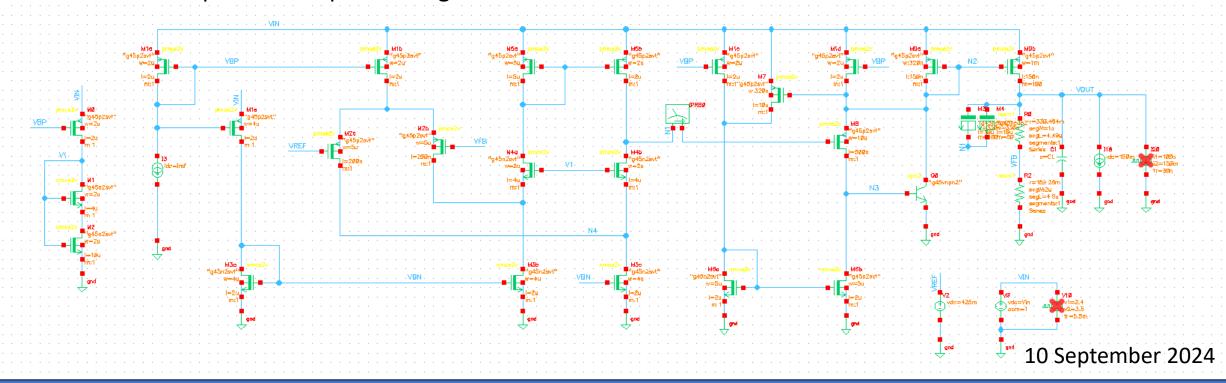
Design Specs



Design Methodology



- LDO Topology
 We want a stable fast-transient topology
- Error Amplifier's Topology
 How is the input and output's swings?



Design Methodology



- Static gain error Map it into V_{ref} , β and $A_{v_{error\ amplifier}}$.
- Stability constraints
 Hard to achieve. What about Miller compensation?
- Load and Line regulation
 How to make the current change negligible?
- Achieving PSR proposals

Simulation Results



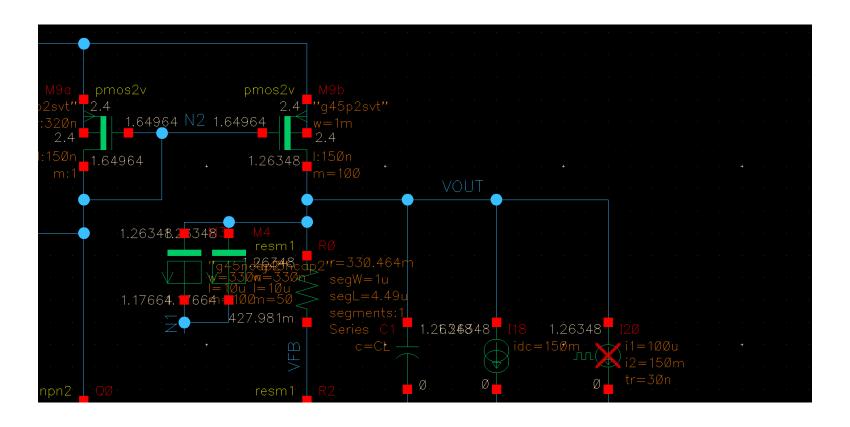
- 1. DC operating parameters simulation
- 2. Transient load simulation
- 3. Transient input simulation
- 4. Stability analysis and PSR
- 5. Figure of merit
- 6. Specs achieved

DC OP Simulation



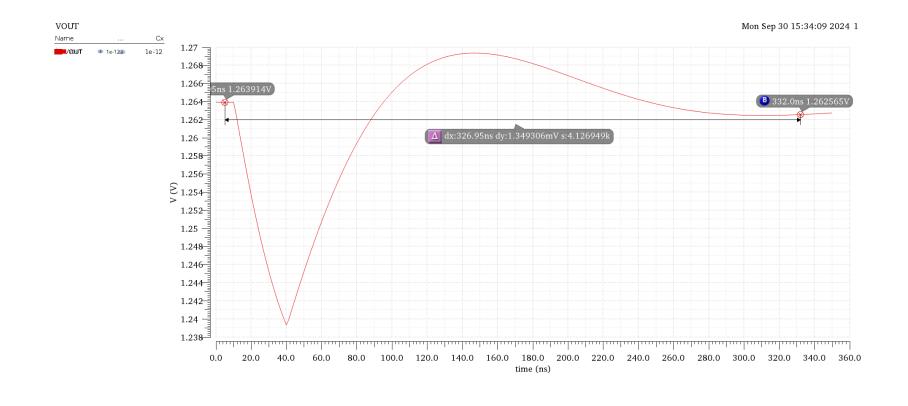
1. Max output error

Evaluated at Minimum $loop\ gain$ (minimum V_{in} &minimum β)



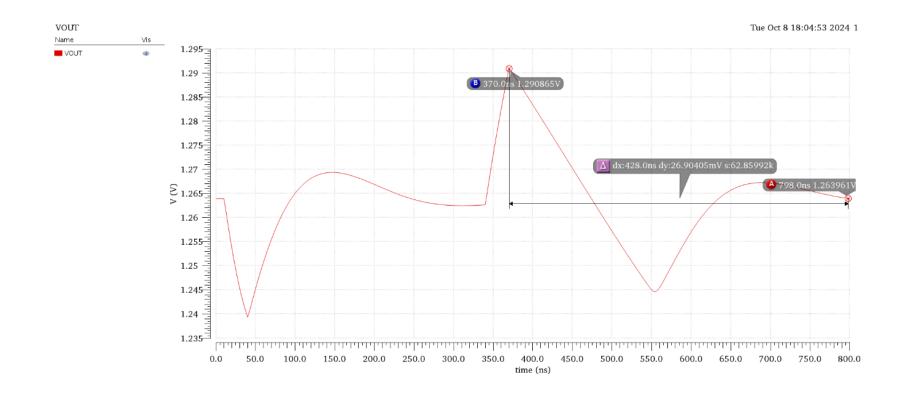


1. Load regulation



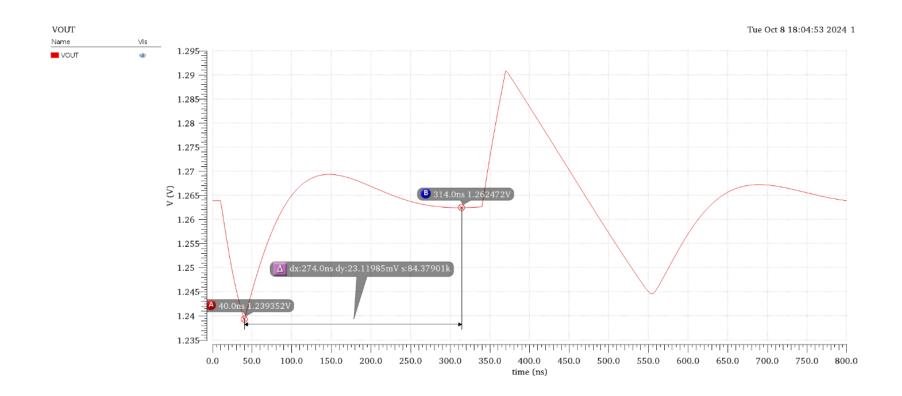


- 1. Load regulation
- 2. Overshoot



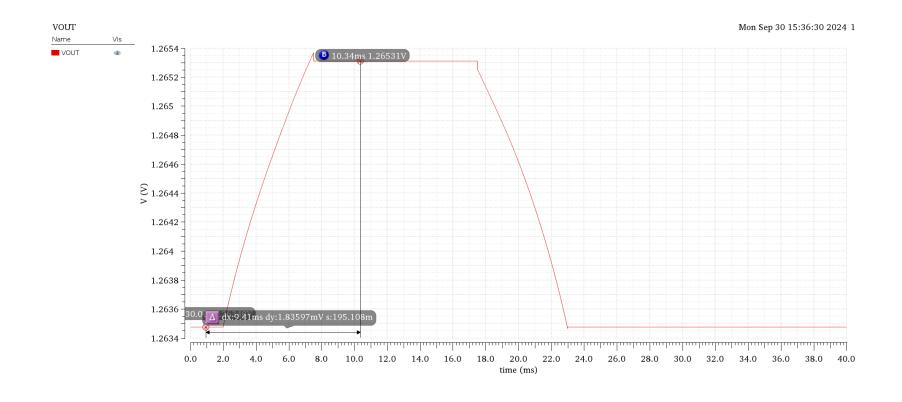


- 1. Load regulation
- 2. Overshoot
- 3. Undershoot





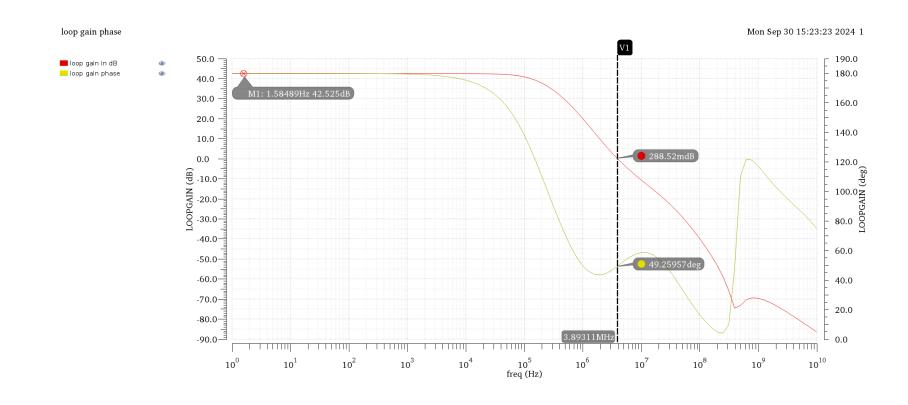
1. Line regulation



Stability Analysis and PSR



1. Phase Margin



Stability Analysis and PSR



1. Phase Margin

2. PSR

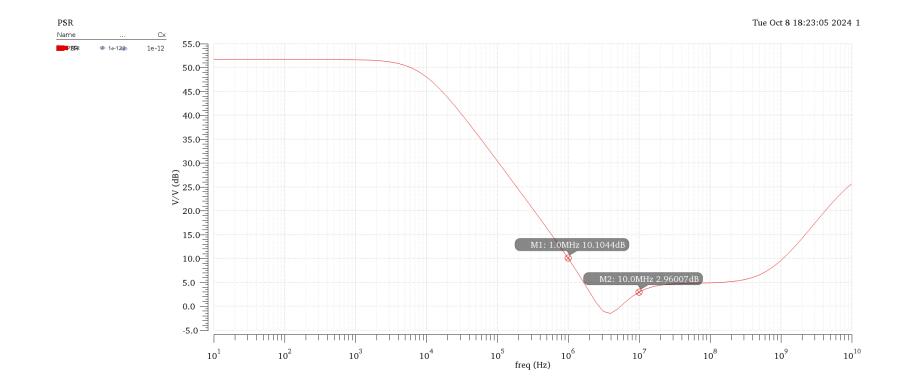


Figure of Merit



$$FOM = \frac{C_L * \Delta V_{out} * I_Q}{I_{L,max}^2} = 2.16 * 10^{-6} (ns)$$

Achieved Specs



Spec	Required	Achieved
Technology used	45nm CMOS	
Supply Voltage	$2.4 V \rightarrow 3.5 V$	_
Output Voltage	$0.85 V \rightarrow 1.25 V$	-
Untrimmed output voltage accuracy	< ±6%	1%
Load Current	$0.1 \ mA \rightarrow 150 \ mA$	_
Undershoot/Overshoot	< 50 mV	27 mV
Phase margin	> 45°	49°
Max Load Capacitance	1 <i>nF</i>	_
Line Regulation	< 2 mV/V	1.7 <i>mV /V</i>
Load Regulation	$< 50 \ mV/A$	9 mV/A
Power Supply Rejection at 1 MHz	30 <i>dB</i>	10 <i>dB</i>
Power Supply Rejection at 10 MHz	20 <i>dB</i>	4 dB
FOM	-	$2.16*10^{-6} (ns)$

Design Challenges



- 1. PSR
 - Bypass device length, low-pass filter and El-Nozahy's paper
- Load regulationMagical mismatch effect
- 3. Line regulation

 Decrease the bypass current change

Thank You

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