
IEEE
Egypt Section

Fast-Transient Low-Dropout Regulator

Main Points

- Introduction
- Design specs
- Design methodology
- Simulation results
- FOM and specs achieved
- Design challenges

Introduction

- **Who are we?**
- **Our goals**
  Robust power management unit
- **What is an LDO?**
  Is it really an LDO?

Design Specs

Parameter	Name	Min	Typ	Max	Units	Comments
Power Supply Voltage	Vin	2.4		3.5	V	
Output Voltage	Vout	0.85	1	1.25	V	Large drop out
Untrimmed Output Voltage Accuracy			±6		%	
Load Current	Iout	0.1		150	mA	Large range of current
Vin Ramp Rate	dVin/dt			0.2	mV/µs	
Rate of Iout Change	dIout/dt			5	mA/ns	
Undershoot/Overshoot				50	mV	
Load Capacitance	CL			1	nF	Not large enough
Power Supply Rejection at 1 MHz	PSR1MHz	30			dB	
Power Supply Rejection at 10 MHz	PSR10MHz	20			dB	Large PSR bandwidth
Line Regulation			2		mV/V	
Load Regulation			50		mV/A	

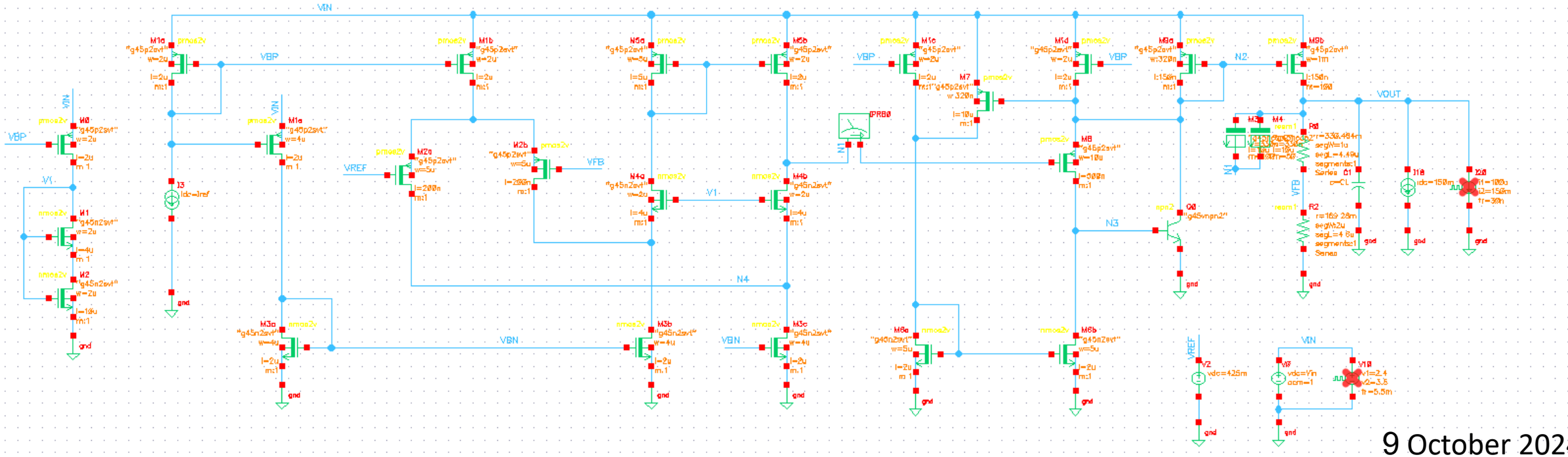
Design Methodology

- **LDO Topology**

  We want a stable fast-transient topology

- **Error Amplifier's Topology**

  How is the input and output's swings?



9 October 2024

Design Methodology

- **Static gain error**

  Map it into $V_{ref}, \beta \; and \; A_{v_{error\ amplifier}}$

- **Stability constraints**

  Hard to achieve. What about Miller compensation?

- **Load and Line regulation**

  How to make the current percent change negligible?

- **Achieving PSR proposals**

Simulation Results

1. **DC operating parameters simulation**

2. **Transient load simulation**

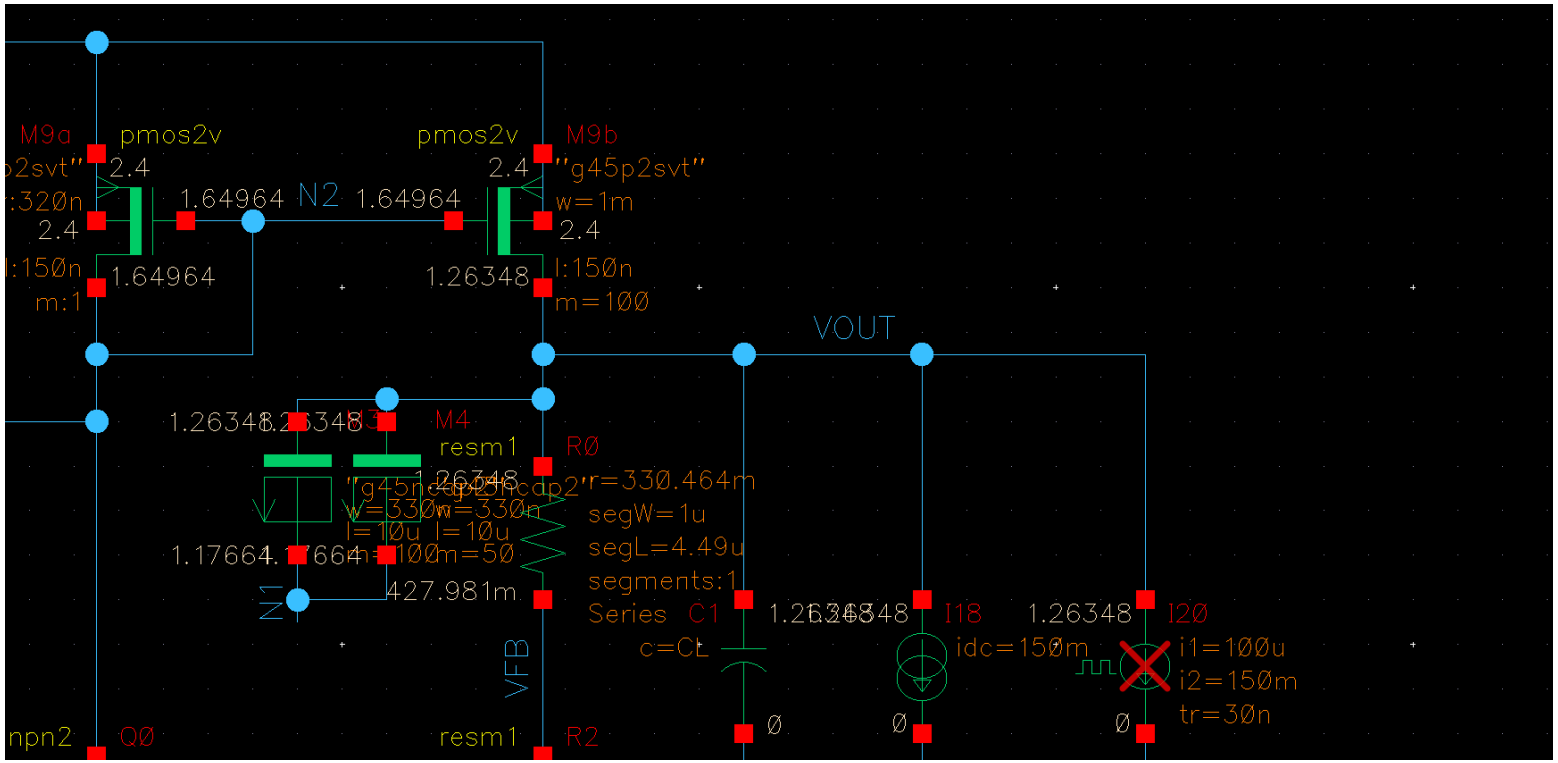
3. **Transient input simulation**

4. **Stability analysis and PSR**

DC OP Simulation

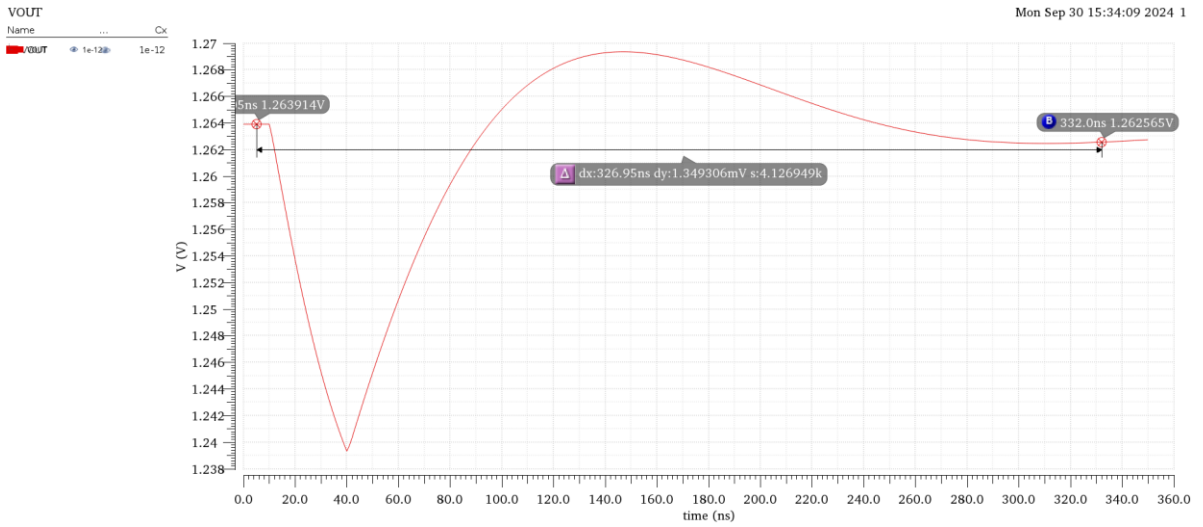
1. **Max output error**

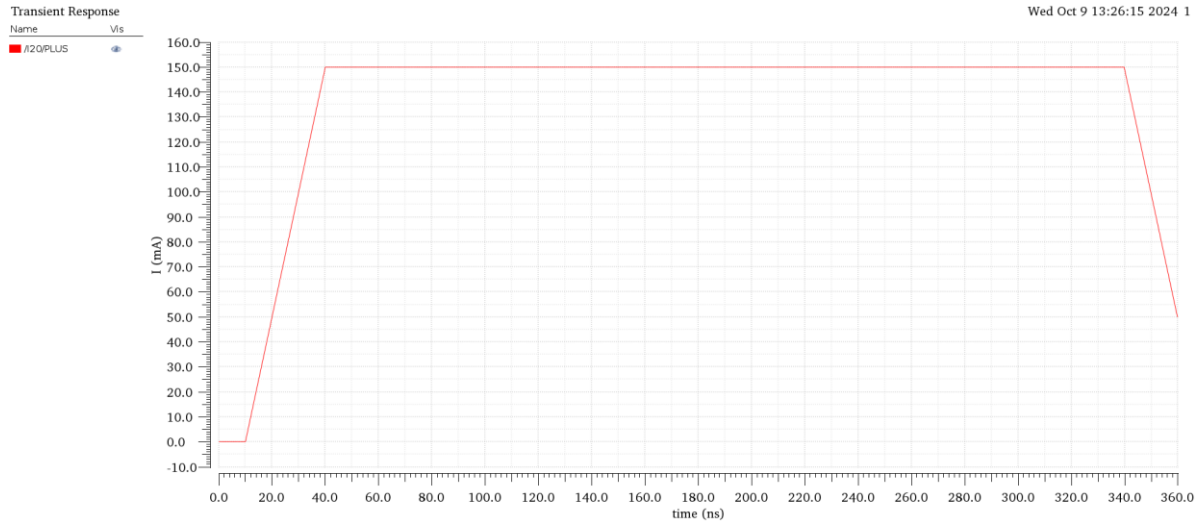
   Evaluated at Minimum $loop\ gain$ (minimum V_{in} &minimum β)



Transient Load Simulation

1. **Load regulation**



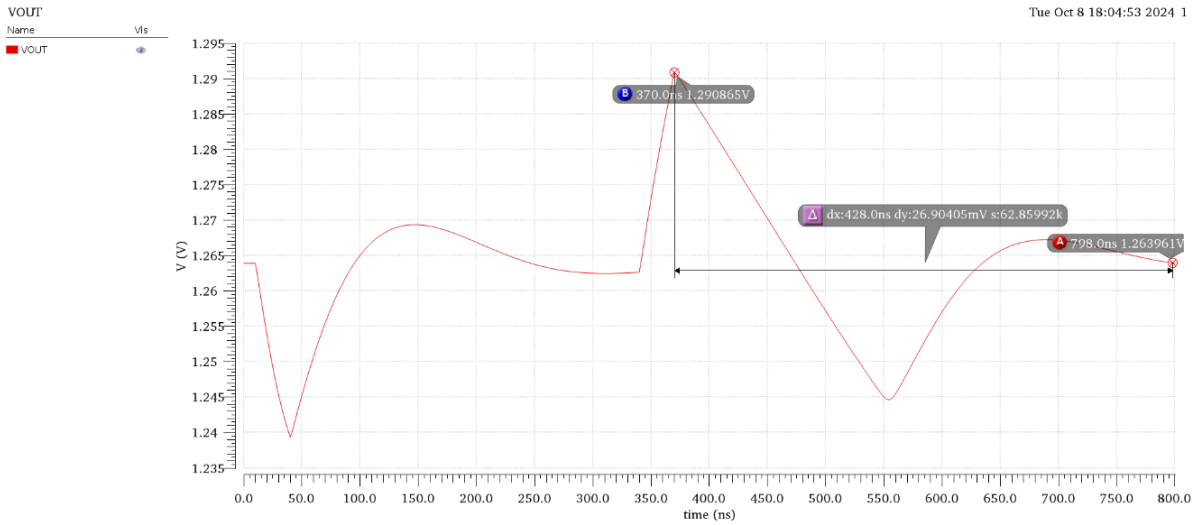


9 October 2024

Transient Load Simulation

1. **Load regulation**

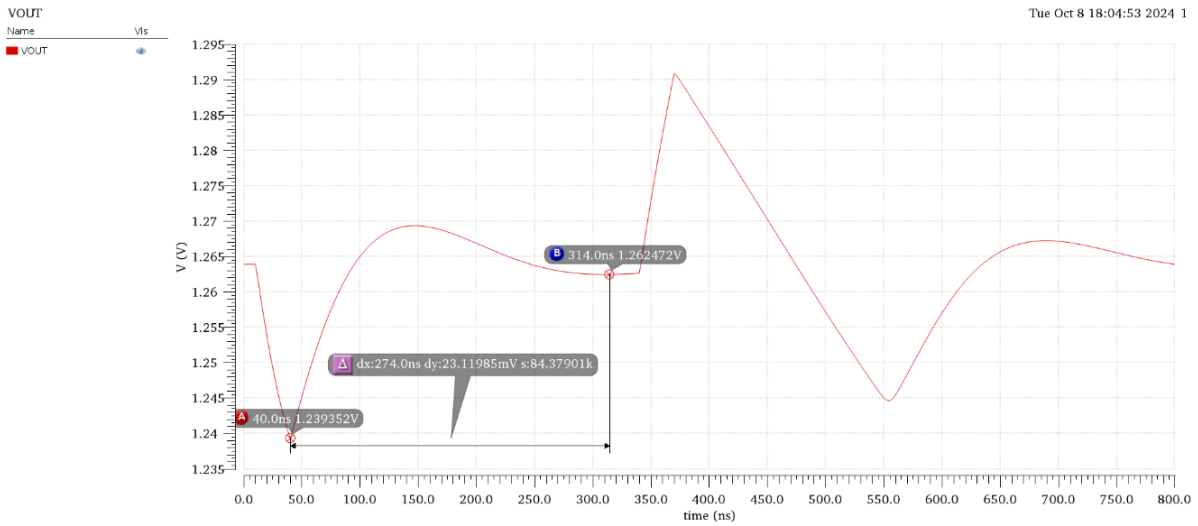
2. **Overshoot**



9 October 2024

Transient Load Simulation

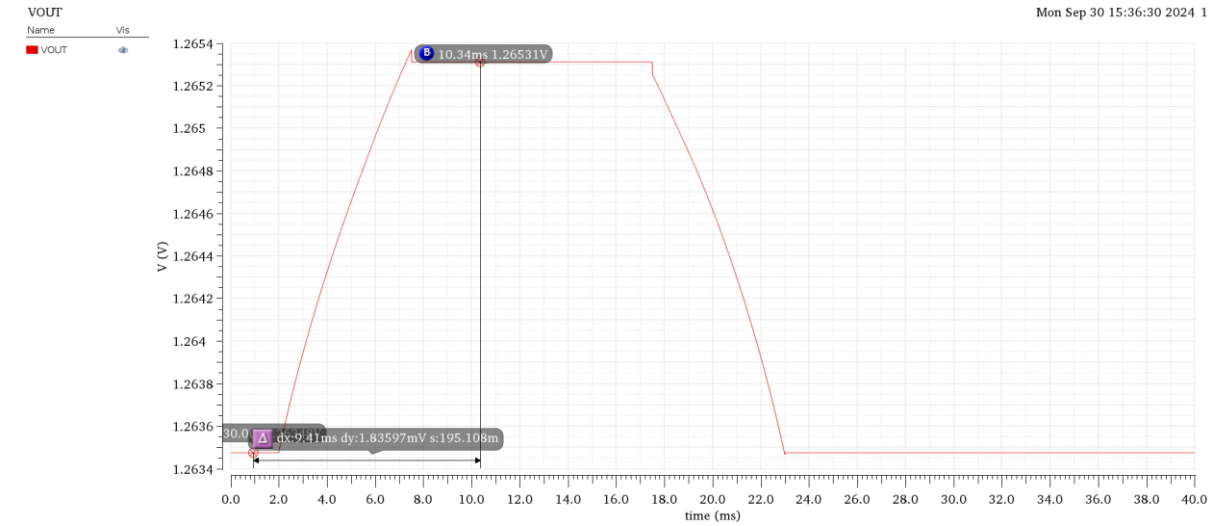
1. **Load regulation**
2. **Overshoot**
3. **Undershoot**

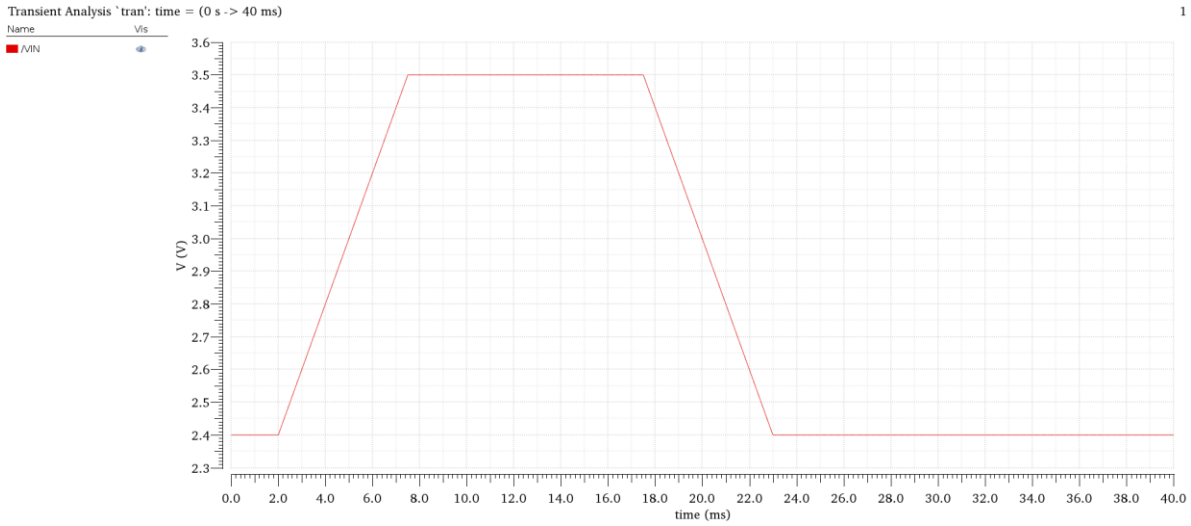


9 October 2024

Transient Input Simulation

1. **Line regulation**

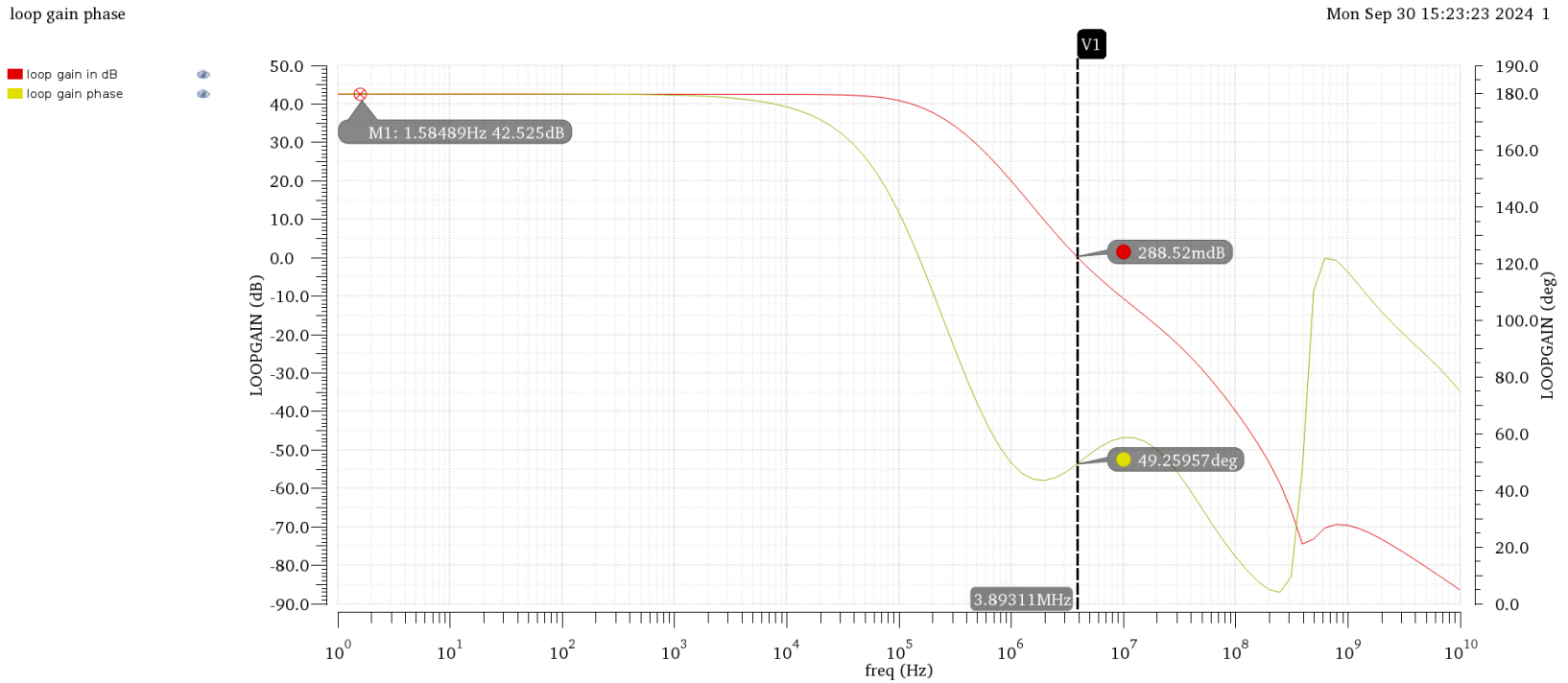




9 October 2024

Stability Analysis and PSR

1. Phase Margin

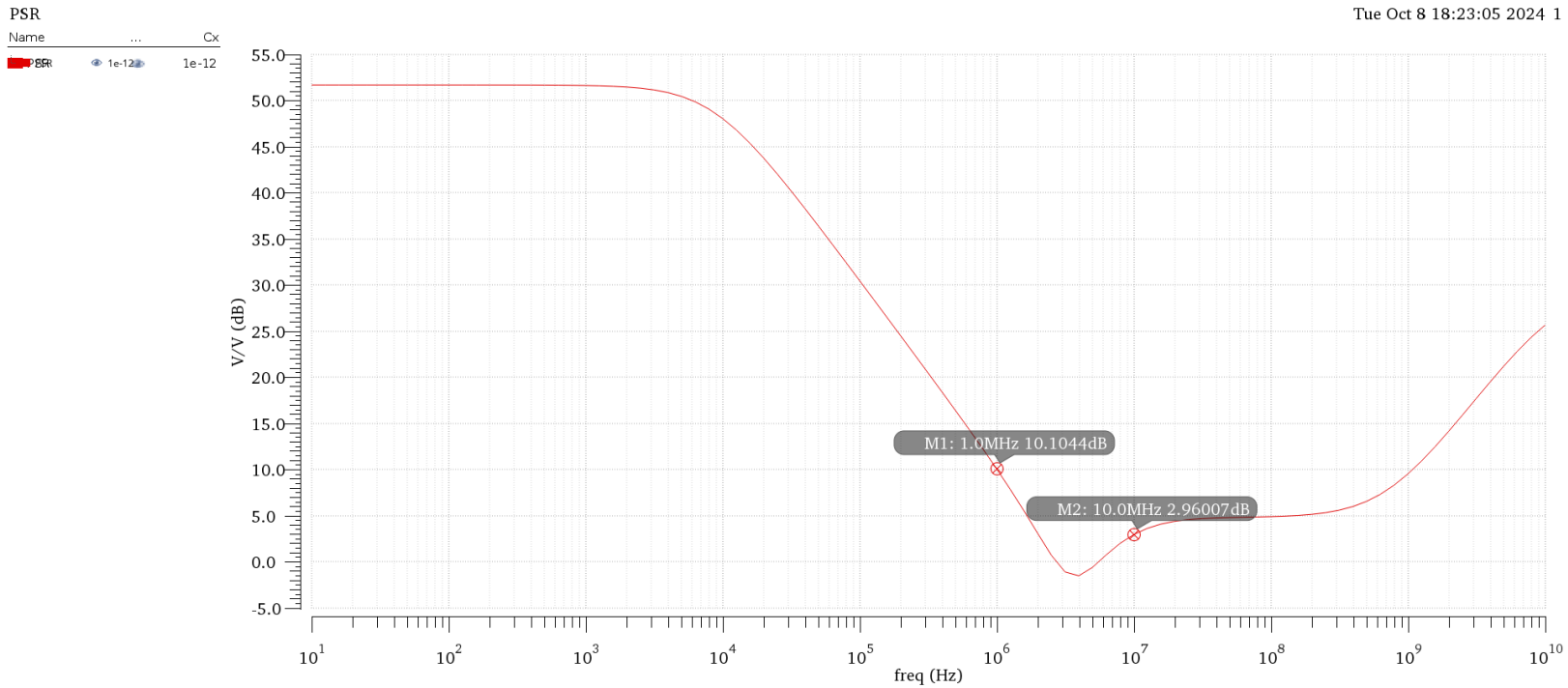


9 October 2024

Stability Analysis and PSR

1. **Phase Margin**

2. **PSR**



9 October 2024

Figure of Merit

$$FOM = \frac{C_L * \Delta V_{out} * I_Q}{I_{L,max}^2} = 2.16 * 10^{-6}\ (ns)$$

Achieved Specs

Spec	Required	Achieved
Technology used	$45nm\ CMOS$	
Supply Voltage	$2.4\ V \rightarrow 3.5\ V$	–
Output Voltage	$0.85\ V \rightarrow 1.25\ V$	–
Untrimmed output voltage accuracy	$< \pm 6\%$	1%
Load Current	$0.1\ mA \rightarrow 150\ mA$	–
Undershoot/Overshoot	$< 50\ mV$	$27\ mV$
Phase margin	$> 45^o$	49^o
Max Load Capacitance	$1\ nF$	–
Line Regulation	$< 2\ mV/V$	$1.7\ mV/V$
Load Regulation	$< 50\ mV/A$	$9\ mV/A$
Power Supply Rejection at 1 MHz	$30\ dB$	$10\ dB$
Power Supply Rejection at 10 MHz	$20\ dB$	$4\ dB$
FOM	–	$2.16 * 10^{-6}\ (ns)$

Design Challenges

1. **Why Al-shyoukh?**
   Fast-transient response and stability

2. **PSR**
   Bypass device length, low-pass filter and El-Nozahy's paper

3. **Line regulation**
   Magical mismatch effect

4. **Load regulation**
   Decrease the bypass current normalized change

Thank You

Presented by
Mohamed Essam
Bilal Ramadan
Abdelrahman Abohendy
Mahmoud Saker

For more details

9 October 2024