Fast-Transient Low Dropout Regulator

IEEE SSCS

Table of Contents

Table of Figures

Part 1: Group Members

1	**Bilal Ramadan Helmy**
2	**Abdelrahman Mohamed Abohendy**
3	**Mahmoud Abdelsalam Saker**
4	**Mohamed Essam Abdelazim**

Part 1: Design Specs

Spec	Required	Achieved
Technology used	$45nm\ CMOS$	
Supply Voltage	$2.4\ V \rightarrow 3.5\ V$	–
Output Voltage	$0.85\ V \rightarrow 1.25\ V$	–
Untrimmed output voltage accuracy	$< \pm 6\%$	1%
Load Current	$0.1\ mA \rightarrow 150\ mA$	–
Undershoot/Overshoot	$< 50\ mV$	$27\ mV$
Phase margin	$> 45^o$	49^o
Max Load Capacitance	$1\ nF$	–
Line Regulation	$< 2\ mV/V$	$1.7\ mV/V$
Load Regulation	$< 50\ mV/A$	$9\ mV/A$
Power Supply Rejection at 1 MHz	$30\ dB$	$10\ dB$
Power Supply Rejection at 10 MHz	$20\ dB$	$4\ dB$
FOM	–	$2.16 * 10^{-6}\ (ns)$

Part 2: Design Methodology

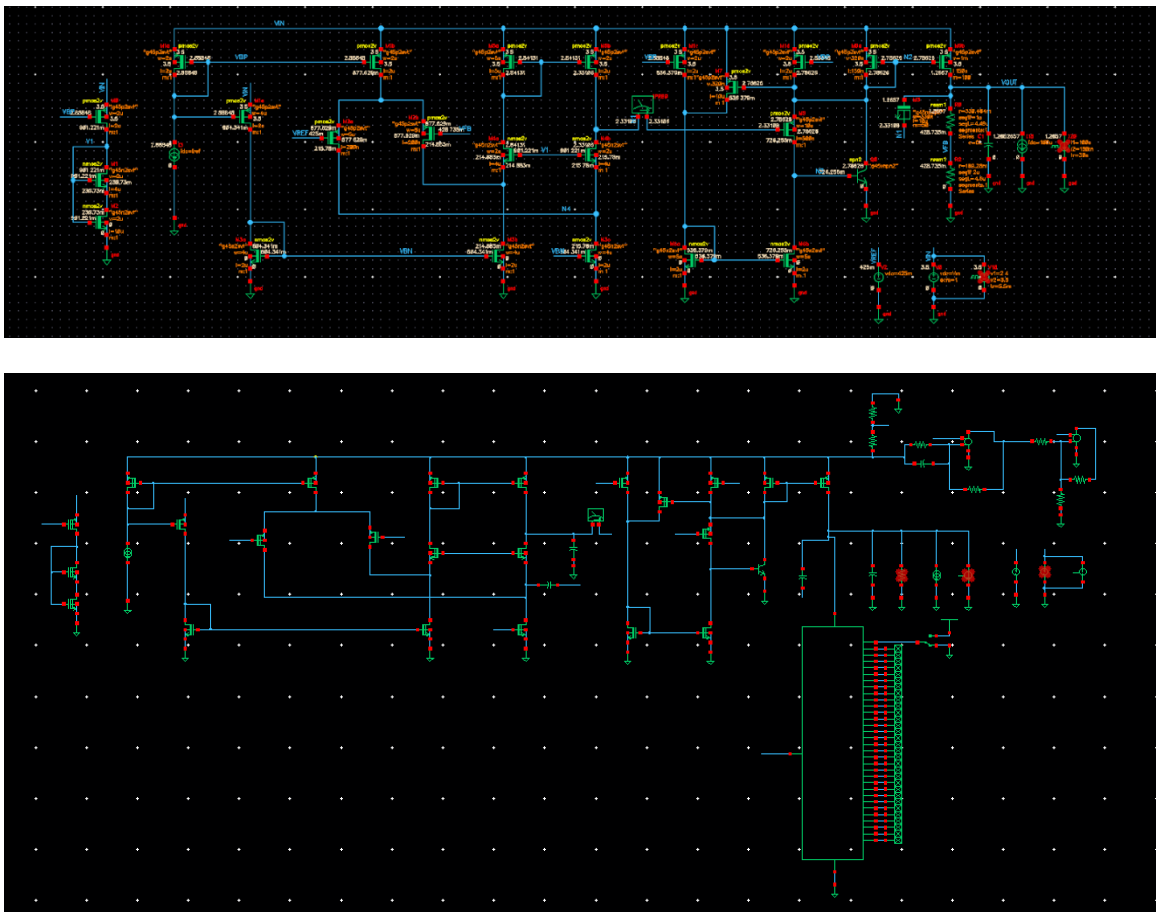

Figure 1: schematics

Our design methodology, based on the work of Al-Shyoukh (2007)[1], focused primarily on enhancing the transient response of the low-dropout (LDO) regulator while maintaining stability requirements.

To achieve this, we ensured the output pole was dominant and shifted the pole at the bypass transistor gate to a non-dominant position by incorporating a buffer between the error amplifier

[1] IEEE JOURNAL OFSOLID-STATE CIRCUITS, VOL. 42, NO. 8, AUGUST 2007

and the bypass gate and used small feedback resistors so we get very high frequency non-dominant pole at the output node. Additionally, we used a compensation capacitor to compensate the pole at the error amplifier's output. The resulting high bandwidth, along with maintained stability, enabled us to meet the specifications for both load and line regulation.

Main design points:

- The amplifier's CMIR spec is around Vref which is 425 mV.
- The amplifier's DC gain spec is specified from the error spec at minimum feedback factor (β) which is $\frac{1.25}{0.425}$.
- The switches are made by MOSFETs with minimum length and large width which is $6\ \mu m$.
- The biasing voltages are included.
- In order to increase line and load regulations we decreased the feedback resistors so the MOSFET current increased and the load current effect decreases. Also the PSR is increased as the PSR is a voltage divider between them and ro. ro change is not straight forward because I increases so gm/Id decreases which causes VA increase.
- All LDO components are from the PDK. Caps are small so we used two in parallel to get the compensation capacitance needed.
- Stability and PSR specs' worst case is at $I_L = 0.1\ mA, V_{in} = 2.4\ V$ as the non-dominant pole (at the output node gets nearer due to the increase in the load resistance).
- Load regulation's worst case is at $V_{in} = 2.4\ V$.
- Line regulation's worst case is at $I_L = 150\ mA$.

Part 3: Simulation Results

1. DC OP simulation

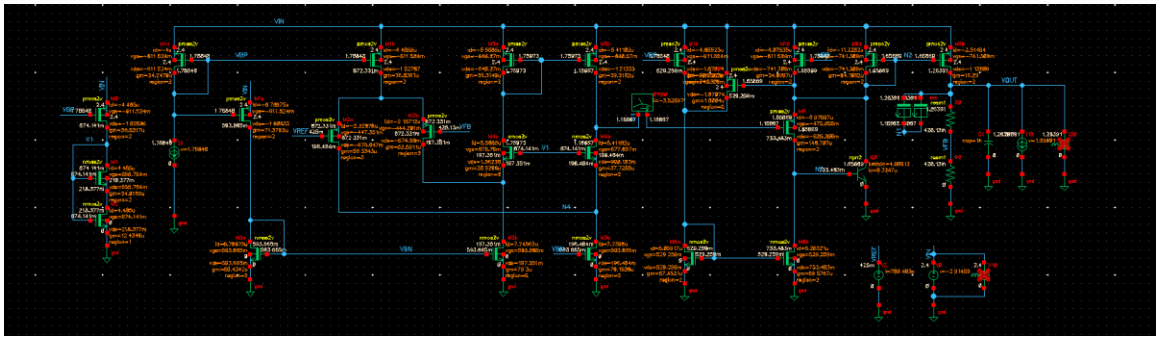

Figure 1: DC OP at Vin=2.4V and IL=0.1mA

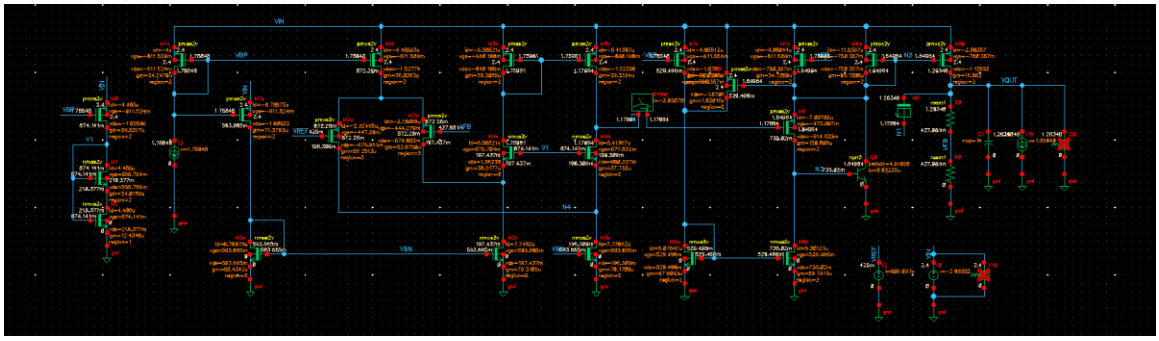

Figure 2: DC OP at Vin=2.4V and IL=150mA

$Max\ error = 1.12\%, I_Q = 36\ \mu A$

2. Transient load simulation

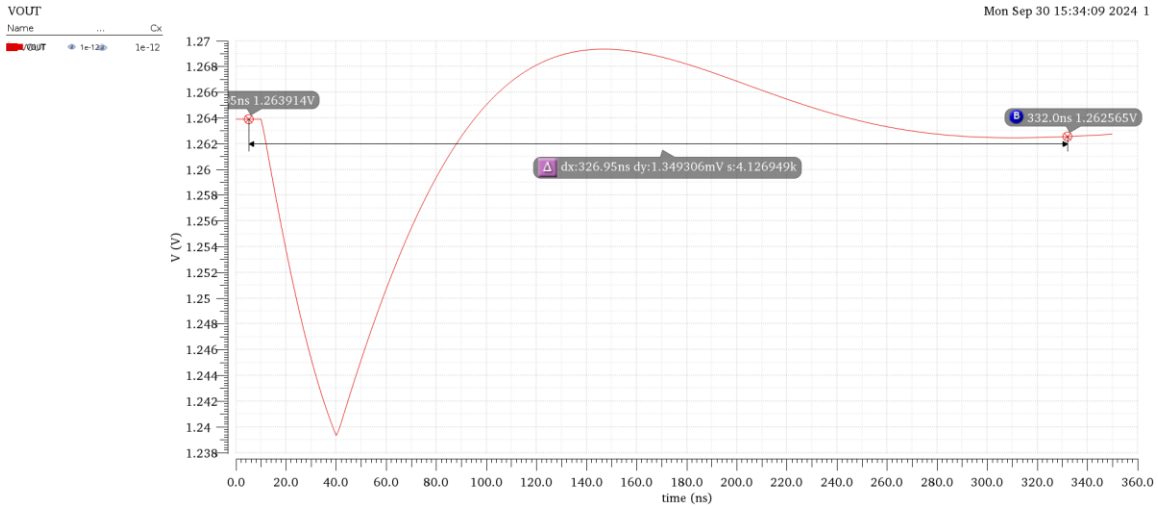

Figure 3: Load regulation

$$\Delta V_{out} = 1.35\ mV, Load\ regulation = \frac{1.35}{0.15} = 9\ mV/A$$

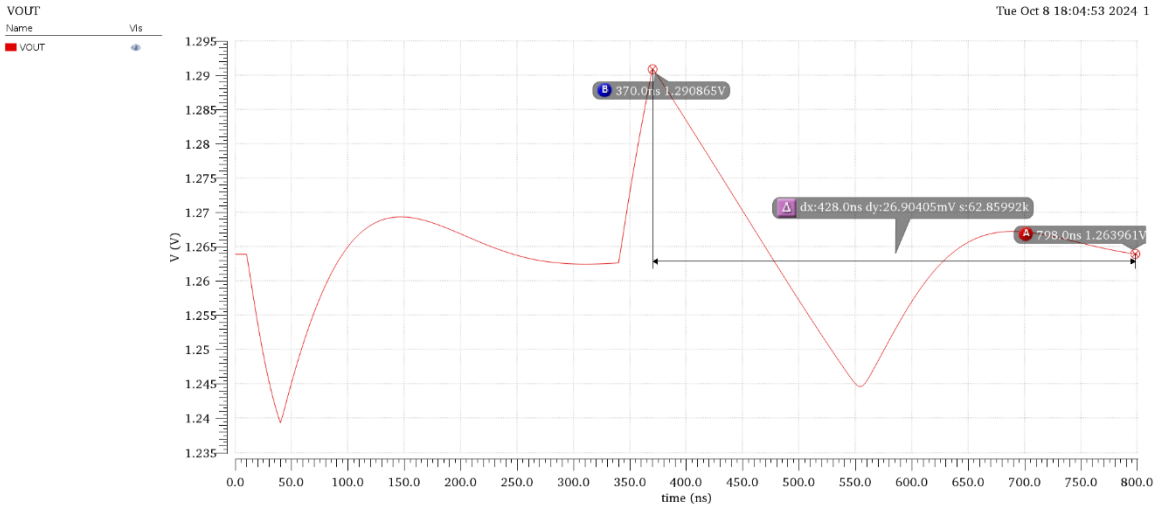

Figure 4: Overshoot

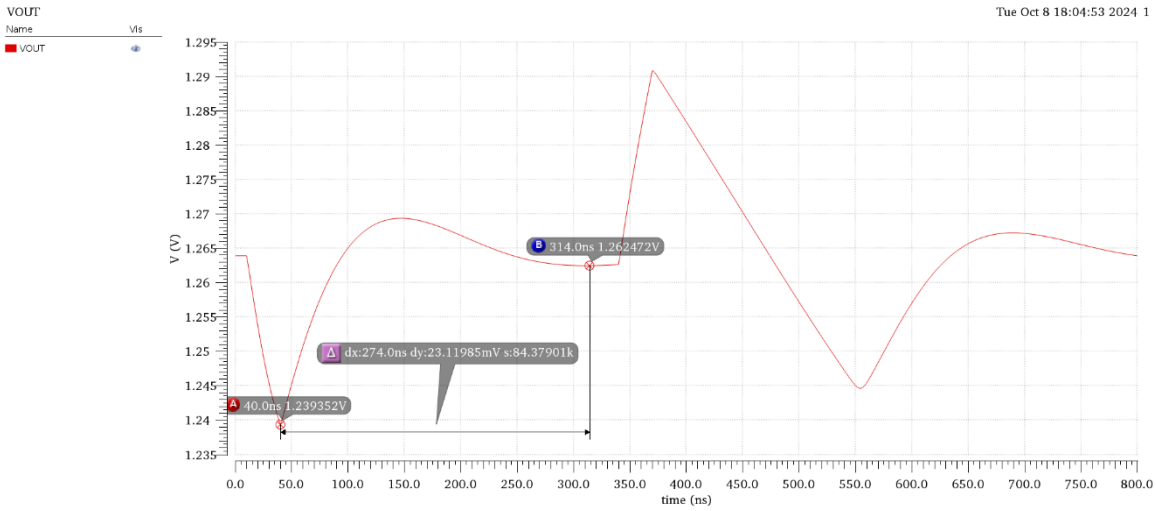

Figure 5: Undershoot

Overshoot $= 26.9\ mV$, Undershoot$= 23.1\ mV$

3. Transient input simulation

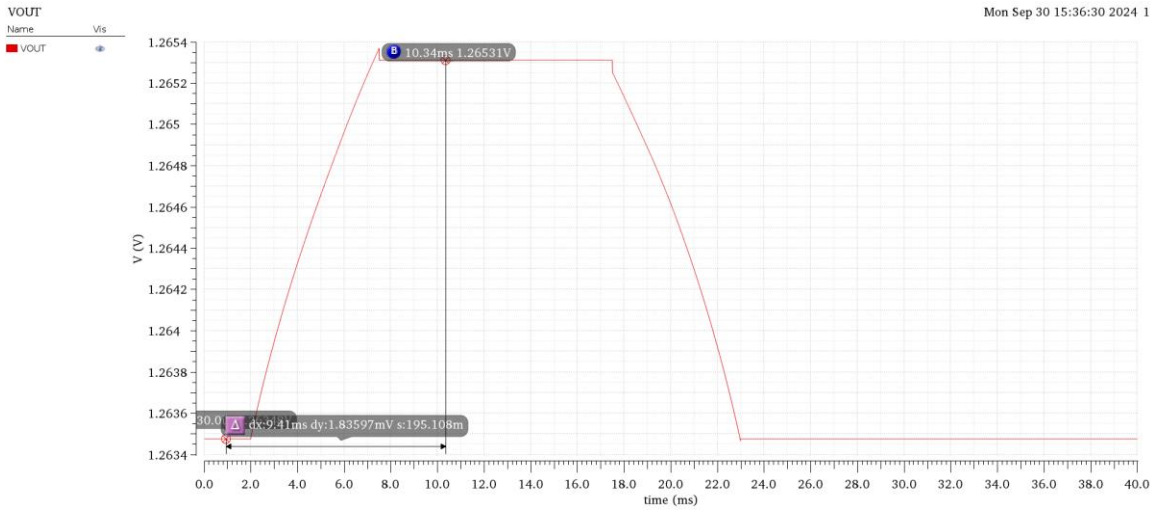

Figure 6: Line regulation

$$Line\ regulation = \frac{1.84}{1.1} = 1.7\ mV$$

4. Stability analysis and PSR

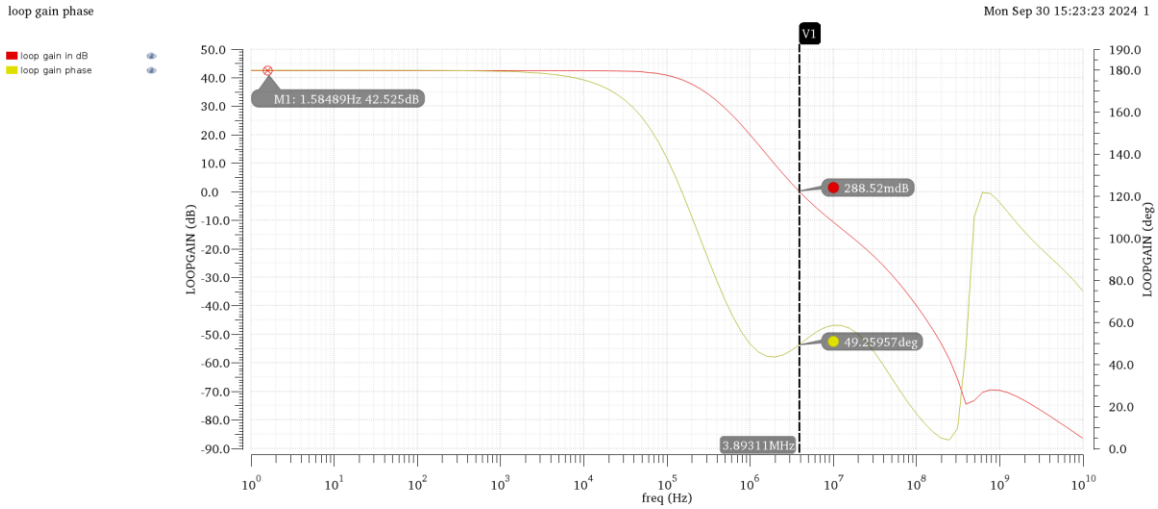

Figure 7: minimum phase margin

Minimum phase margin is at $I_L = 0.1\ mA, V_{in} = 2.4\ V$, equals 49^o.

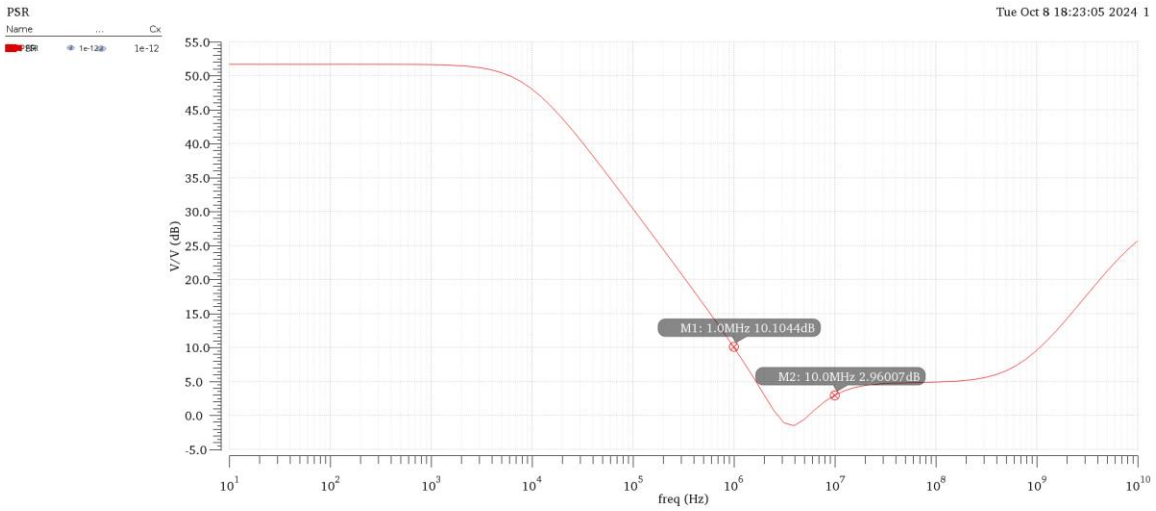

Figure 8: minimum PSR

Minimum PSR is at $I_L = 0.1\ mA, V_{in} = 2.4\ V$. We sadly did not achieve the PSR spec.

5. Figure of merit

$$FOM = \frac{C_L * \Delta V_{out} * I_Q}{I_{L,max}^2} = 2.16 * 10^{-6}\ (ns)$$

Part 4: Design challenges

I. We faced most of our challenges with meeting the power supply rejection (PSR) specifications, and attempted several approaches to address this:

   1. We increased the length of the bypass transistor to reduce the effects of channel length modulation and isolate ripples at VDD from the output. This was combined with lowering the values of the feedback resistors to preserve the voltage divider between ro and the feedback resistors. However, this approach failed as the current was too high, keeping gds large and leading to poor PSR performance but it got better than first.

   2. We also tried adding a low-pass filter (LPF) after VDD, but this significantly affected the high frequency operation so we got poor load and line regulations and the DC operating point because V_{DD-DC} becomes a voltage divider between the very small resistors parallel combination and the LPF resistor, resulting in incorrect V_{out}. Also tried decreasing the LPF resistor but the results were still unacceptable.

   3. As a last try we used El-Nozahy paper[2] whose purpose is to increase the bandwidth of PSR by introducing a second loop to cancel the noise from the V_{DD} but when putting the ideal and behavioural models to test the performance it only increased it by 3 dB only and we found it hard to understand the paper well at this limited time.

II. Other challenge faced us was the load regulation spec, it was small but we achieved it by increasing the error amplifier gain and introducing mismatch between its load transistors so the amplifier's output node DC level is shifted up enhancing the buffer operation.

III. The last challenge was the line regulation spec, which we enhanced by decreasing feedback resistors as mentioned before.

The end.

[2] IEEE JOURNAL OFSOLID-STATE CIRCUITS, VOL. 45, NO. 3, MARCH 2010