Fast-Transient Low-Dropout Regulator

Main Points

- Introduction
- Design specs
- Design methodology
- Simulation results
- Design challenges

Introduction

- **Who are we**
- **Our goals**
  Robust power management unit
- **What is an LDO**
  Is it really an LDO?

Design Specs

Parameter	Name	Min	Typ	Max	Units	Comments
Power Supply Voltage	Vin	2.4		3.5	V	Large range for drop out
Output Voltage	Vout	0.85	1	1.25	V	Programmable with 12.5 mV step
Untrimmed Output Voltage Accuracy			±6		%	
Load Current	Iout	0.1		150	mA	Large range of current
Vin Ramp Rate	dVin/dt			0.2	mV/µs	
Rate of Iout Change	dIout/dt			5	mA/ns	Load transient regulation for maximum load variation at maximum capacitance
Undershoot/Overshoot				50	mV	
Load Capacitance	CL			1	nF	Not a large enough
Power Supply Rejection at 1 MHz	PSR1MHz	30			dB	
Power Supply Rejection at 10 MHz	PSR10MHz	20			dB	
Line Regulation			2		mV/V	
Load Regulation			50		mV/A	

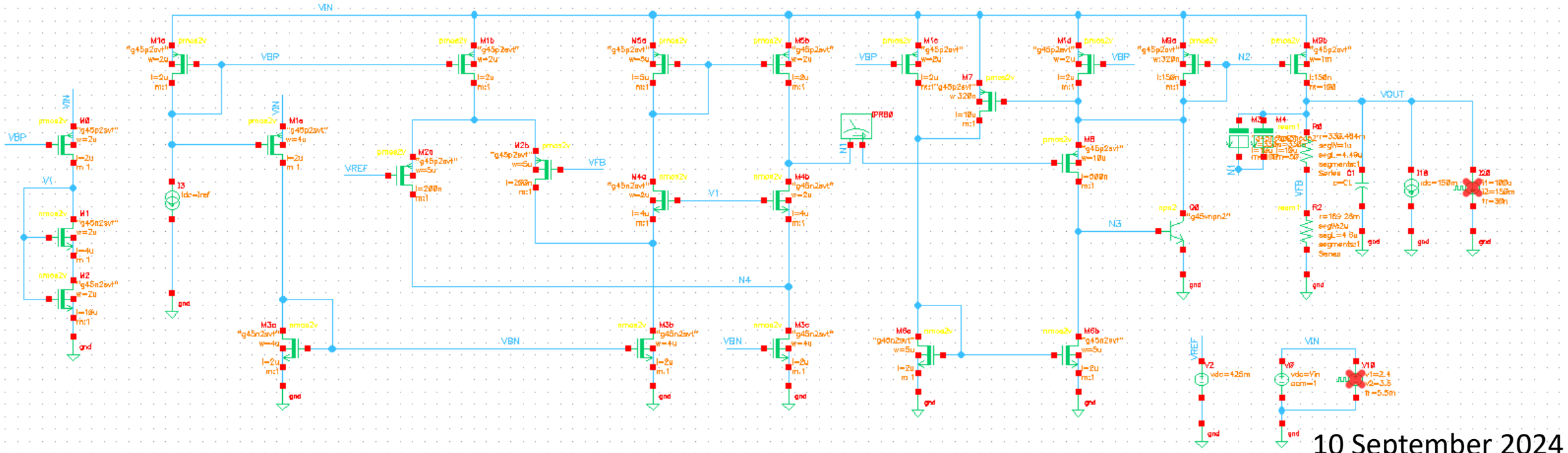
Design Methodology

- **LDO Topology**

  We want a stable fast-transient topology

- **Error Amplifier's Topology**

  How is the input and output's swings?



Design Methodology

- **Static gain error**

  Map it into $V_{ref}, \beta \; and \; A_{v_{error\; amplifier}}$.

- **Stability constraints**

  Hard to achieve. What about Miller compensation?

- **Load and Line regulation**

  How to make the current change negligible?

- **Achieving PSR proposals**

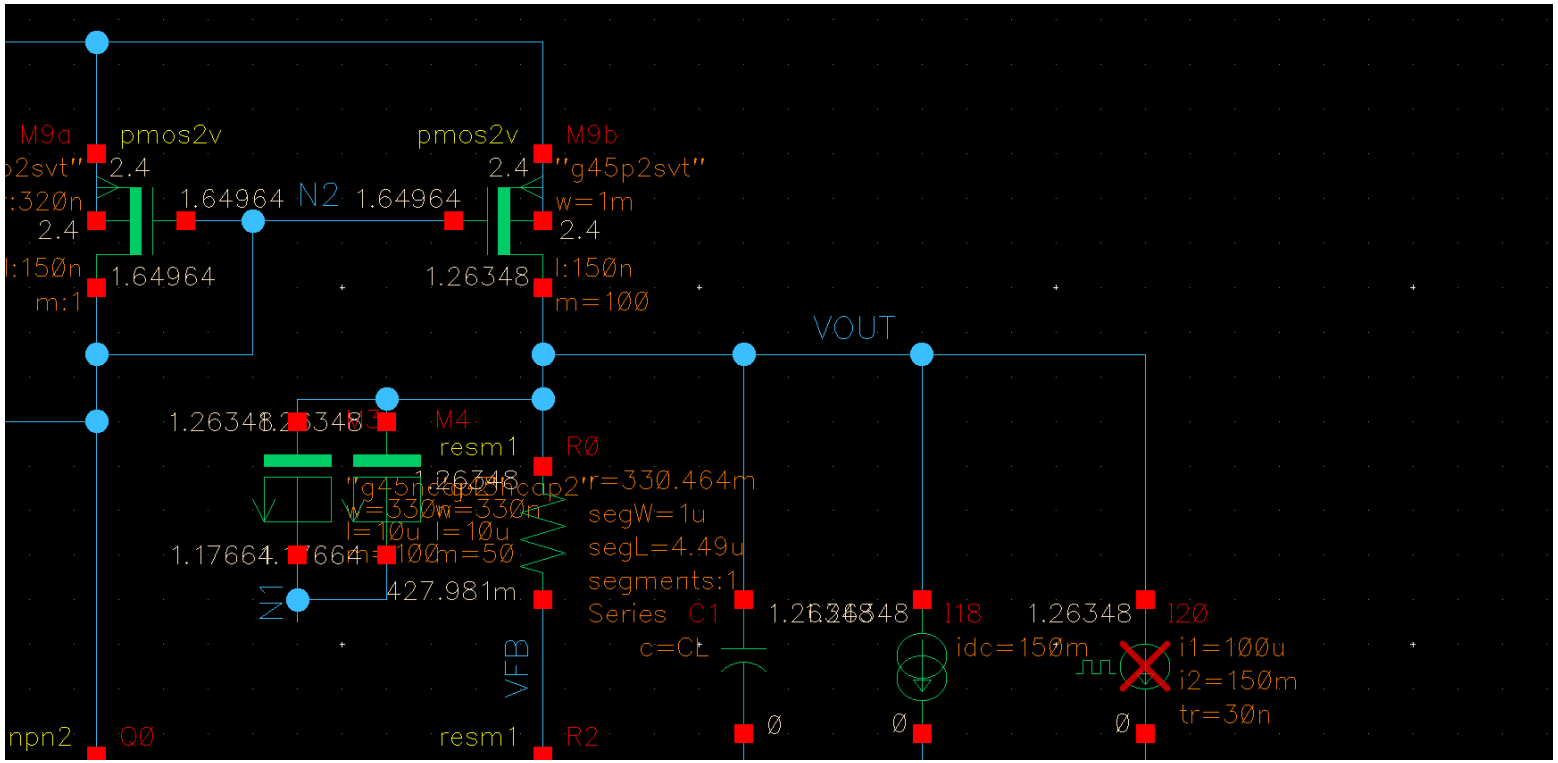
Simulation Results

1. DC operating parameters simulation
2. Transient load simulation
3. Transient input simulation
4. Stability analysis and PSR
5. Figure of merit
6. Specs achieved

DC OP Simulation

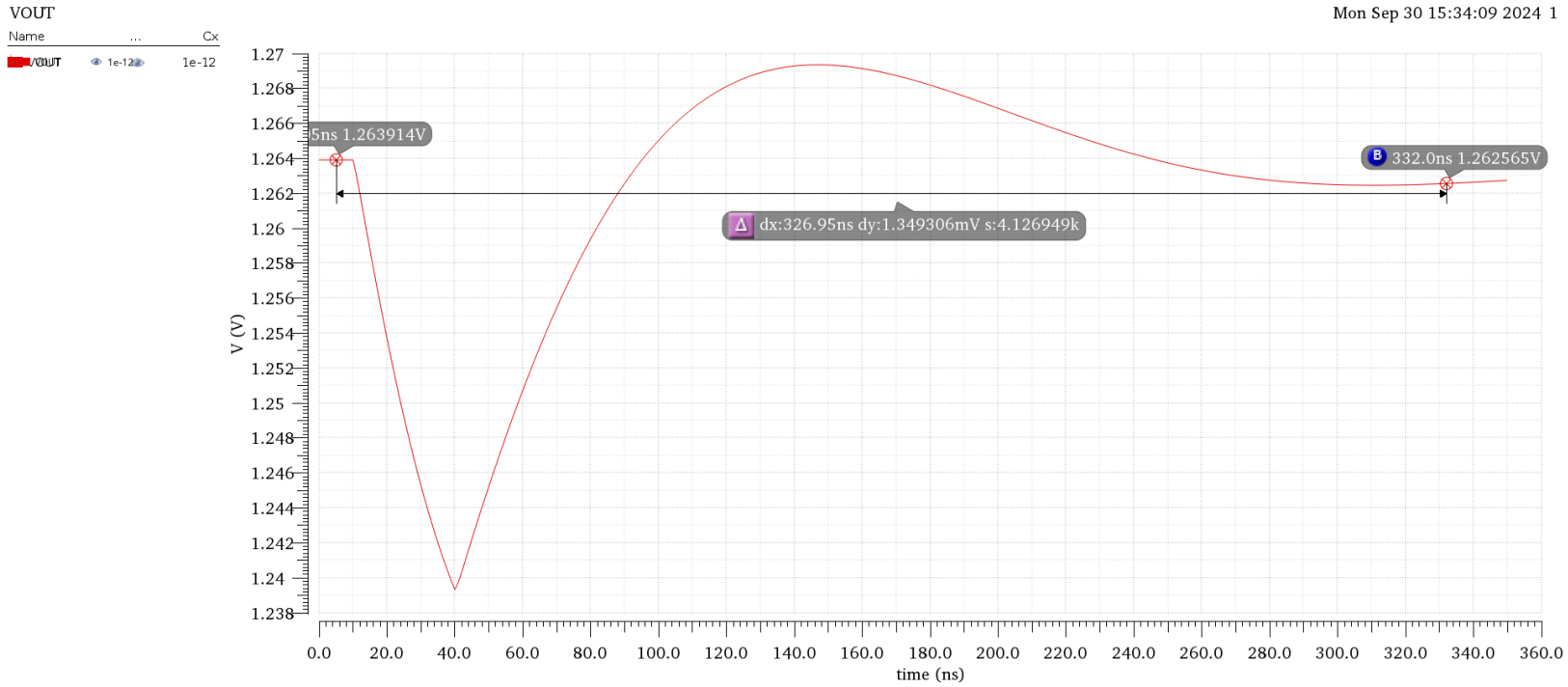
1. **Max output error**

   Evaluated at Minimum $loop\ gain$ (minimum V_{in} &minimum β)



Transient Load Simulation

1. Load regulation



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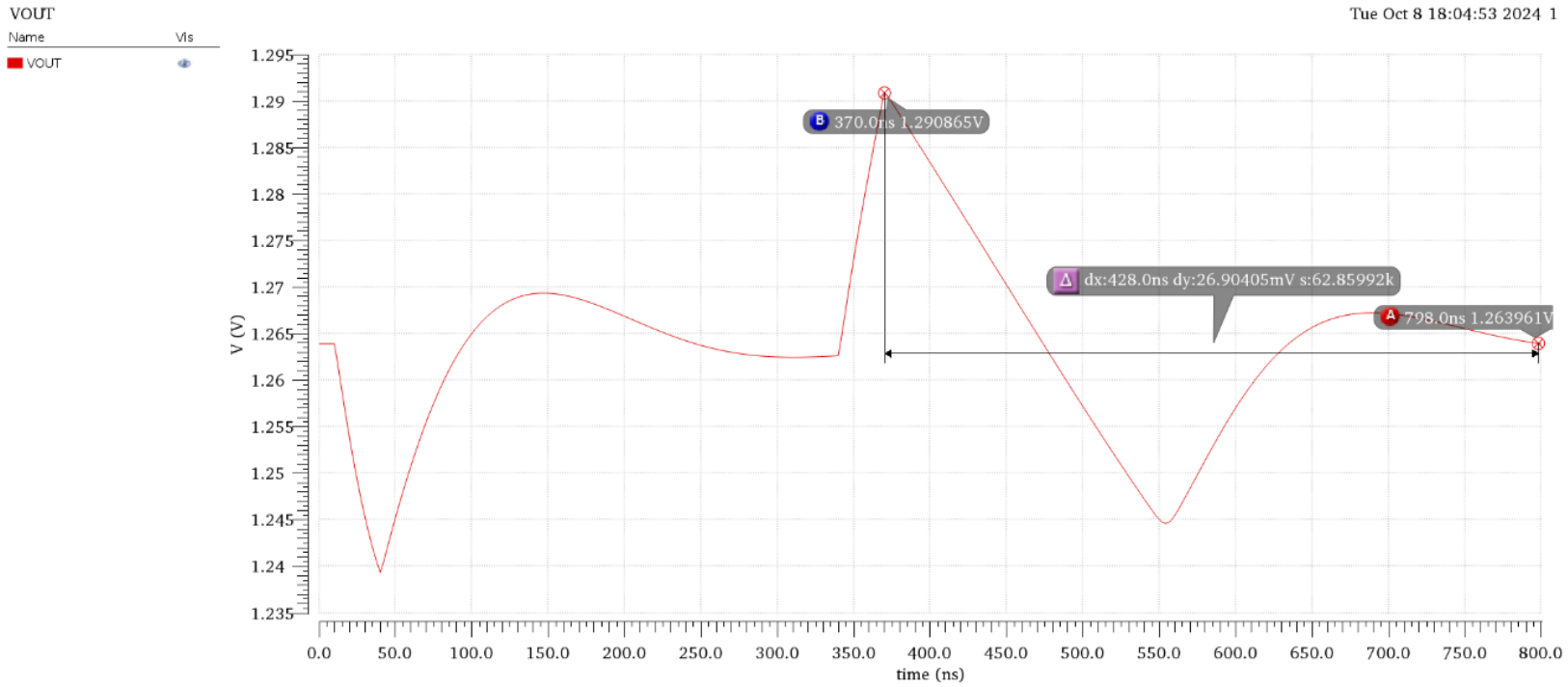
Transient Load Simulation

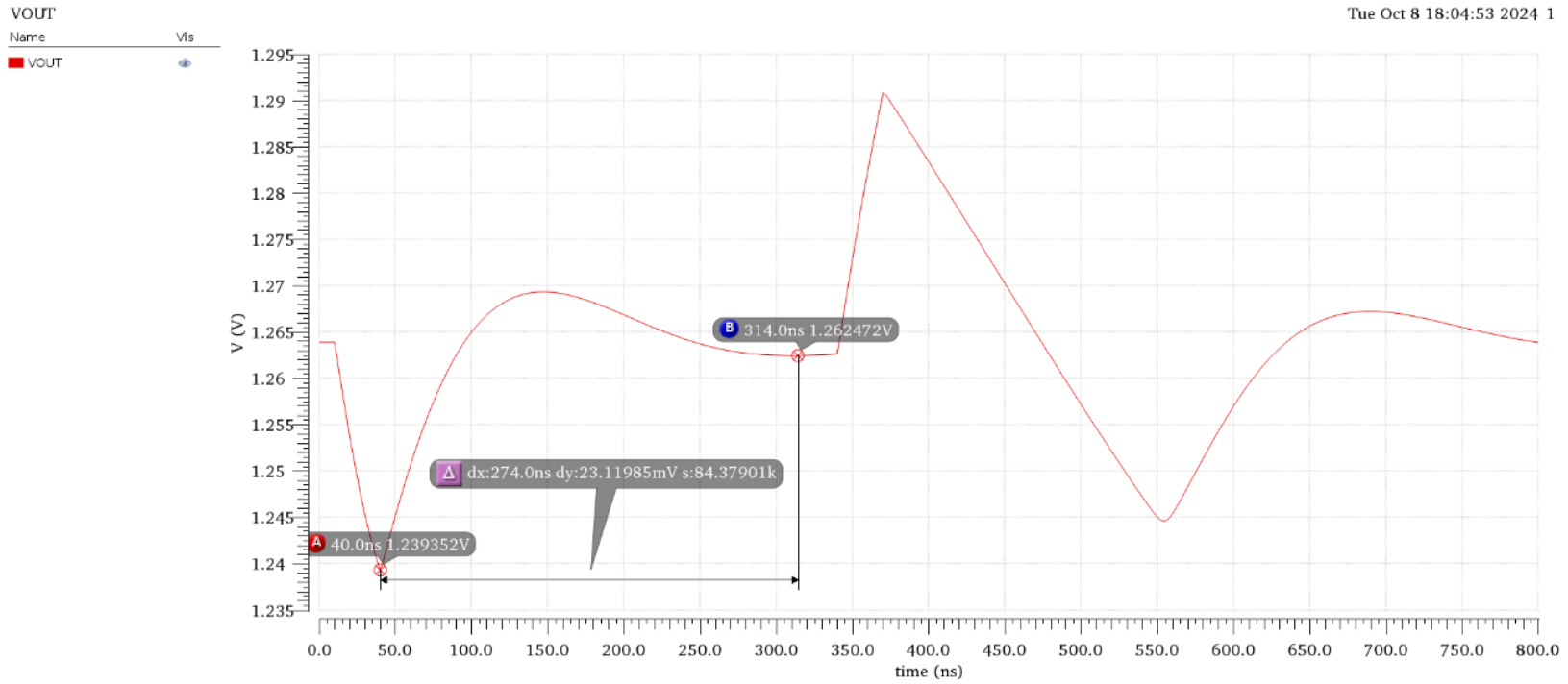
1. Load regulation

2. Overshoot



Transient Load Simulation

1. Load regulation
2. Overshoot
3. Undershoot



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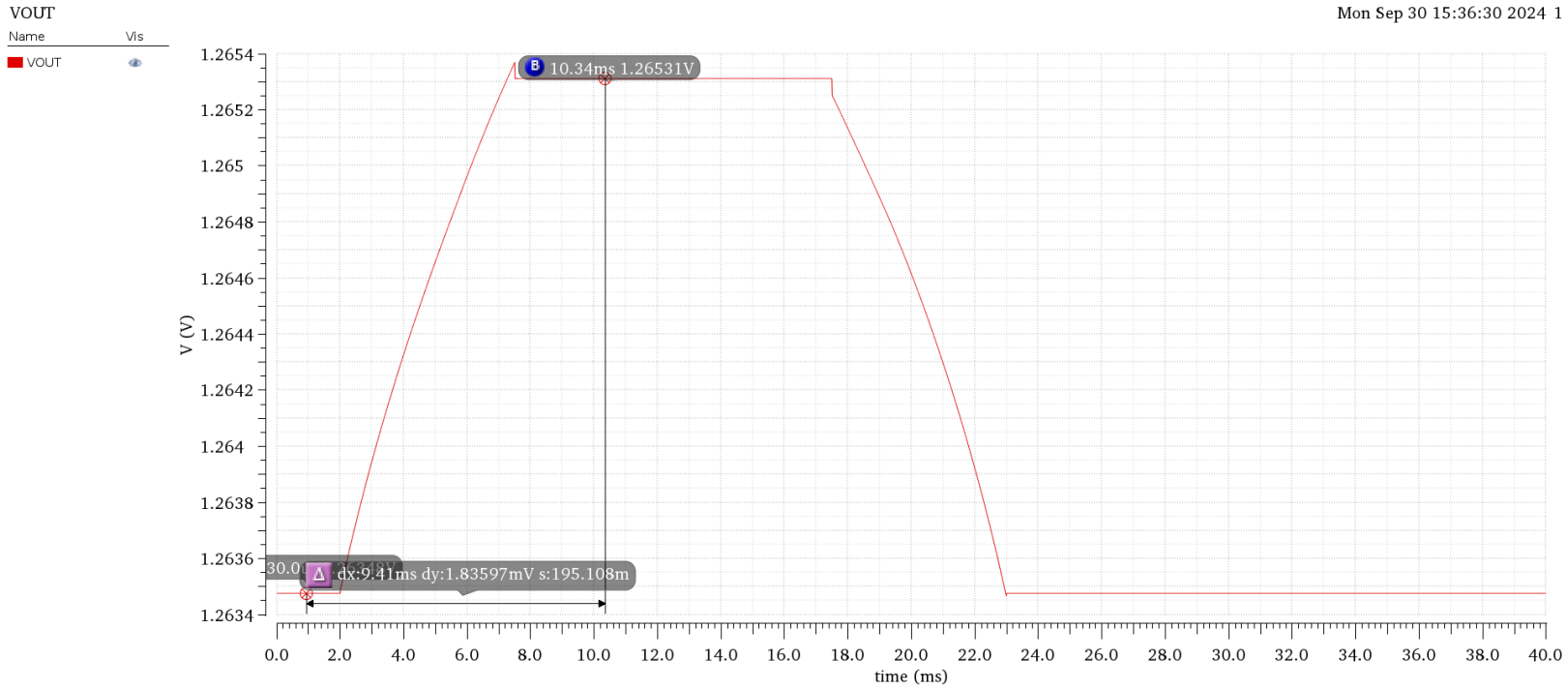
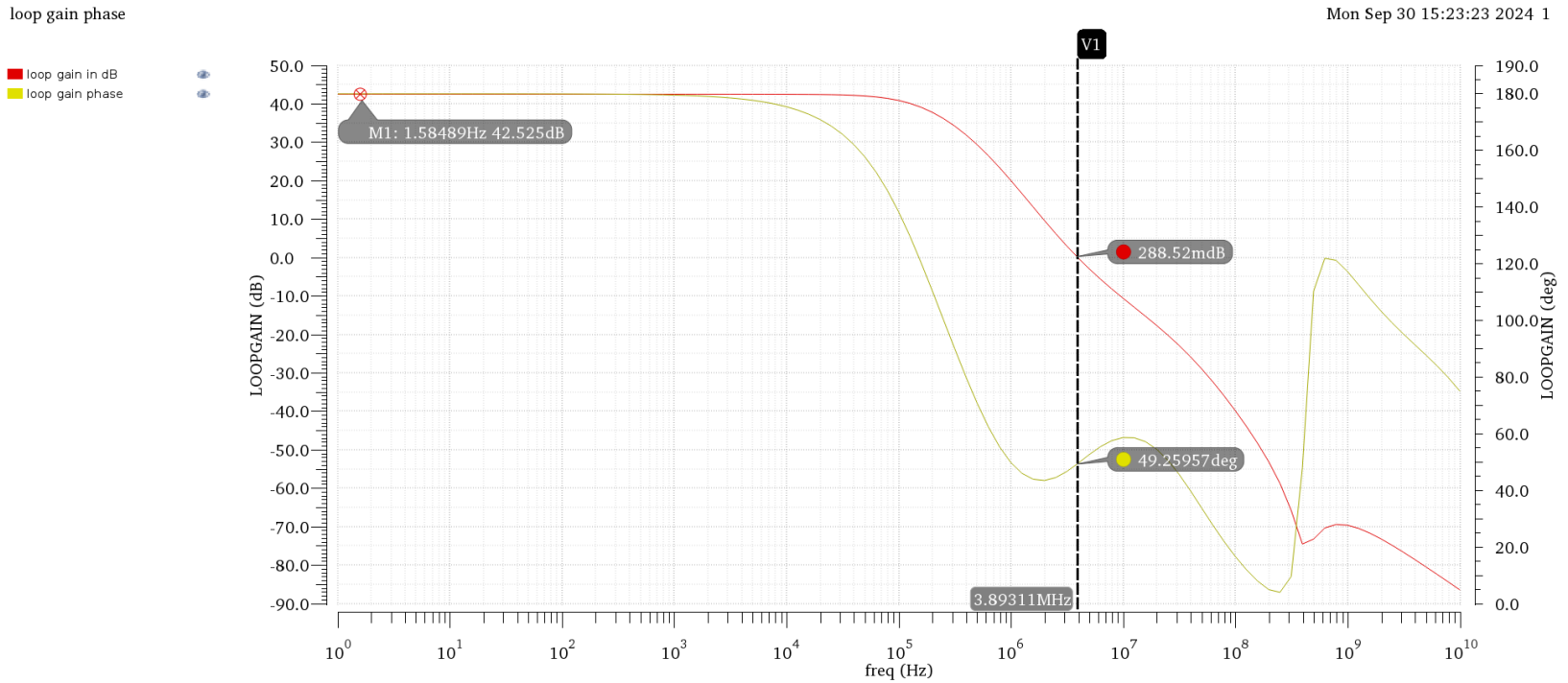
Transient Input Simulation

1. Line regulation



Stability Analysis and PSR

1. Phase Margin



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Stability Analysis and PSR

1. Phase Margin
2. PSR

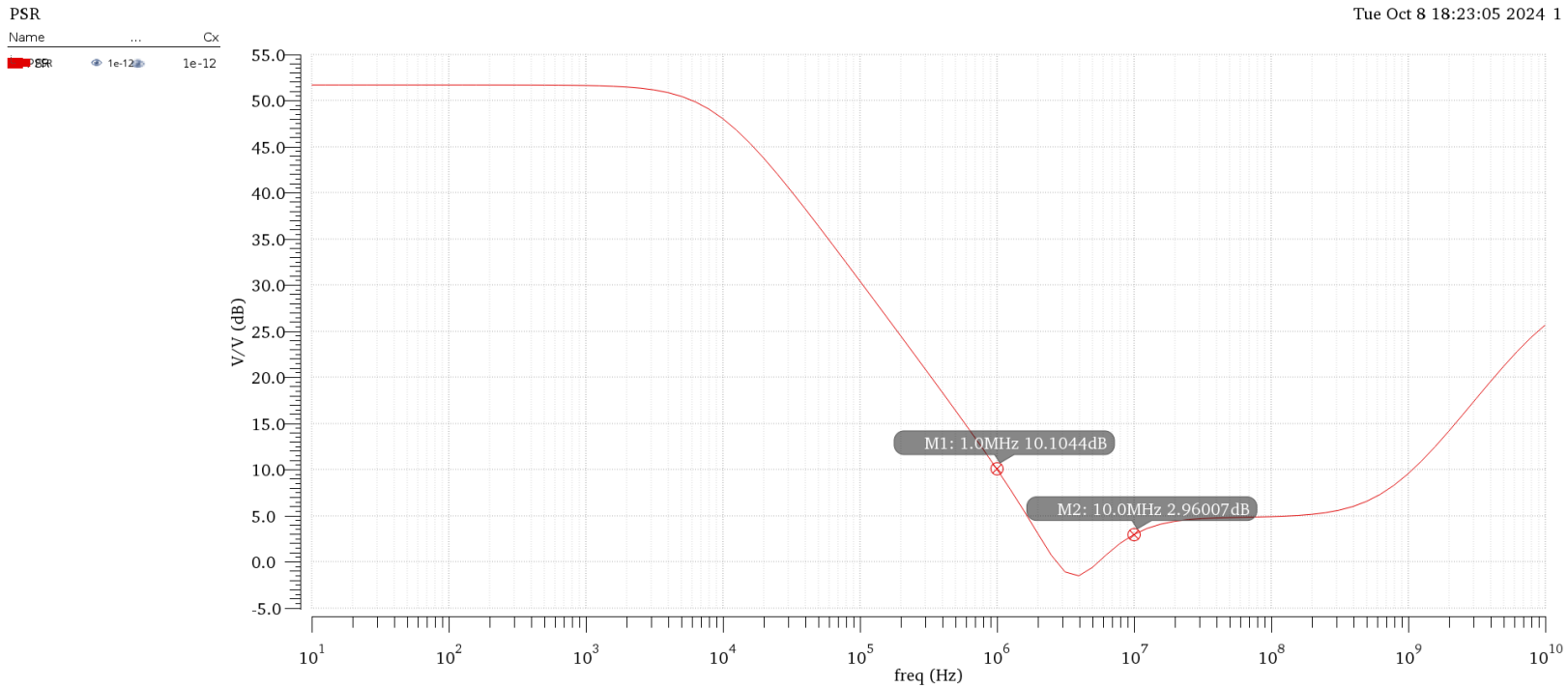

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Figure of Merit

$$FOM = \frac{C_L * \Delta V_{out} * I_Q}{I_{L,max}^2} = 2.16 * 10^{-6}\ (ns)$$

Achieved Specs

Spec	Required	Achieved
Technology used	$45nm\ CMOS$	
Supply Voltage	$2.4\ V \rightarrow 3.5\ V$	–
Output Voltage	$0.85\ V \rightarrow 1.25\ V$	–
Untrimmed output voltage accuracy	$< \pm 6\%$	1%
Load Current	$0.1\ mA \rightarrow 150\ mA$	–
Undershoot/Overshoot	$< 50\ mV$	$27\ mV$
Phase margin	$> 45^o$	49^o
Max Load Capacitance	$1\ nF$	–
Line Regulation	$< 2\ mV/V$	$1.7\ mV/V$
Load Regulation	$< 50\ mV/A$	$9\ mV/A$
Power Supply Rejection at 1 MHz	$30\ dB$	$10\ dB$
Power Supply Rejection at 10 MHz	$20\ dB$	$4\ dB$
FOM	–	$2.16 * 10^{-6}\ (ns)$

Design Challenges

1. **PSR**
   Bypass device length, low-pass filter and El-Nozahy's paper

2. **Load regulation**
   Magical mismatch effect

3. **Line regulation**
   Decrease the bypass current change

Thank You

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