وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

Ain Shams University – Faculty of Engineering – ECE Dept. – Integrated Circuits Lab.
Dr. Hesham Omran

Analog IC Design
Lab 11 (Mini Project 02)
Fully-Differential Folded Cascode OTA

Intended Learning Objectives

In this lab you will:

- Learn how to generate and use gm/ID design curves.
- Learn how to design a fully-differential folded-cascode OTA achieving given specifications.
- Learn how to simulate the open-loop characteristics of the fully-differential folded-cascode OTA.
- Learn how to simulate the closed-loop characteristics of the fully-differential folded-cascode OTA.
- Learn how to design the common-mode feedback circuit for the OTA.

PART 1: gm/ID Design Charts

Using ADT Sizing Assistant, plot the following design charts vs gm/ID for both PMOS and NMOS. Set VDS to a reasonable value and L = min,1u:1u:5u.

1) VA
2) W/ID
3) fT
4) VGS

PART 2: OTA Design

Design a fully-differential folded cascode OTA with capacitive feedback that meets the specifications below.

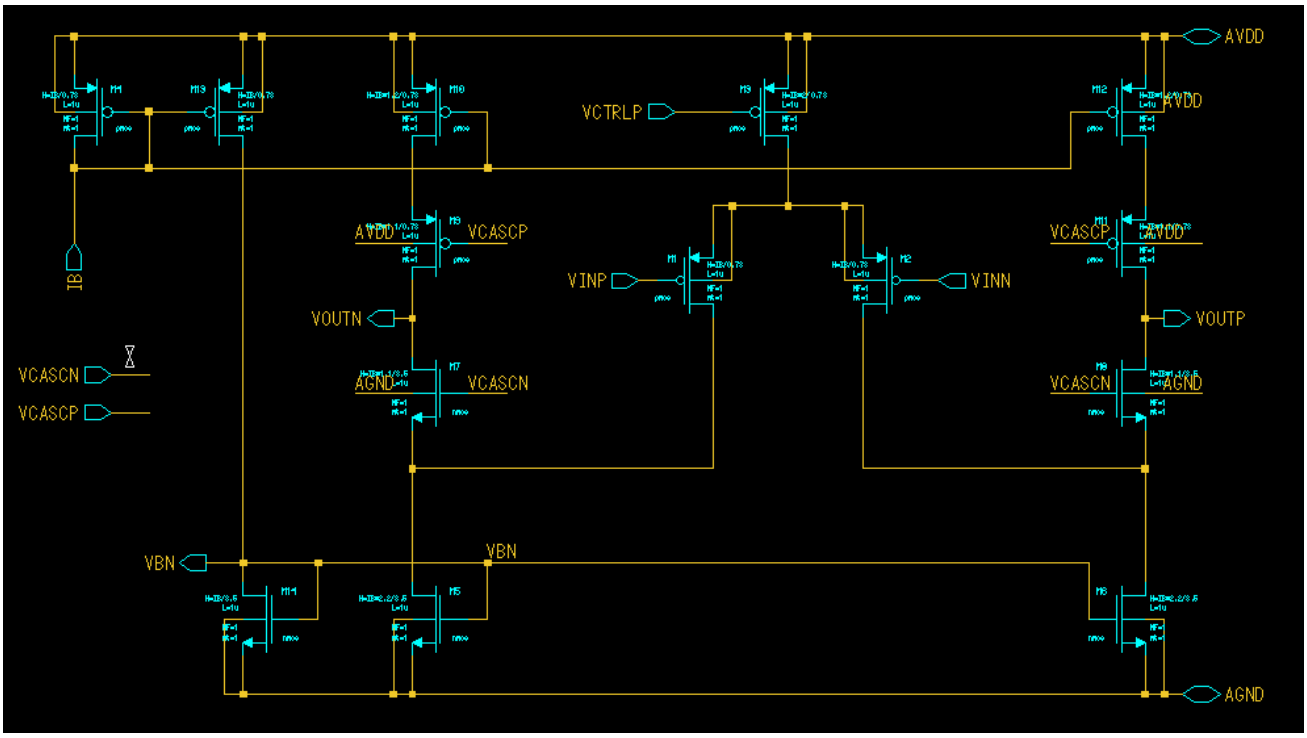
The current consumed in the biasing branches (current mirrors) is not included in the specifications.

Technology	0.13um	GF180MCU
Supply voltage	1.2V	2.5V
Closed loop gain	2	2
Phase margin at the required ACL	>= 70°	>= 70°
CM input range – low	<= 0	<= 0
CM input range – high	>= 0.6V	>= 1V
Differential output swing	0.6Vpk-to-pk	1.2Vpk-to-pk
Load	500fF	500fF
DC Loop gain	50dB	60dB

CL settling time for 1% error	**100ns**	**100ns**

Note: The power consumption and the total area should be reasonable.

Note: The DC loop gain and closed loop bandwidth specs may be difficult to include (precisely) in the initial hand analysis. After following the suggested design procedure, you may tune the circuit on the simulator (while taking trade-offs into account) to achieve these specs.



You can use the following ideal sources in your testbench:

- A single 10uA DC current source
- A DC voltage source for VDD
- Two DC voltage sources for biasing the cascode transistors (VCASCP and VCASCN)
- A DC voltage source for the CM output level (VREF)

➔ Suggested Design Procedure:

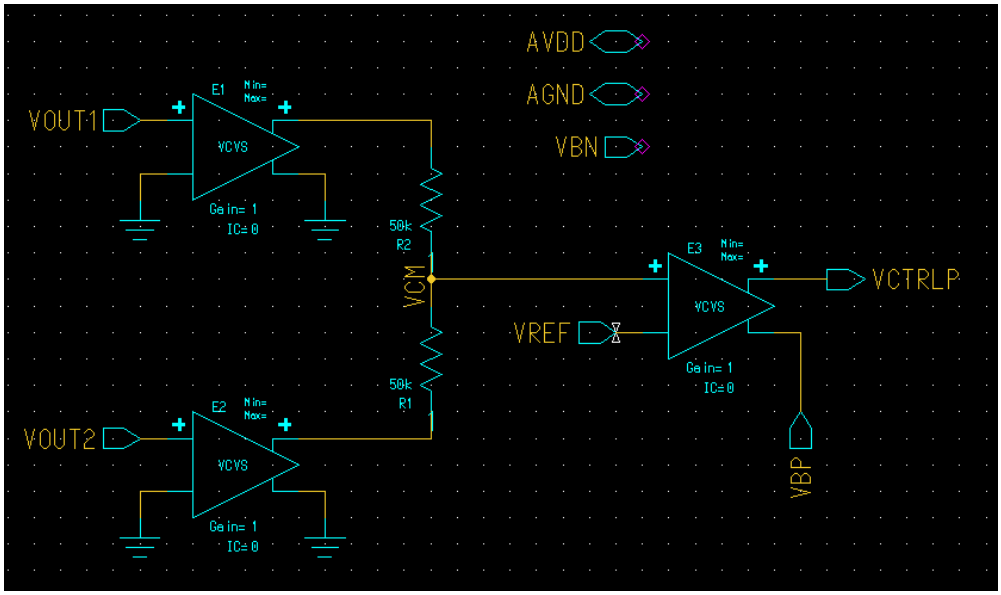
1) From the CMIR spec you will find that you need a PMOS input stage as shown in the schematic above.
2) Since this is a relatively difficult design, you will directly assume values for L and gm/ID (or V*) based on your designer's intuition and folded cascode trade-offs matrix.
   - For the input pair use short L and bias it in MI or WI. This maximizes the GBW (good efficiency) and minimizes the input capacitive loading (avoid reducing the DC LG). You will have to tune your gm/ID to achieve the CL bandwidth spec.
   - For the current source transistors use relatively long L and bias them in SI, e.g., L = 1um and gm/ID = 10. These transistors contribute significant offset and noise. A large gm will not help the gain but will increase the offset and noise.

- For the cascode transistors use moderate L and bias them in MI or WI, e.g., L = 0.5um and gm/ID = 15. These transistors do not contribute significant offset and noise, so they don't need to be large. A large gm helps the gain and doesn't increase the noise.
- These assumptions greatly simplify the design process and can be later tuned in simulations (taking the trade-offs matrix into consideration) to achieve exact specifications.

3) Convert the settling time spec to a spec on the closed-loop bandwidth (assume first-order system for simplicity).
4) From the closed loop bandwidth spec, calculate a reasonable bias current. The OTA current will be divided equally for the input pair (CS) and the cascode branches (CG). The NMOS current sources in the bottom needs to sink double the current[1].
5) From the assumed L and gm/ID (V*), use the charts to find the sizing (W) of all transistors.
6) From the assumed V*, select suitable biasing for the cascode transistors (VCASCP and VCASCN).
   Hint: Set VCASCN ≈ VGSN + V* and VCASCP ≈ VDD - |VGSP| - V*

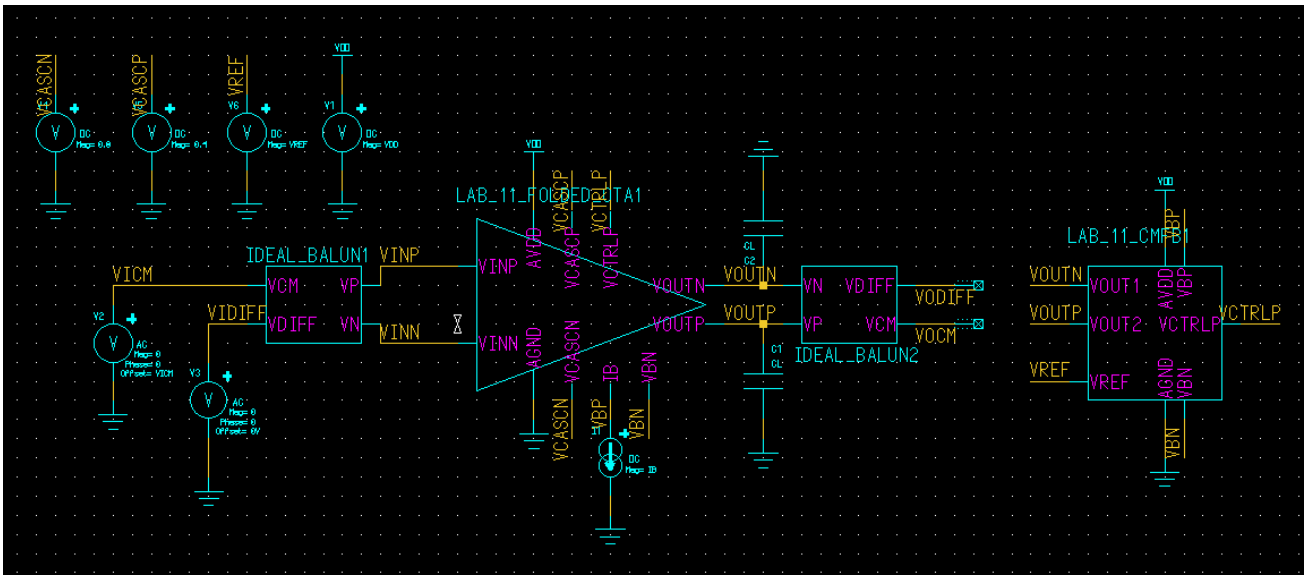
PART 3: Open-Loop OTA Simulation (Behavioral CMFB)

We will start with a behavioral CMFB network similar to the one shown below. We use ideal buffers to avoid loading the OTA output with the CM sensing resistors. Note that we don't need high gain in the CMFB loop (why?); thus, we use a gain = 1 in the error amplifier. We use dummy pins in the behavioral CMFB circuit to be "pin-accurate" with the actual CMFB circuit we will use later.



Create a testbench similar to the one shown below.

[1] For more details on how to select the folded cascode current split check this paper: "Optimum Split Ratio for Folded Cascode OTA Bias Current: A Qualitative and Quantitative Study" DOI: 10.1109/ICM48031.2019.9021755.



Report the following:

1) Schematic of the OTA and bias circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.
   - Set VICM at the middle of the CMIR.
   - Select VREF to maximize the symmetrical output swing.
   - What is the CM level at the OTA output?
   - What are the differential input and output voltages of the error amplifier? What is the relation between them?
2) Diff small signal ccs:
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Set VICM at the middle of the CMIR.
   - Plot diff gain (magnitude in dB and phase) vs frequency.
   - Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

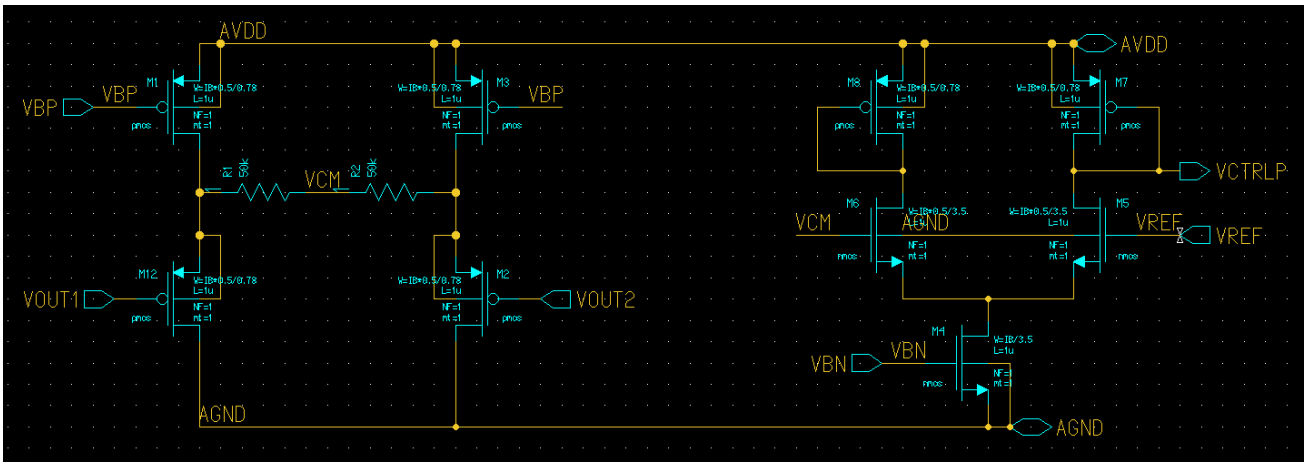
➔ Cadence Hint: Use Cadence calculator expressions to calculate circuit parameters (Ao, Ao in dB, BW, GBW, UGF). You may use Cadence calculator to create other useful expressions.

Name	Type	Expression/Signal/File
Ao	expr	ymax(mag(VF("/VOUT")))
Ao_dB	expr	dB20(ymax(mag(VF("/VOUT"))))
BW	expr	bandwidth(VF("/VOUT") 3 "low")
fu	expr	unityGainFreq(VF("/VOUT"))
GBW	expr	(Ao * BW)

   - Compare simulation results with hand calculations in a table (use SS parameters from OP simulation in your hand analysis).

PART 4: Open-Loop OTA Simulation (Actual CMFB)

Inside the CMFB cell, create a new schematic view for the actual CMFB circuit as shown below.



Note the following in the CMFB circuit design:

- Assume a reasonable CMFB current budget, e.g., 50% of the amplifier current.
- You may assume L = 1um and gm/ID = 15 for all transistors with unknown L or gm/ID for simplicity (note that L and gm/ID for some transistors are already known, why?).
- We need CD (source followers) to buffer the OTA output. This avoids loading the OTA with the sensing resistors[2].
- The sensing resistors are chosen such that the max current flowing through them (when diff signal is max) is less than the CD bias current. This avoids starving the CD when the diff output signal has its maximum excursion.
- The CD introduces DC shift. Thus, the input to the error amplifier is not Vocm. Instead, it is Vocm + |VGSP|. Thus, you need to set VREF to VREF + |VGSP|. The correct approach is to apply VREF to an identical CD buffer, so that it experiences the same |VGSP| shift.
- The CMFB limits the output swing. Max Vout is VDD – V* – |VGSP|. One reason why we selected PMOS CD is to avoid increasing VTH by body effect (increasing VTH will limit output swing even more).
- The output range now is from 2V* to VDD – V* – |VGSP|. Select Vocm to be around the middle of this range to have maximum symmetric output swing (it will be different from the value selected in the behavioral model).
- The output of the CD buffer is close to VDD; thus, we select NMOS input for the error amplifier.
- The error amplifier is a simple differential amplifier with diode connected loads. We don't need high gain from the error amplifier, but we need low impedance nodes to avoid deteriorating the stability of the CMFB loop.
- The bias point output of the error amplifier is equal to VDD - |VGSP|. That's why we use the error amplifier output to control the PMOS current source in the folded OTA rather than the NMOS current source.

[2] Note that this type of CMFB will have a limited linear range and may affect the output swing specification.

- Note that we select the non-inverting error amplifier output to maintain -ve feedback in the CMFB loop.

Use hierarchy editor to change the model of the CMFB circuit to use the actual circuit instead of the behavioral one.

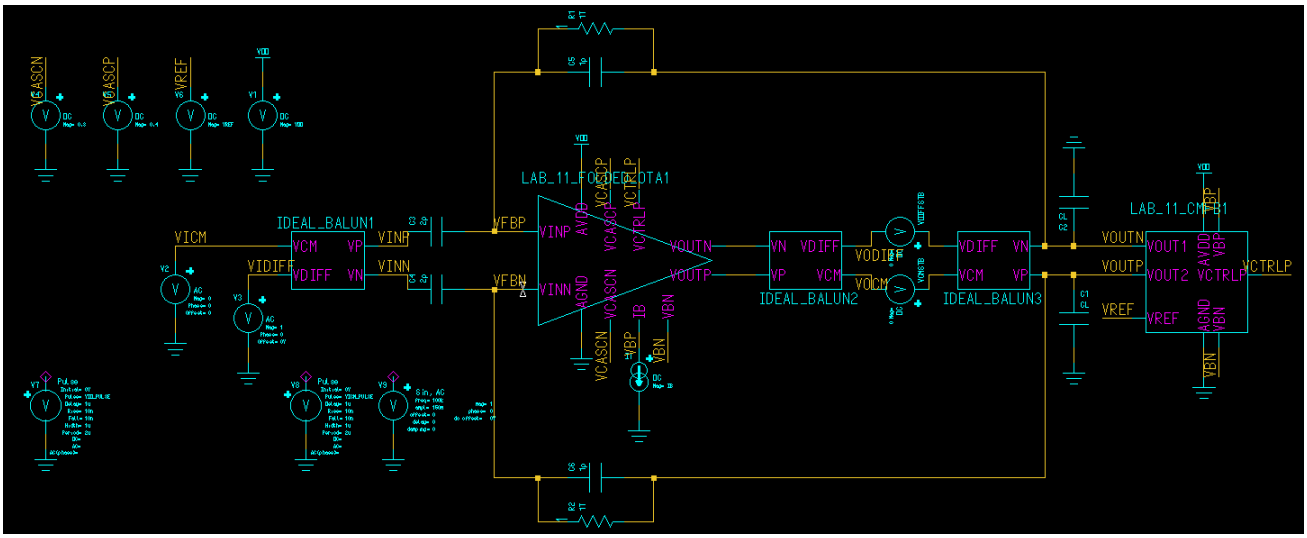
Report the following:

1) Schematic of the OTA and CMFB circuit with DC node voltages and transistors OP parameters (id, vgs, vds, vdsat, vth, gm, gds, region) clearly annotated.
   - Set VICM at the middle of the CMIR.
   - What is the CM level at the OTA output? Why?
   - What are the differential input and output voltages of the error amplifier? What is the relation between them?
2) Diff small signal ccs:
   - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
   - Set VIDAC = 1 and VICMAC = 0.
   - Set VICM at the middle of the CMIR.
   - Plot diff gain (magnitude in dB and phase) vs frequency.
   - Calculate circuit parameters (DC gain, BW, GBW, UGF, and PM).

PART 5: Closed Loop Simulation (AC and STB Analysis)

Create a new testbench with the OTA connected in closed-loop feedback configuration using capacitive feedback as shown below. Note that the CM DC level provided before the input balun is useless because it is blocked by the capacitor.

Note that we use two baluns at the output in order to allow stability analysis. We divide the output to diff and CM and break the diff/CM loops by 0V dc sources, then we combine them again to VOUTN and VOUTP to close the feedback loop. We use a 2pF input capacitance and 1pF feedback capacitance to provide a closed loop gain = 2. Note that you need to connect VOUTN to VINP and VOUTP to VINN to maintain negative feedback. We use large resistors across the feedback capacitance to close the loop in DC. This will set Vicm = Vocm.



➔ Cadence Hint: Instead of using two baluns at output, you can use diffstbprobe (or cmdmprobe in older versions) to simulate LG of differential and CM loops.

Report the following:

1) Schematic of the OTA and the CMFB circuit with DC OP point clearly annotated in closed-loop configuration.
    - What is the CM level at the OTA output? Why?
    - What is the CM level at the OTA input? Why?
2) Differential closed-loop response:
    - Use AC analysis (1Hz:10Gz, logarithmic, 10 points/decade).
    - Set VIDAC = 1 and VICMAC = 0.
    - Plot VODIFF vs frequency
    - Use Measures or cursors to calculate circuit parameters (DC gain, CL BW, CL GBW)
3) Differential and CMFB loops stability (STB analysis):
    - Run STB analysis (in addition to AC analysis 1Hz:10Gz, logarithmic, 10 points/decade) **<u>two times</u>**: first using the 0V source in the diff path, and second using the 0V source in the CM path.
    - Plot loop gain in dB and phase vs frequency for the two simulations overlaid.
    - Compare GBW and PM of diff and CM loops. Comment.
    - Compare DC LG and GBW of the diff loop with those obtained from open-loop simulation. Comment

PART 6: Closed Loop Simulation (Transient Analysis)

Use the same testbench as in Part 5, but change diff and CM input sources as explained below.

Report the following:

1) Differential and CMFB loops stability (transient analysis) + CL settling time: Differential input pulse

- Apply a differential input pulse (initial value = 0, pulse value = 100mV, delay = 1us, period = 2us, pulse width = 1us, rise = fall = 10ns).
- Run transient analysis for 3us with 10ns max step.
- Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.
- Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
- Calculate the 1% settling time and compare it to the required specification. If the specification is not satisfied, what design changes could be a possible solution?

2) Differential and CMFB loops stability (transient analysis): CM input pulse
   - Set differential input to zero and apply the same previous pulse at the balun CM input.
   - Run transient analysis for 3us to test the fully differential capacitive amplifier stability.
   - Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.
   - Do you notice any differential/CM ringing? Are both loops stable with adequate PM?
3) Output swing:
   - Apply a differential sinusoidal input with freq = 100kHz and amplitude = 150mV.
   - Run transient analysis for three periods (30us) with 0.1us max time step.
   - Plot the transient signals at VINP, VINN, VOUTP, VOUTN, and VOCM overlaid in the same figure.
   - Plot the transient signals at VIDIFF and VODIFF overlaid in the same figure.
   - Calculate the diff input and output peak-to-peak swings and the closed loop gain.

Lab Summary

- In Part 1 you learned:
  - How to generate and use gm/ID design curves.
- In Part 2 you learned:
  - How to design a fully-differential folded cascode OTA meeting desired specifications.
- In Part 3 you learned:
  - How to set the CM output voltage of a fully-differential OTA with an ideal CMFB circuit.
  - How to simulate the small-signal differential characteristics of a fully-differential folded cascode OTA in open-loop configuration with an ideal CMFB circuit.
- In Part 4 you learned:
  - How to design a CMFB circuit.
  - How to set the CM output voltage of a fully-differential OTA with an actual CMFB circuit.
  - How to simulate the small-signal differential characteristics of a fully-differential folded cascode OTA in open-loop configuration with a real CMFB circuit.
- In Part 5 you learned:
  - How to simulate the small-signal differential gain of a fully-differential folded cascode OTA in closed-loop configuration with a real CMFB circuit.
  - How to simulate the stability of both the main OTA loop and the CMFB loop of a fully-differential folded cascode OTA in closed-loop configuration.
- In Part 6 you learned:
  - How to simulate the stability of both the main OTA loop and the CMFB loop of a fully-differential folded cascode OTA using transient simulation.

- How to simulate the output swing of both the main OTA loop and the CMFB loop of a fully-differential folded cascode OTA using transient simulation.

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