Fully-Differential Folded Cascode OTA Design

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Part 1:OTA Design

Technology	$180\ nm\ CMOS$
Supply Voltage	$2.5\ V$
Closed loop gain	2
Phase margin at the required ACL	$\geq 70°$
CMIR - low	$\leq 0\ V$
CMIR - high	$\geq 1\ V$
Differential output swing	$1.2\ V_{pk2pk}$
Load	$500\ fF$
DC loop gain	$60\ dB$
CL settling time for 1% error	$100\ ns$

Table 1: Desired Specs

At first, we need to identify the topology.

Since the CMIR is near to GND, therefore the topology we will use in the Fully-Differential Folded Cascode OTA is PMOS for the CS stage and NMOS for the CG stage.

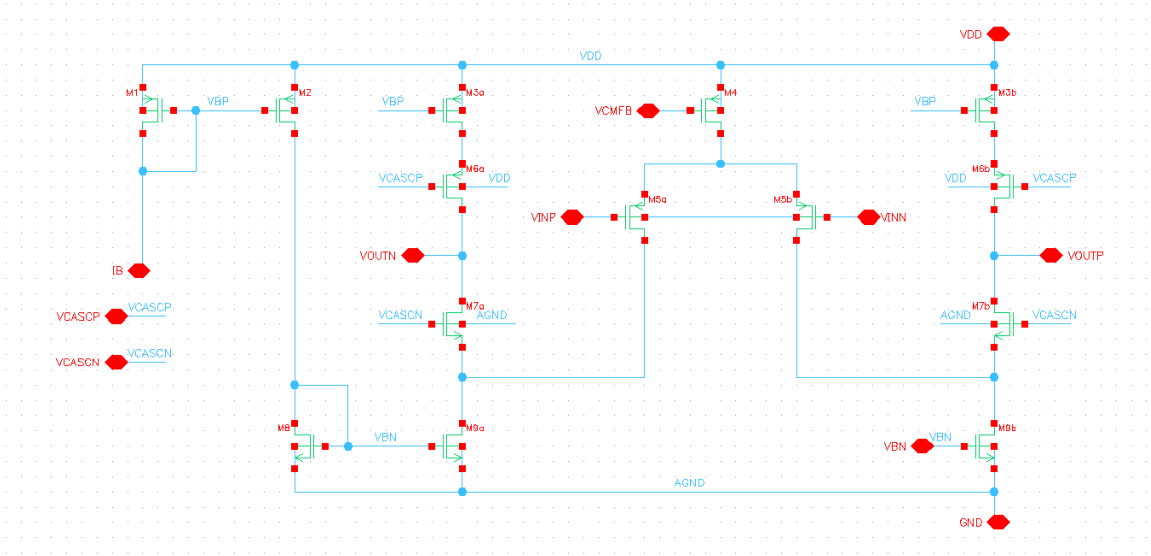

Figure 1: OTA schematic

1. OTA Initial Devices Sizing

Device	M_1	M_2	M_3	M_4	M_5	M_6	M_7	M_8	M_9
W	5 μm	981 nm	3.1 μm	11 μm	27.3 μm	2.8 μm	885 nm	711 nm	6.1 μm
L	500 nm	500 nm	500 nm	500 nm	420 nm	460 nm	520 nm	1.3 μm	1.3 μm
g_m	80 μS	16 μS	48 μS	176 μS	176 μS	48 μS	48 μS	16 μS	136 μS
I_D	10 μA	2 μA	6 μA	22 μA	11 μA	6 μA	6 μA	2 μA	17 μA
g_m/I_D	8	8	8	8	16	8	8	8	8
$\lvert V_{DSsat}\rvert$	214 mV	214 mV	214 mV	214 mV	110 mV	230 mV	219 mV	212 mV	212 mV
V_{ov}	211 mV	211 mV	211 mV	211 mV	45 mV	210 mV	195 mV	208 mV	208 mV
V^*	250 mV	250 mV	250 mV	250 mV	125 mV	250 mV	250 mV	250 mV	250 mV

Table 2: OTA initial devices sizing

$CMIR_{low} = 0.5 + V_5^* - |V_{GS5}| = -0.5\ V, CMIR_{high} = V_{DD} - V_4^* - |V_{GS5}| = 1.12\ V.$
$V_{out}\ upper\ limit = V_{DD} - 0.5 - V_6^* = 1.75\ V, lower\ limit = 0.5 + V_7^* = 0.75\ V.$

$. V_{cascp} = V_{DD} - |V_{GS6}| - 0.5 = 0.816\ V, V_{cascn} = V_{GS7} + 0.5 = 1.56\ V.$

2. OTA final design schematic

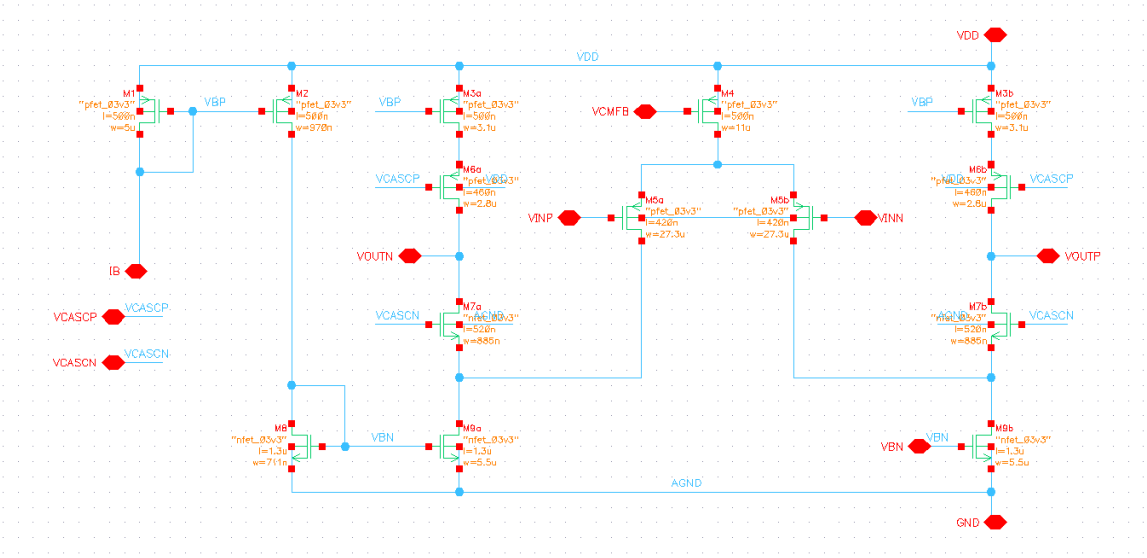

Figure 2: fully differential OTA final design schematic after tuning

The DC differential gain is much higher than desired due to body effect for $M_{6,7}$ and due to the difference between nmos/pmos and nfet/pfet models so we can save some area resources by decreasing the cascode devices lengths.

3. Resizing Cascode Devices (M_6&M_7)

For the PMOS cascode devices $(M_{6(a\&b)})$

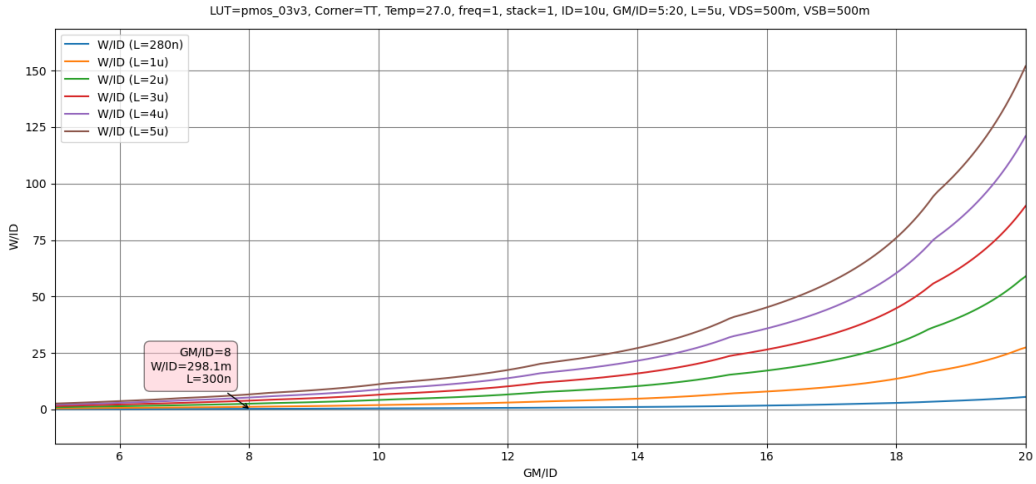

Figure 3: W/ID chart for M6

Keep same gm/ID and decrease L and get the corresponding W till the gain decreases enough, we got $L_6 = 300\ nm, W_6 = 1.8\ \mu m$.

And do the same for the NMOS cascode devices $\left(M_{7(a\&b)}\right)$ till we get the wanted gain (about 3.1 K)

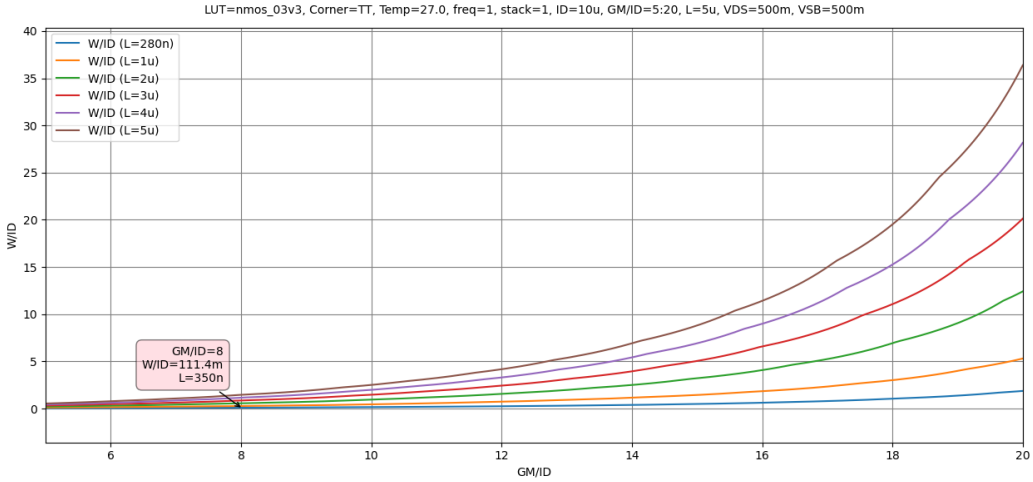

Figure 4: W/ID chart for M7

$L_7 = 350\ nm, W_7 = 670\ nm.$

4. Biasing Circuits Design $(V_{cascn} \& V_{cascp})$

Now we will design the biasing circuits for V_{cascn} and V_{cascp}.
For both circuits we will use two stack devices so the cascode one works in sat and we will make it matched to the cascode device in the targeted circuit, we will only size the 2nd device. For these devices we will have $V_{SB} = 0, |V_{DS}| = 0.5\ V$ (the same V_{DS} wanted for the NMOS/PMOS current mirrors).

For the NMOS device (M_{18}):

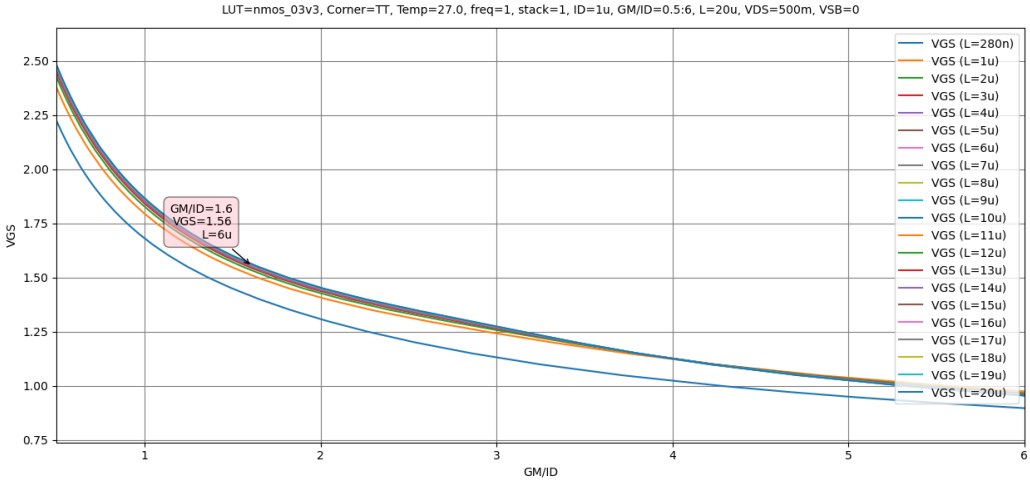

Figure 5: VGS chart for M18

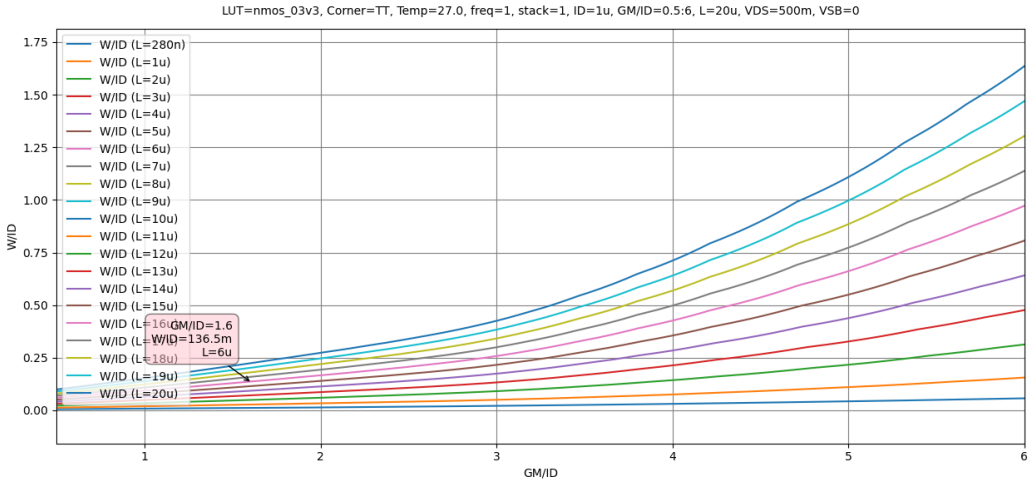

Figure 6: W/ID chart for M18

We will use a current of 2 μA to get a usable width $L_{18} = 6\ \mu m, W_{18} = 273\ nm$.

For the PMOS device (M_{15}):

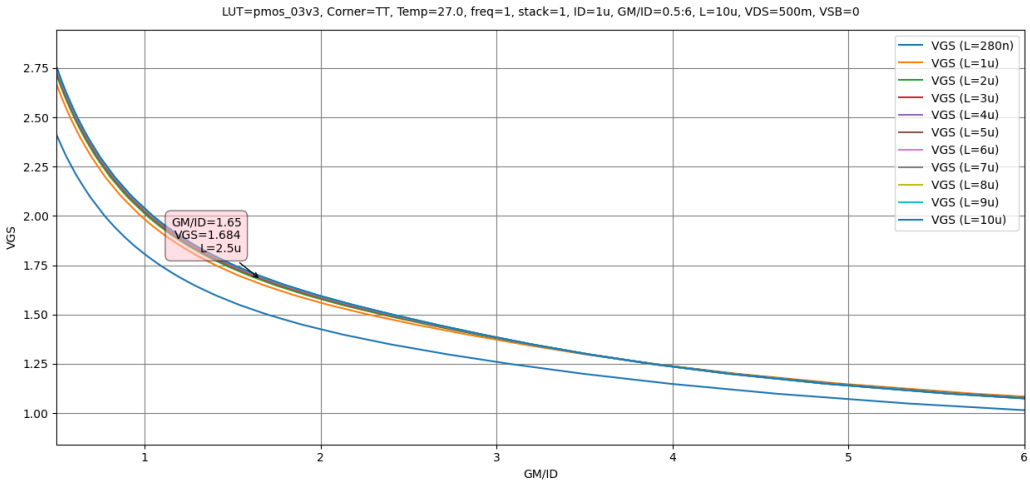

Figure 7: VGS chart for M15

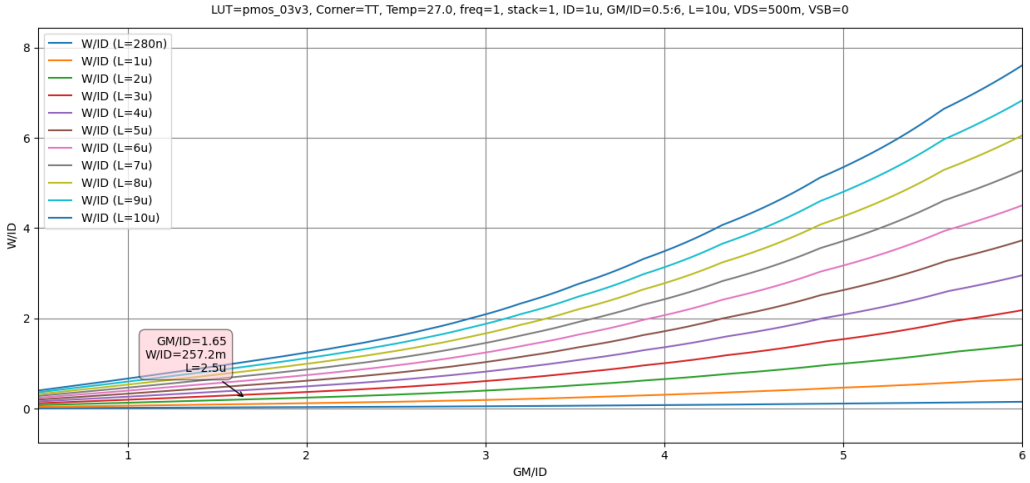

Figure 8: W/ID chart for M15

We will use a current of only 1 μA as it's enough to get a usable width in order to minimize the current consumption $L_{18} = 6\,\mu m, W_{18} = 273\,nm$.

So, after fine tuning we get the desired V_{cacsn} and V_{cascp}.

Part 2: Open-Loop OTA Simulation (Behavioral CMFB)

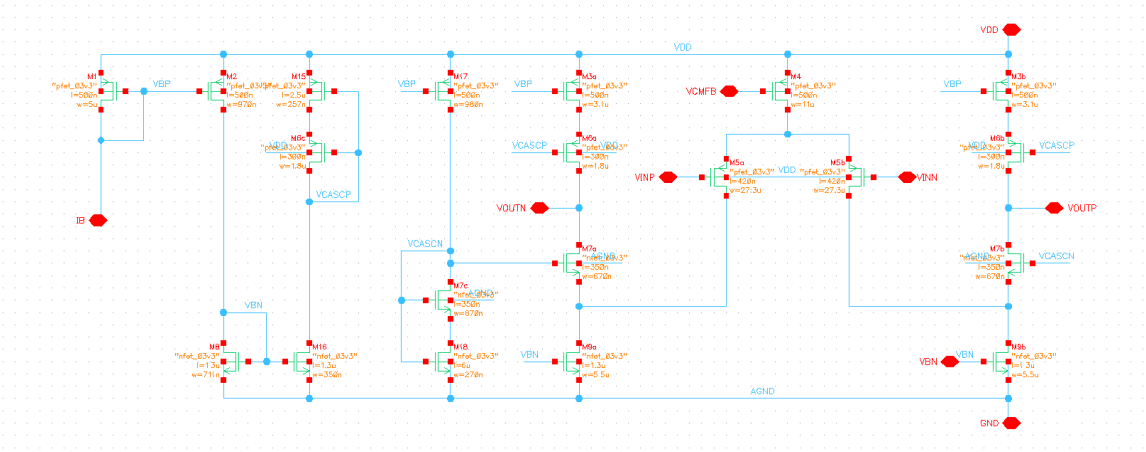

Figure 9: Final design schematic with biasing circuits.

1. OP Simulation

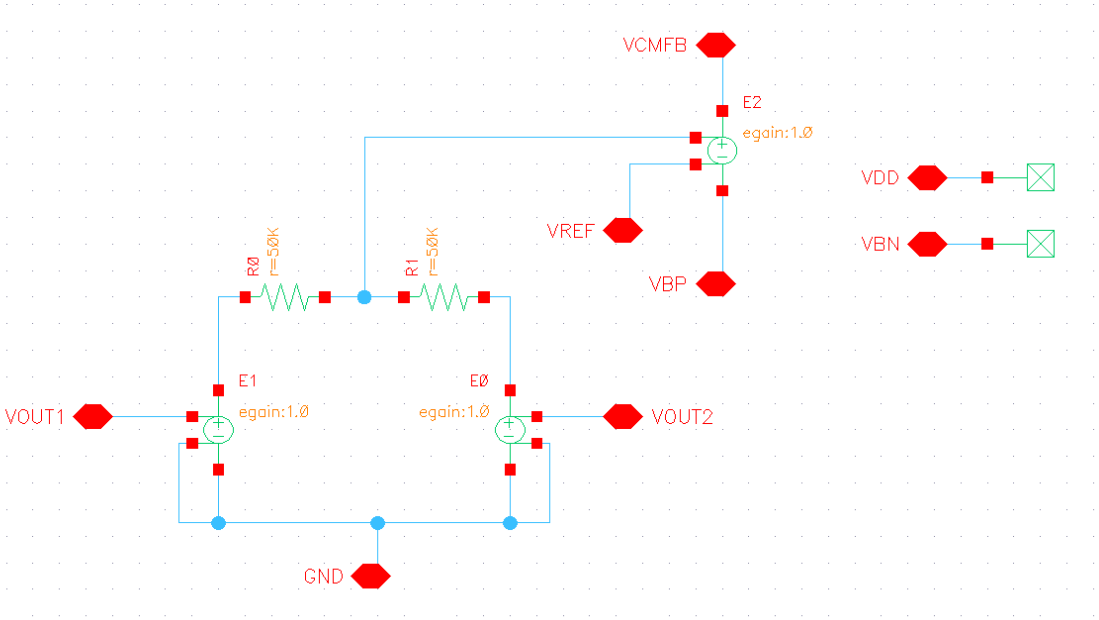

Figure 10: CMFB circuit behavioral model

- Set VICM to 0.5 V (half CMIR).
- Set VREF to 1.25 V as the output swing (single rail) is from 0.75 to 1.75 V.

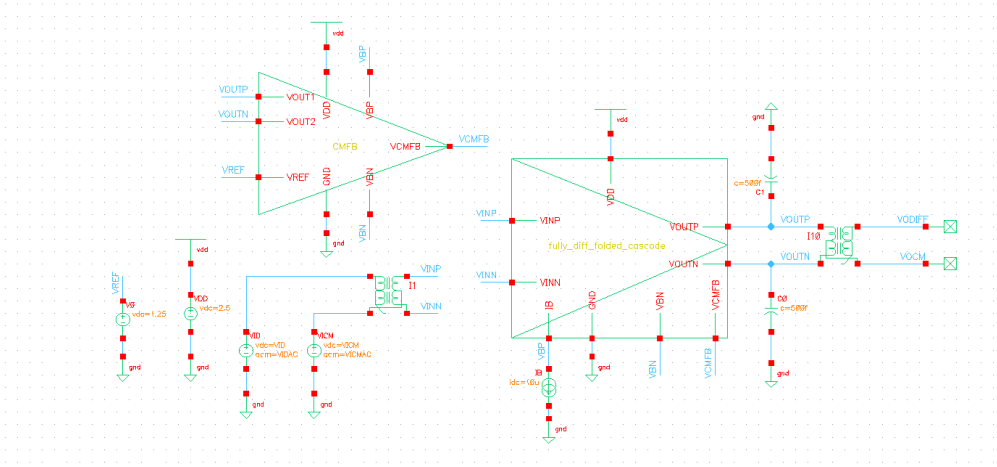

Figure 11: Open-loop testbench

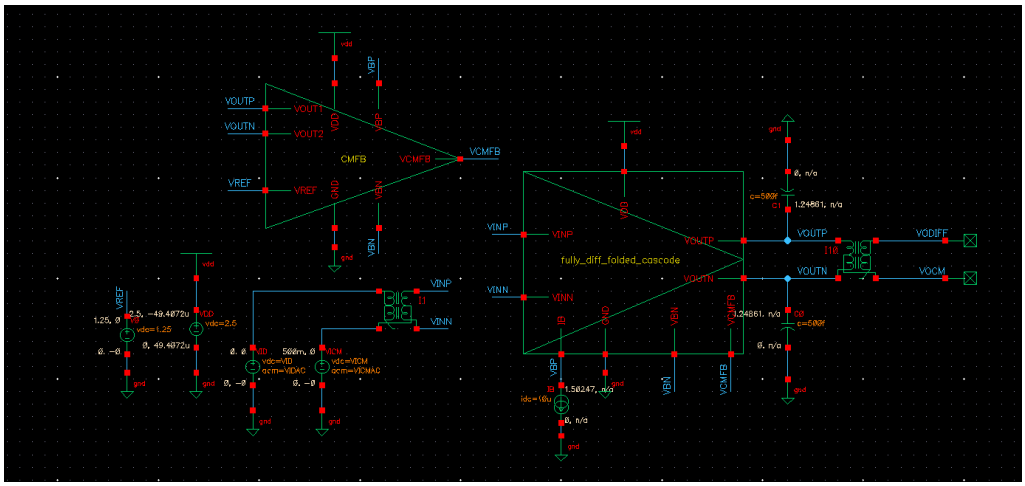

Figure 12: bias circuit with DC node voltages annotated

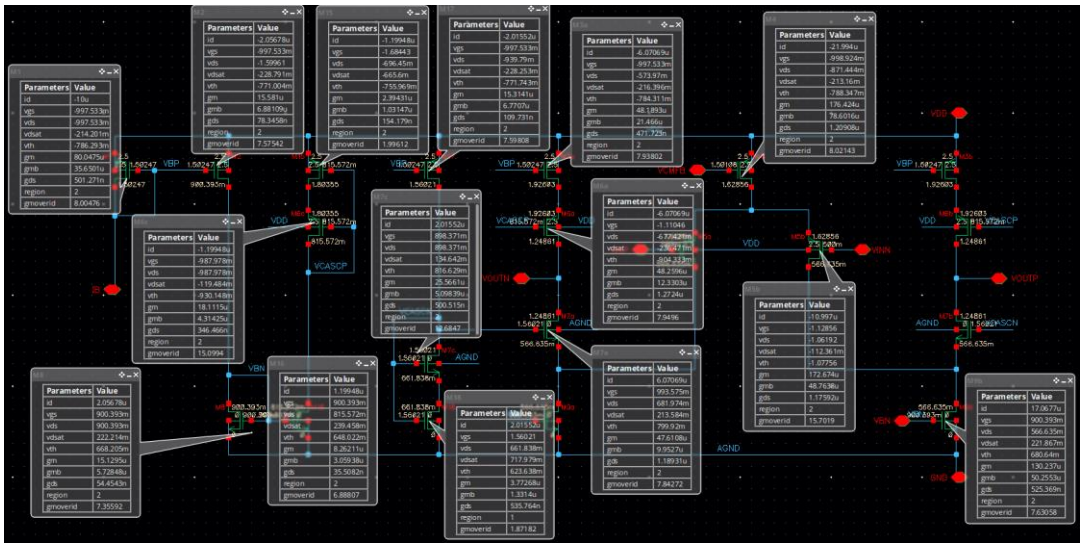

Figure 13: OTA schematic with DC node voltages and OP parameters annotated

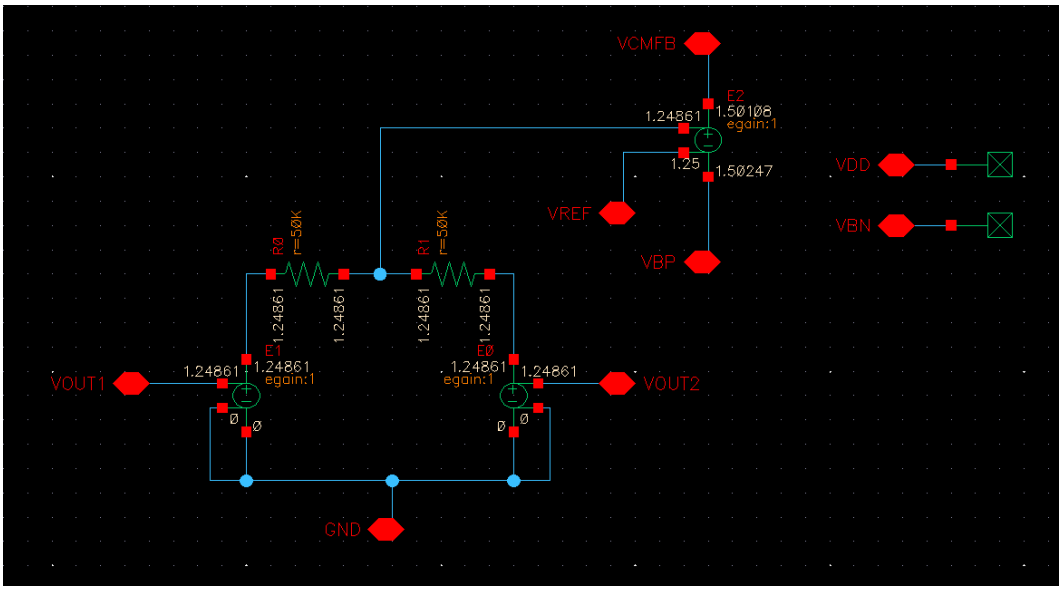

Figure 14: Behavioral CMFB schematic with DC node voltages annotated

- All devices are in sat except the non-degenerated devices in the biasing circuits.
- The output swing is from $0.75\ to\ 1.75\ V$ so we set V_{ref} to $1.25\ V$.
- The total current consumption in the fully differential OTA and current mirror branches is about $49.4\ \mu A$ ($34\ \mu A\ in\ the\ OTA$).
- If we check the branches currents we will find out that it's near from what we expected as we took VDS into consideration in the W/ID charts and done fine tuning.
- The current and gm in the input pair exactly equal, due to the absence of differential signal and dc offset and no mismatch between the devices.
- The dc level of V_{out} is $1.2486\ V$ as a result of the CMFB circuit which tends to minimize the error between the common mode dc level of V_{out} and V_{ref} and the error equals the reciprocal of the CMFB loop-gain.
- The differential input and output voltages of the error amplifier are $-1.4\ mV$ (the same) as the relation between them is the error amplifier gain which is 1.

2. Diff Small Signal CCS

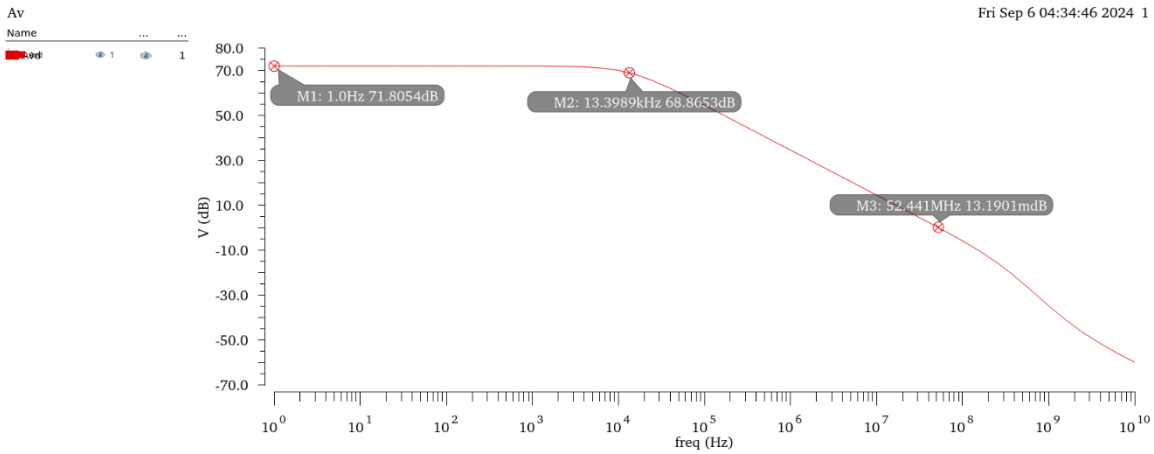

Figure 15: diff gain bode plot (magnitude)

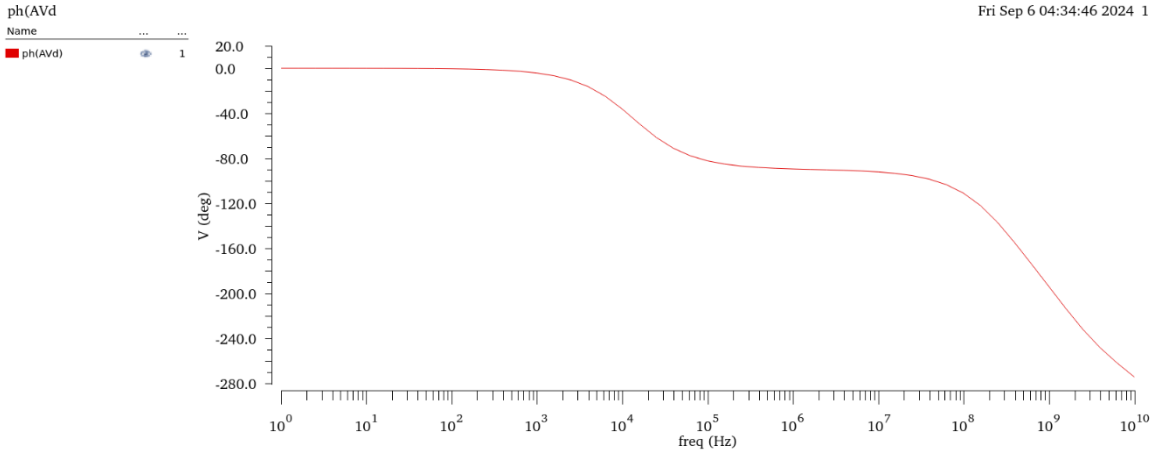

Figure 16: Differential gain bode plot (phase)

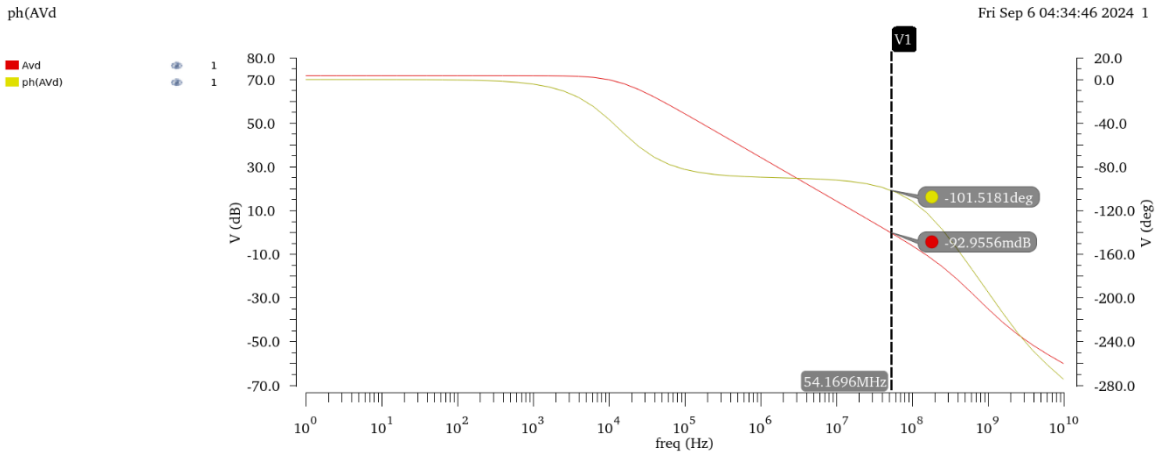

Figure 17: open-loop gain Gx

$PM \approx 180 - 102 = 78^o$

Test	Output	Nominal	Spec
ITI_labs:lab11_TB1:1	Avd @dc	3.893k	> 3.1k
ITI_labs:lab11_TB1:1	Avd @dc (dB)	71.81	> 70
ITI_labs:lab11_TB1:1	BW	13.73k	
ITI_labs:lab11_TB1:1	GBW	53.59M	> 34.3M
ITI_labs:lab11_TB1:1	UGF	54.94M	> 34.3M

Figure 18: diff small signal results

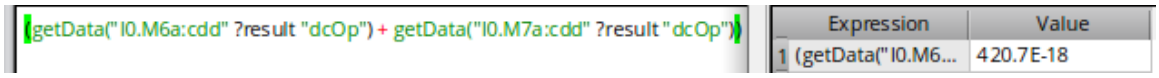

Figure 19: Cout_parasitics

$|DC\ diff\ gain| = g_{m5} * \left((g_{m6} + g_{mb6})r_{o6}r_{o3} \parallel (g_{m7} + g_{mb7})r_{o7}(r_{o5} \parallel r_{o9})\right)$

$BW \approx \frac{1}{2\pi\left((g_{m6}+g_{mb6})r_{o6}r_{o3} \parallel (g_{m7}+g_{mb7})r_{o7}(r_{o5} \parallel r_{o9})\right)C_L}$, $GBW = \frac{g_{m5}}{2\pi C_L}$ (parasitics are too small can be neglected)

Spec	*Simulation*	*Hand analysis*
DC diff gain	71.8 dB	71.7 dB
BW	13.73 KHz	14.34 KHz
GBW	53.6 MHz	54.96 MHz
PM	78^o	89.5^o

Table 3: open-loop simulation vs hand analysis

- UGF and GBW are almost the same and that's an indicator to the good PM.
- BW & GBW hand analysis are different from the simulation as the parasitic caps values are not accurate (I think).

Part 3: CMFB Circuit Design

- The topology selection will depend on the CM controlled by the CMFB circuit, which is the PMOS tail CM so we need the CM load of the error amplifier to be PMOS too, the CD stage is defined to be a PMOS CD stage as the OTA input stage will be NMOS so we need to shift the V_{out} value up so that the CMIR of the error amplifier is matched.
- Let the current budget for CMFB circuit be 17 μA (half differential OTA budget) so let it be 5 μA in each branch - to increase the current capability in the source follower stage - except the error amp $I_{ss} = 2\ \mu A$ is enough.
- The sizing steps are simple not as strict as the OTA because the CMFB loop-gain not necessarily high so we will design with simple steps and make fine tuning in order to get a good design.

1. Actual CMFB Schematic

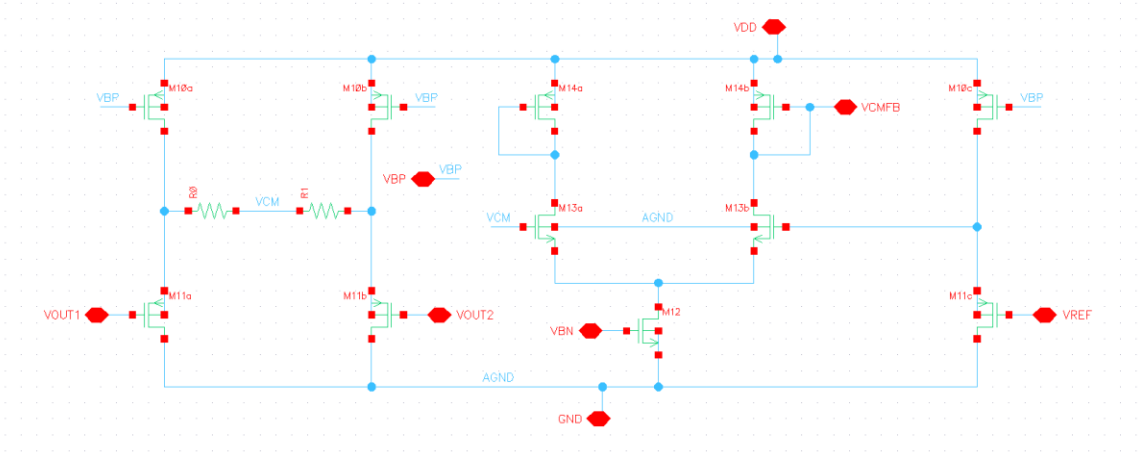

Figure 20: Actual CMFB schematic

2. PMOS Current Mirror $\left(M_{10(a,b\&c)}\right)$

We will use the same sizing as M1 with half its width and it can be tuned a little bit later. $L_{10} = 500\ nm, W_{10} = 2.5\ \mu m$. Note that $V_{10}^{*} = V_{1}^{*} = 250\ mV$ as we will need it in the max V_{outCM} value calculations.

3. PMOS Input Devices $\left(M_{11(a,b\&c)}\right)$

Let VDS=0.9 V as a good initial guess then later we will make fine tuning if necessary.
We need max output swing in one rail to be $> \frac{1.2}{2} = 0.6\ V$, $V_{outmin} = 0.75\ V$ as calculated before so we need $V_{outmax} \geq V_{outmin} + 0.6 = 1.35\ V, V_{outmax} = V_{DD} - V_{10}^{*} - |V_{GS11}|$ so we need $|V_{GS11}| \leq 900\ mV$

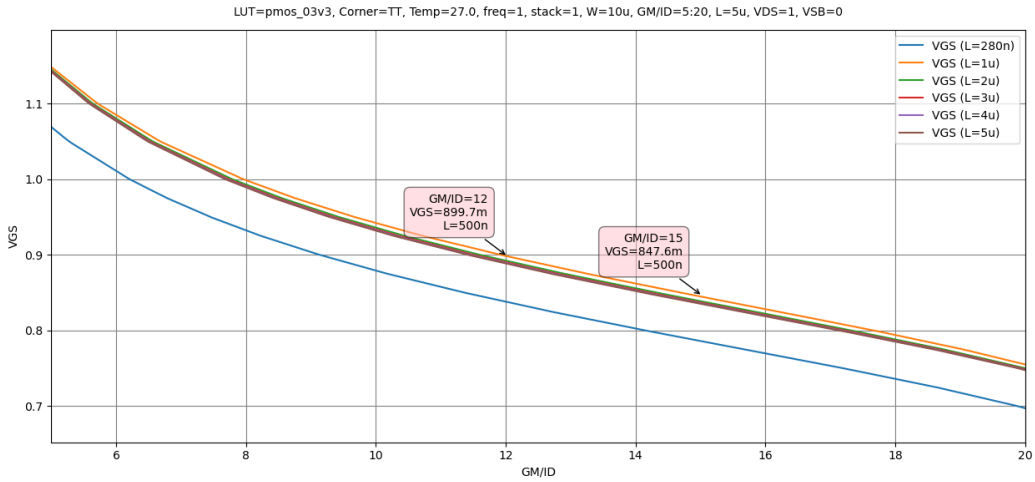

Figure 21: VGS chart for M11

We need $\left(\frac{g_m}{I_D}\right)_{11} \geq 12$.

In order to increase linearity and get better buffer gain we should trigger $V_{A11} \geq V_{A10}$ and high $\left(\frac{g_m}{I_D}\right)_{11}$ As $A_v = \frac{g_{m11}(r_{o10} \| r_{o11})}{1+g_{m11}(r_{o10} \| r_{o11})} = \frac{\left(\frac{g_m}{I_D}\right)_{11}(V_{A10} \| V_{A11})}{1+\left(\frac{g_m}{I_D}\right)_{11}(V_{A10} \| V_{A11})}$.

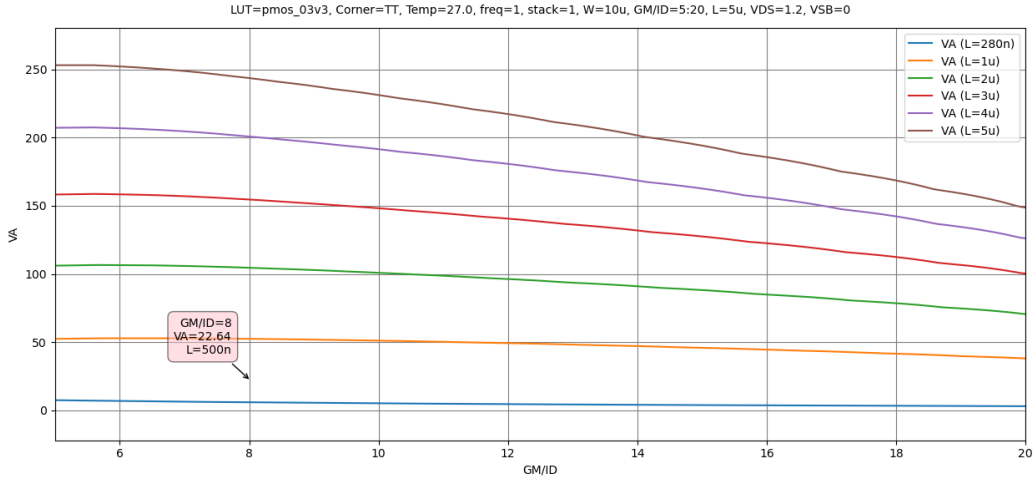

Figure 22: VA chart for M10

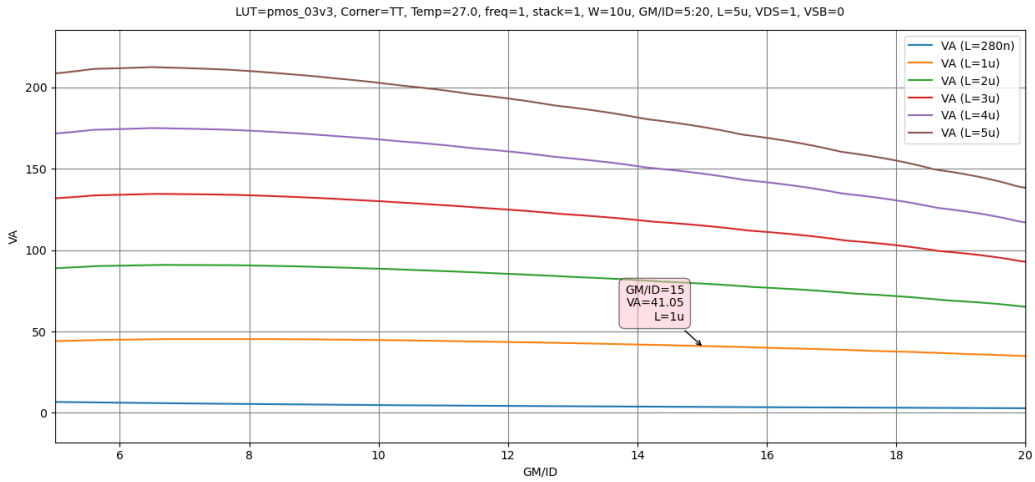

Figure 23: VA chart for M11

so let $\left(\frac{g_m}{I_D}\right)_{11} = 15, L_{11} = 1\ \mu m$. So $|V_{GS11}| \approx 850\ mV$ so $V_{outmax} = 1.4\ V$.

Now get W from W/ID chart where $I_{D11} = 5\ \mu A$.

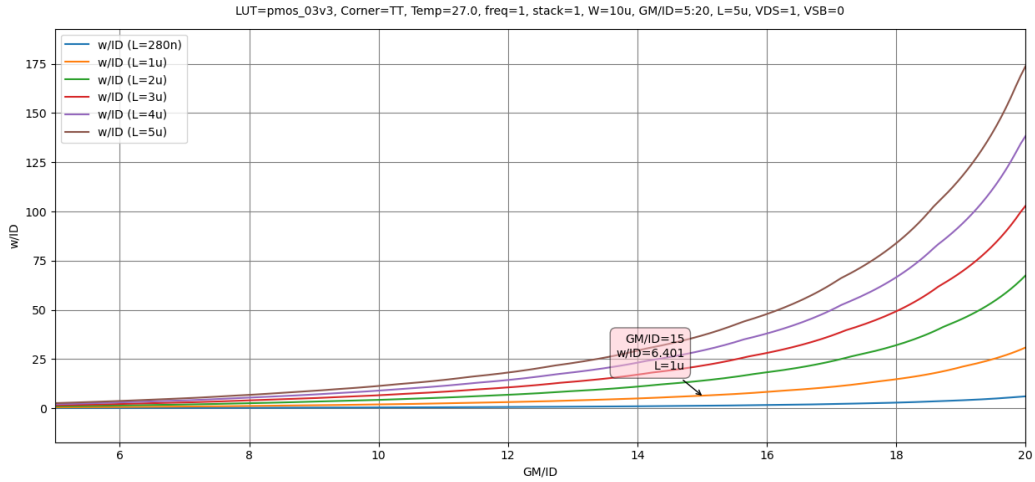

Figure 24: W/ID chart for M11

$W_{11} = 32\ \mu m$.

4. NMOS Current Mirror (M_{12})

We will use the same sizing as M8. its width can be tuned a little bit later.
$L_{12} = 1.3\ \mu m, W_{12} = 711\ nm$.

5. PMOS Error Amp Diode Connected Load $(M_{14(a\&b)})$

M_{11} is desired to be matched to M_4 to get a CMFB voltage near to the required V_{BP}. Then $\left(\frac{g_m}{I_D}\right)_{14} = 8$ and let $L_{14} = 500\ nm, V_{DS11} = V_{GS4} \approx 1\ V$. So now we can get initial value for W and tune it later if necessary.

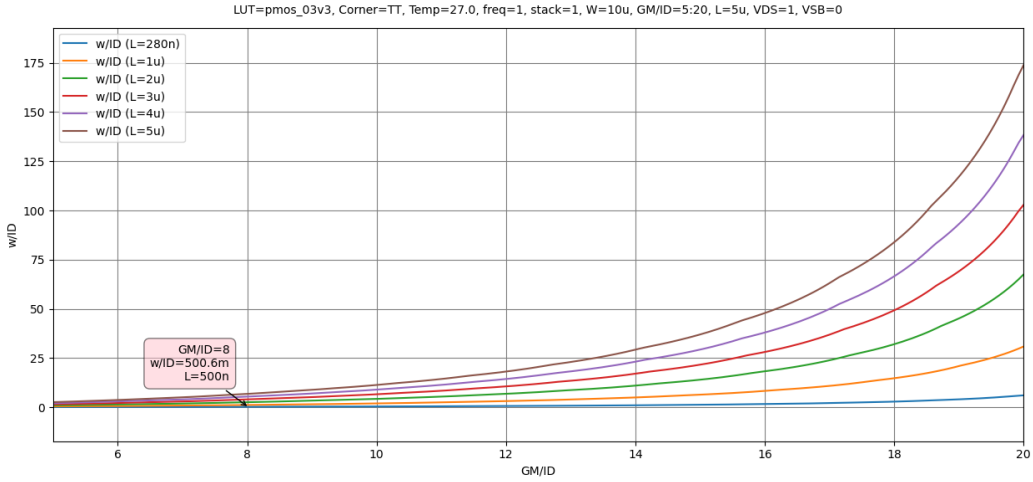

Figure 25: W/ID chart for M14

$W_{14} = 500\ nm$.

6. NMOS Error Amp Input Pair $(M_{13(a\&b)})$

Let $V_{DS13} = 0.5\ V$ as a good assumption.
In order to get the higher possible gain we need to bias M13 in MI with high gm/ID let it be 16 as minimum value to get error amp gain of about 2. $A_v \approx \frac{g_{m11}}{2g_{m14}}$ (note that the error amp gain is half the diff amp gain in order to avoid high impedance nodes which have bad effect on stability) and let $L_{13} = 1\ \mu m$. So now we can get initial value for W and tune it later if necessary.

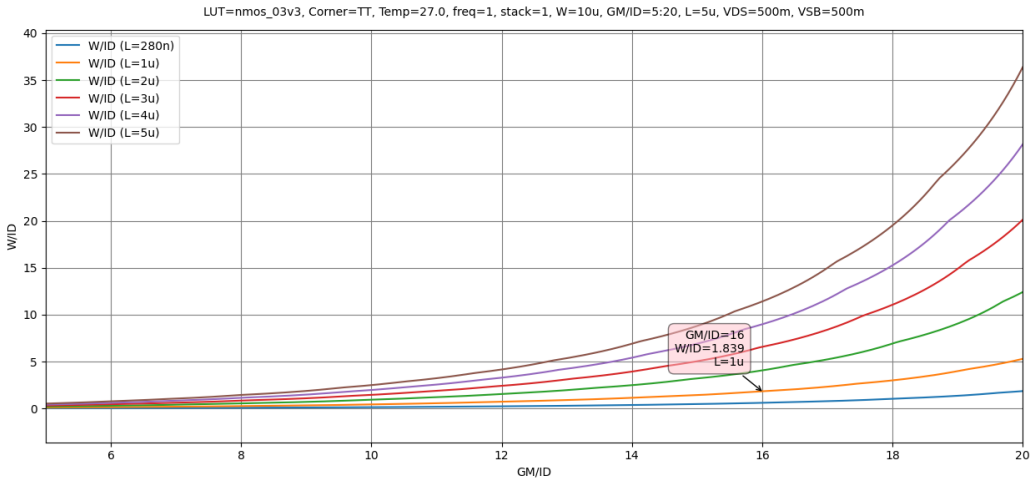

Figure 26: W/ID chart for M13

$W_{13} = 1.84\ \mu m.$

7. Resistive Network $(R_{o,1})$

We need the maximum current in the resistive network to be less than $5\ \mu A$ - where the max voltage drop on the two resistors is $1.4 - 0.75 = 0.65\ V$ - let it be about $2.5\ \mu A$ $(50\%\ of\ I_{D10})$ in order to enhance linearity so we need $\frac{0.65}{2R} \leq 2.5\ \mu A\ so\ R \geq 130\ K\Omega$. Let $R = 130\ K\Omega$.

8. CMFB initial Devices Sizing

Device	M_{10}	M_{11}	M_{12}	M_{13}	M_{14}
W	$2.5\ \mu m$	$32\ \mu m$	$711\ nm$	$1.84\ \mu m$	$500\ nm$
L	$500\ nm$	$1\ \mu m$	$1.3\ \mu m$	$1\ \mu m$	$500\ nm$
g_m	$40\ \mu S$	$75\ \mu S$	$14.8\ \mu S$	$16\ \mu S$	$8\ \mu S$
I_D	$5\ \mu A$	$5\ \mu A$	$2\ \mu A$	$1\ \mu A$	$1\ \mu A$
g_m/I_D	8	15	7.4	16	8

Table 4: CMFB initial devices sizing

9. CMFB Final Design Schematic

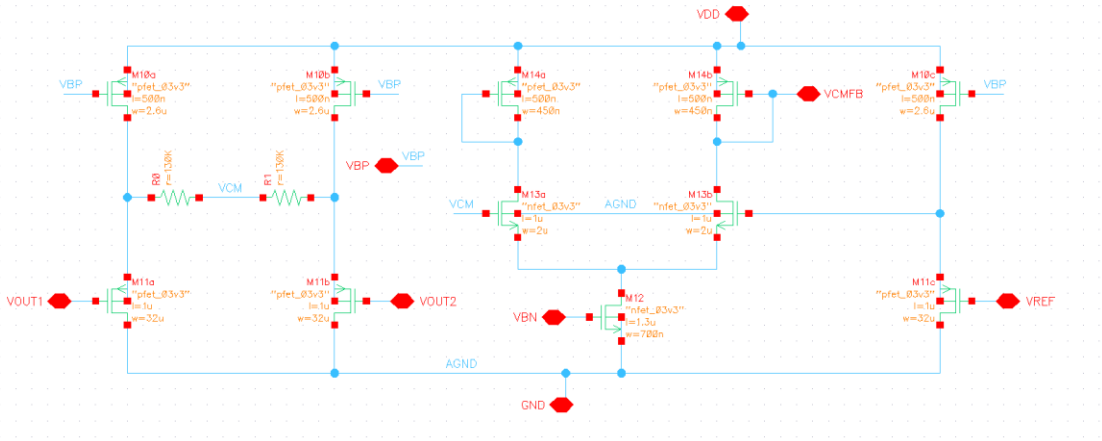

Figure 27: CMFB final design schematic after tuning

Part 4: Open-Loop OTA Simulation (Actual CMFB)

1. OP simulation

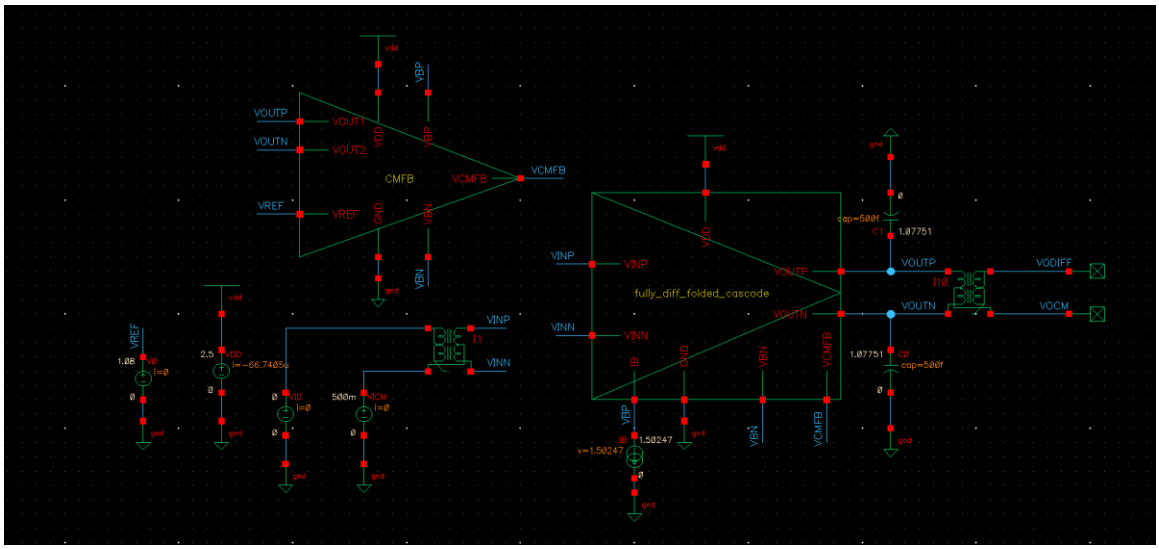

Figure 28: bias circuit with DC node voltages annotated

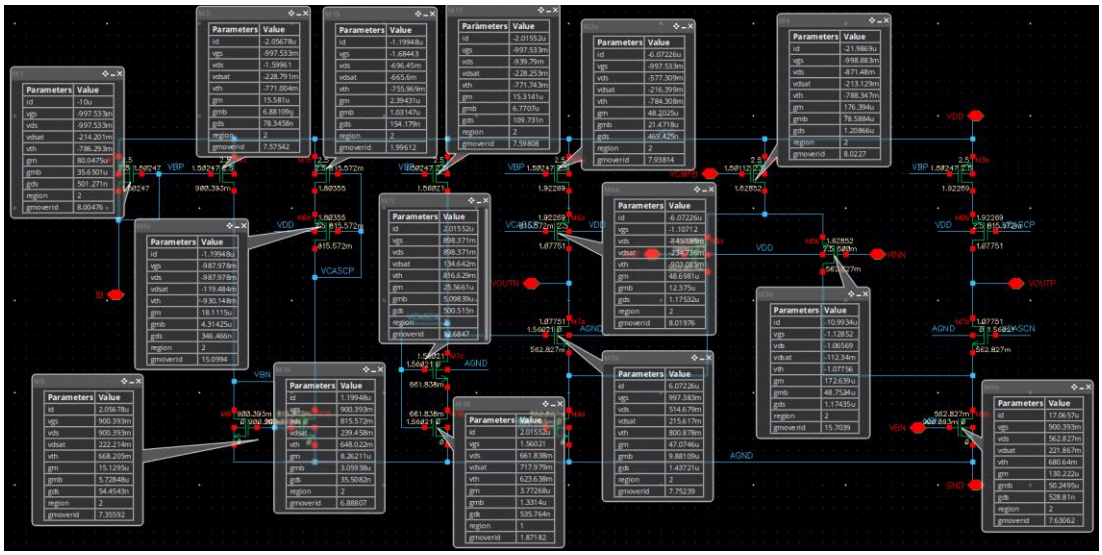

Figure 29: OTA schematic with DC node voltages and OP parameters annotated

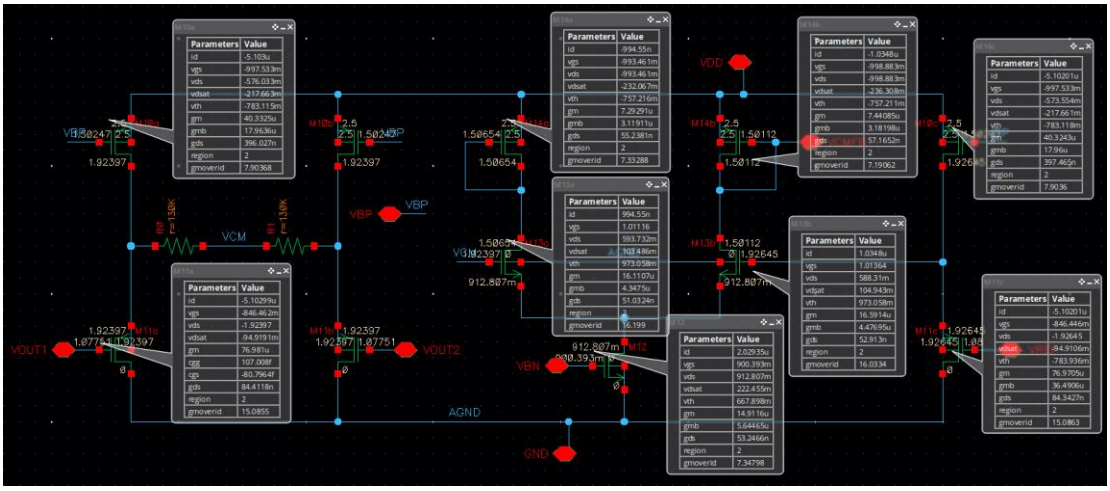

Figure 30: CMFB schematic with DC node voltages and OP parameters annotated

- All devices are in sat except the non-degenerated devices in the biasing circuits.
- We set V_{REF} to 1.08 V as V_{out} max swing is from 0.75 V to 1.4 V.
- The total current consumption in the fully differential OTA, CMFB circuit and current mirror branches is about 66.74 μA (51.5 μA without the current mirror and biasing branches) but that low current consumption in the CMFB circuit results in a very big value for the resistive network in order to activate the circuit plus enhancing linearity.
- The current and gm in the input pair exactly equal, due to the absence of differential signal and dc offset and no mismatch between the devices.
- The dc level of V_{out} is 1.0775 V as a result of the CMFB circuit which tends to minimize the error between the common mode dc level of V_{out} and V_{ref} where the error equals the reciprocal of the CMFB loop-gain.
- The differential input and output voltages of the error amplifier are $-2.5\ mV, -5.4\ mV$. the relation between them is the error amplifier gain (2.2).

2. Diff small signal ccs

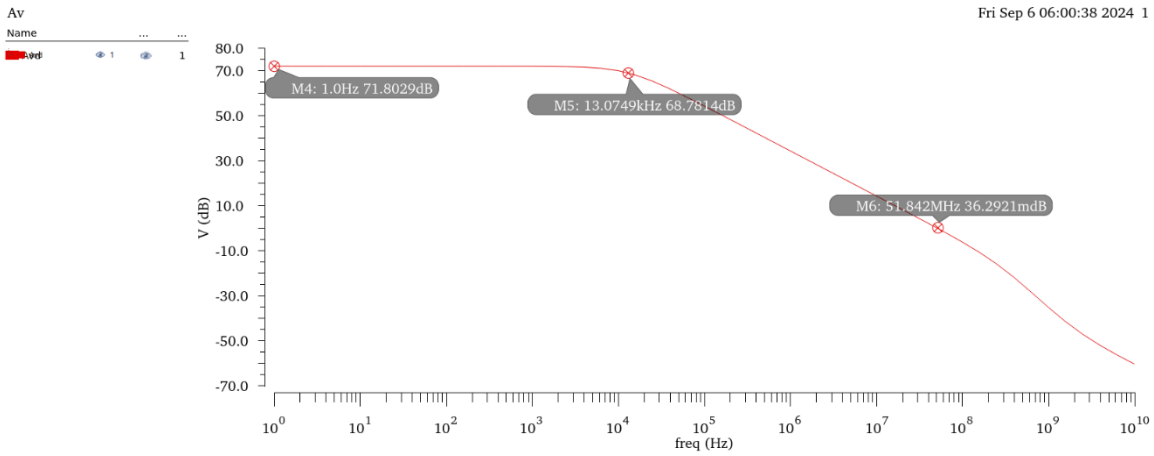

Figure 31: Differential gain bode plot (magnitude)

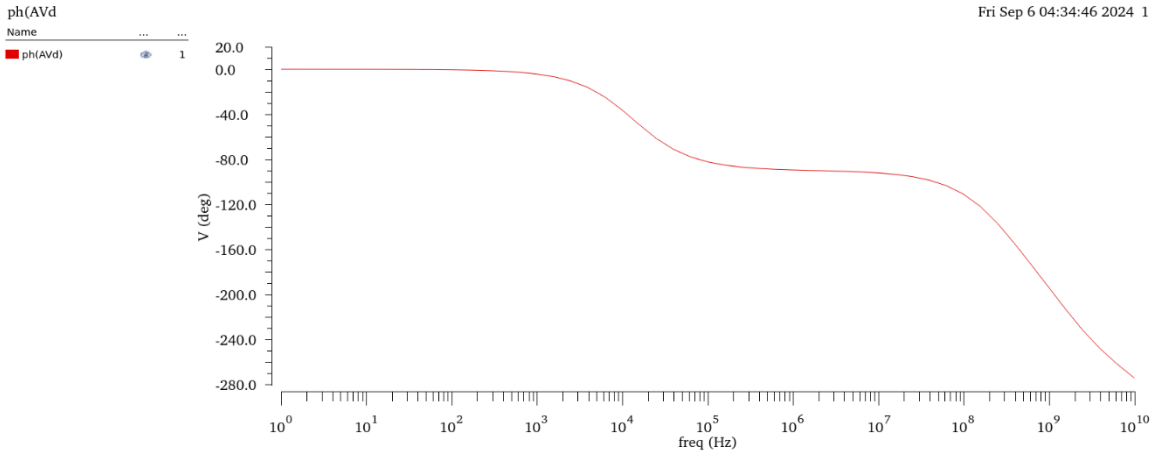

Figure 32: Differential gain bode plot (phase)

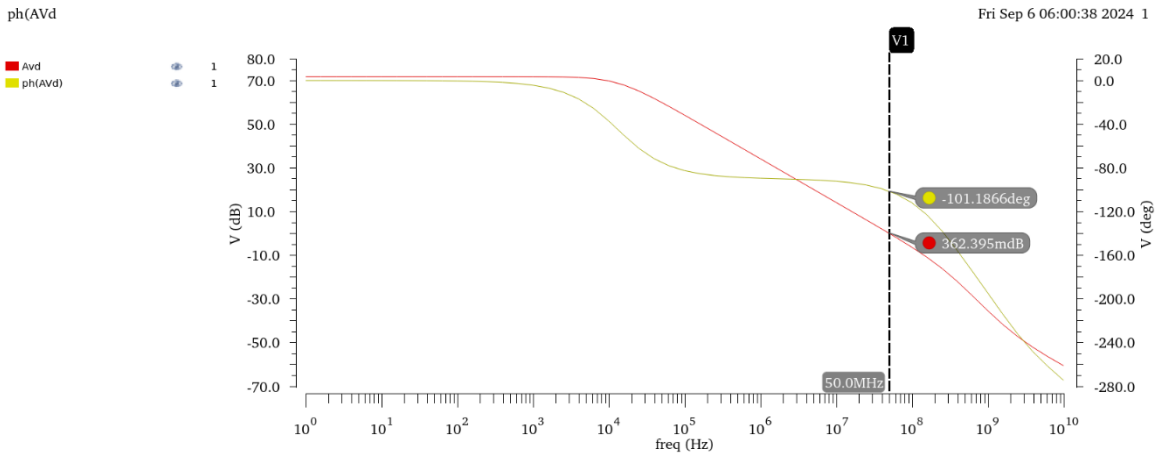

Figure 33: open-loop gain Gx

$PM \approx 78^o$

Test	Output	Nominal	Spec
ITI_labs:lab11_TB1:1	Avd @dc	3.386k	> 3.1k
ITI_labs:lab11_TB1:1	Avd @dc (dB)	70.59	> 70
ITI_labs:lab11_TB1:1	BW	15.24k	
ITI_labs:lab11_TB1:1	GBW	51.71M	> 34.3M
ITI_labs:lab11_TB1:1	UGF	53.4M	> 34.3M

Figure 34: STB analysis results

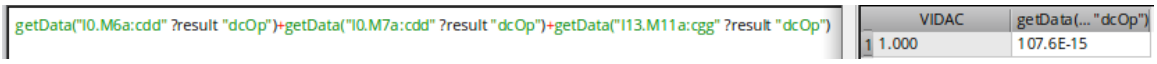

Figure 35: Cout_parasitics

$$|DC\ diff\ gain| = g_{m5} * \left((g_{m6} + g_{mb6})r_{o6}r_{o3} \parallel (g_{m7} + g_{mb7})r_{o7}(r_{o5} \parallel r_{o9})\right)$$

$$BW \approx \frac{1}{2\pi\left((g_{m6} + g_{mb6})r_{o6}r_{o3} \parallel (g_{m7} + g_{mb7})r_{o7}(r_{o5} \parallel r_{o9})\right)(C_L + C_{out\_p})}$$

$$GBW = \frac{g_{m5}}{2\pi(C_L + C_{out\_p})}$$

$$PM = 180 - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right).$$

Spec	*simulation*	*hand analysis*
DC gain	70.6 *dB*	70.4 *dB*
BW	13.4 *KHz*	13.6 *KHz*
GBW	51.7 *MHz*	45 *MHz*
PM	78^o	89^o

Table 5: open-loop simulation vs hand analysis

- GBW & PM hand analysis are different from the simulation as the parasitic caps are not accurate.

Part 5: Closed Loop Simulation (AC and STB Analysis)

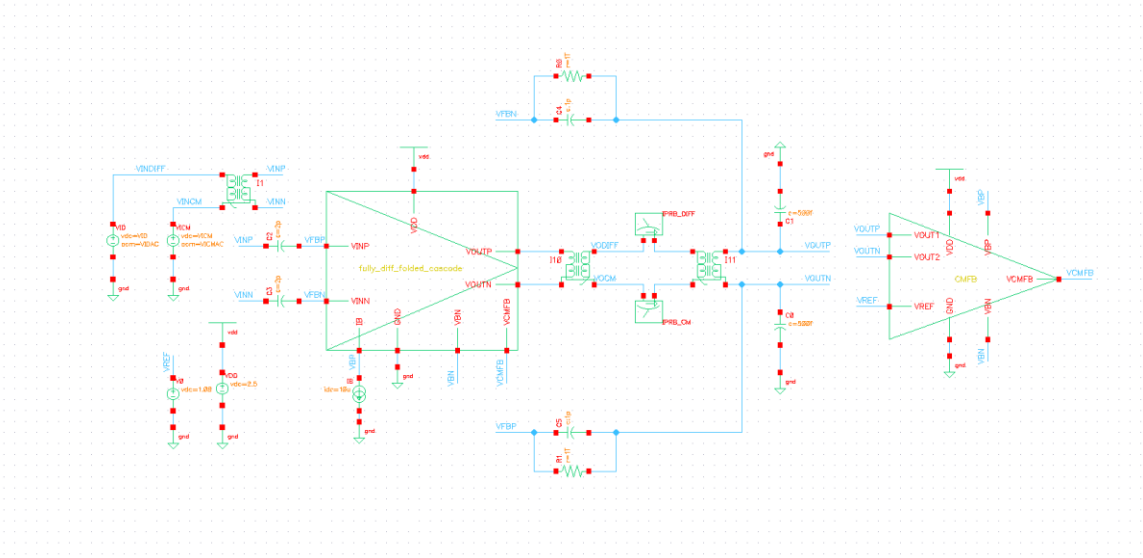

Figure 36: Testbench schematic

1. OP simulation

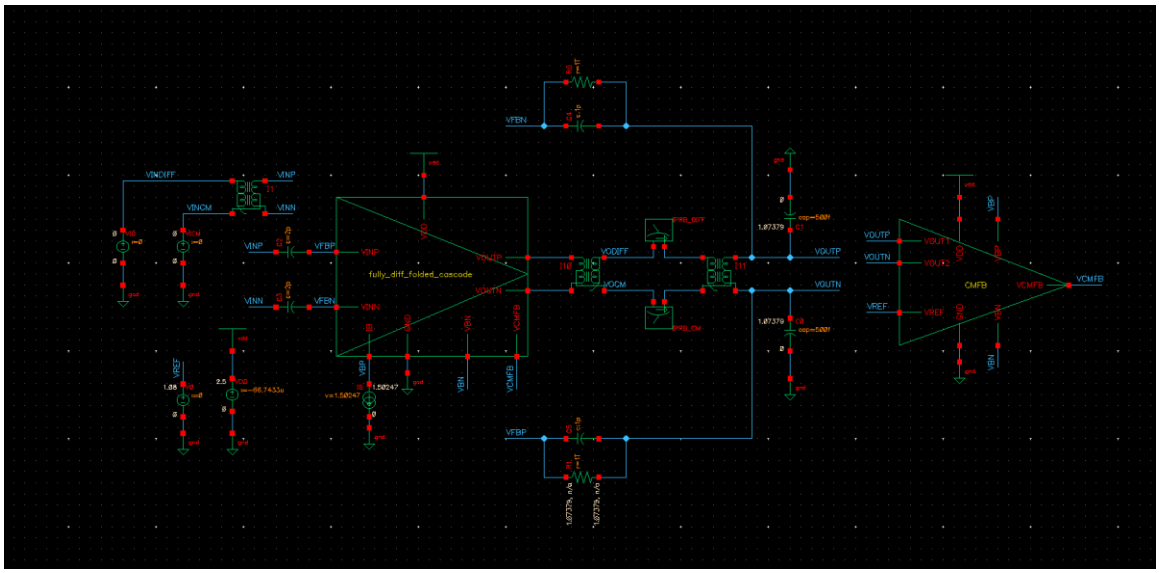

Figure 37: bias circuit with DC node voltages annotated

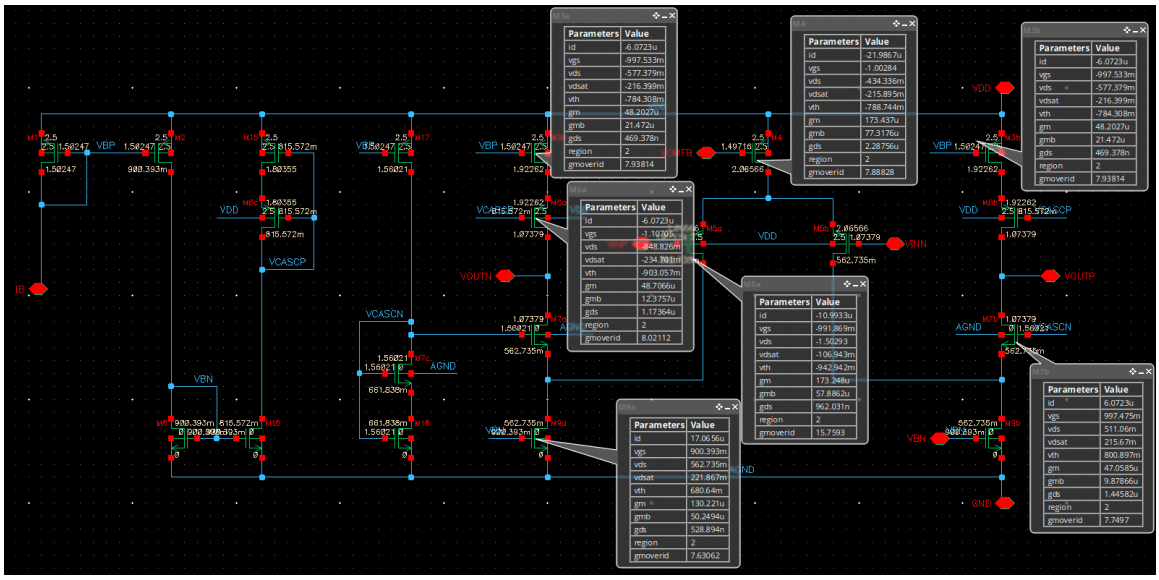

Figure 38: OTA schematic with DC node voltages and OP parameters annotated

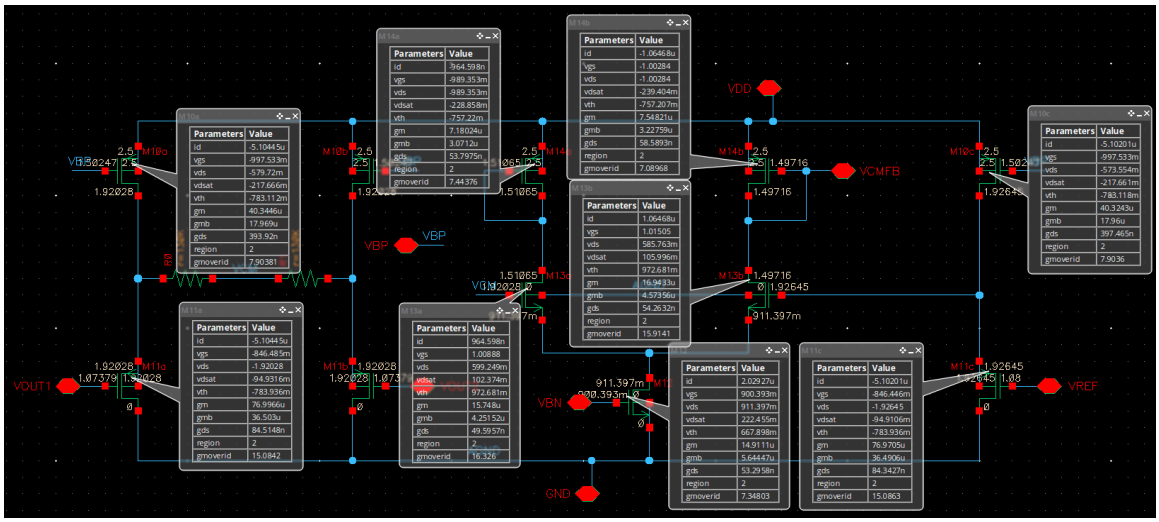

Figure 39: CMFB schematic with DC node voltages and OP parameters annotated

- The OTA output CM level is 1.074 V as the CMFB circuit tends to minimize the error between it and VREF (which is 1.08 V where the error equals the reciprocal of the CMFB loop gain).
- The OTA input CM level is 1.074 V same value as the output CM level because the input capacitance decouples DC and the resistance 1 Tohm creates a DC path - with nearly no current - between the OTA input and output. So in conclusion, the CMFB circuit manages to adjust the OTA input and output to the value of VREF.
- All devices are in sat except the non-degenerated devices in the biasing branches because the CMIR is up to 1.1 V so it will operate in this configuration with $V_{outcm} = 1.08\,V$.

2. Diff closed-loop response

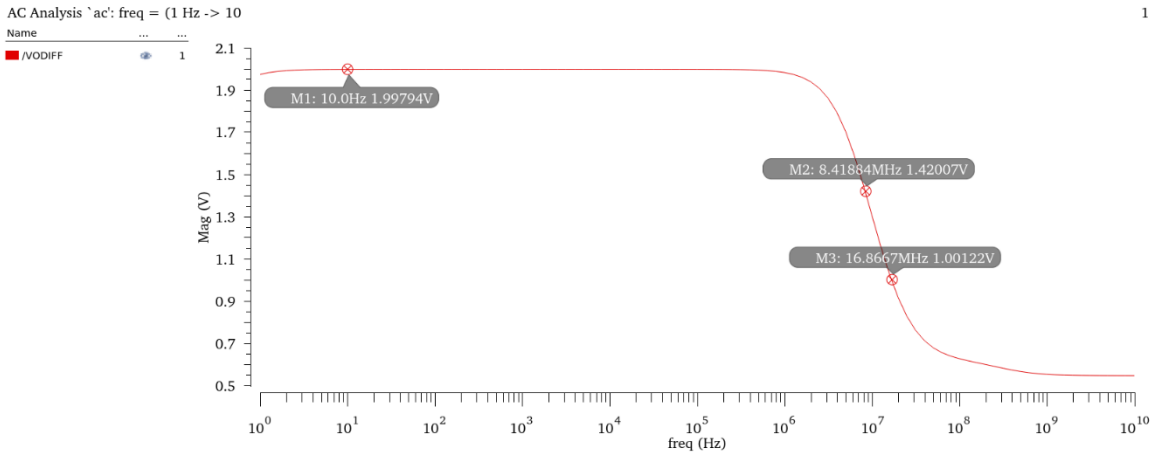

Figure 40: Vodiff vs frequency

Test	Output	Nominal	Spec
ITI_labs:lab11_TB2:1	Acl @DC in V/V	1.998	range 1.99 2.01
ITI_labs:lab11_TB2:1	BWcl	8.742M	> 7.33M
ITI_labs:lab11_TB2:1	GBWcl	17.3M	> 14.64M
ITI_labs:lab11_TB2:1	UGF	16.94M	

Figure 41: diff small signal results

3. Differential and CMFB loops stability (STB analysis)

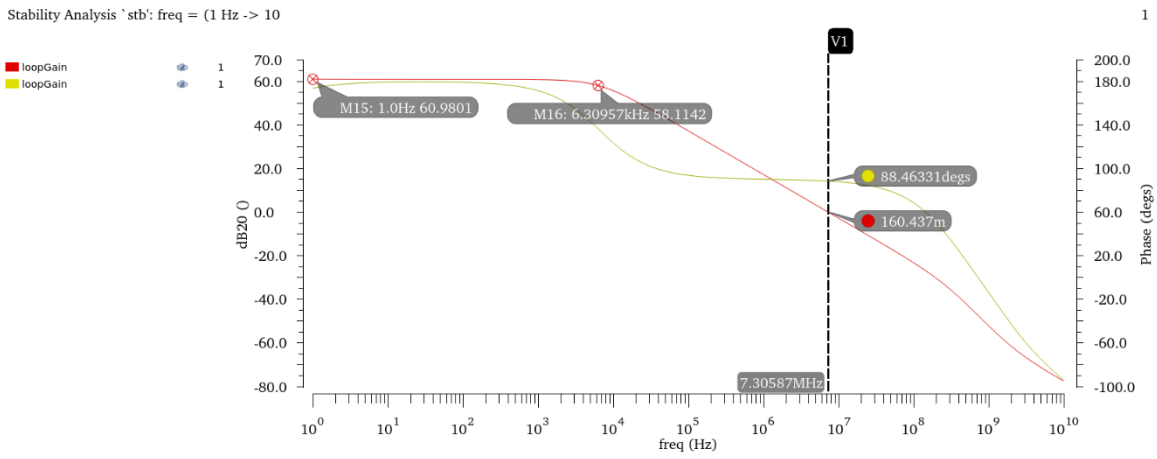

Figure 42: Diff loop bode plot (magnitude and phase)

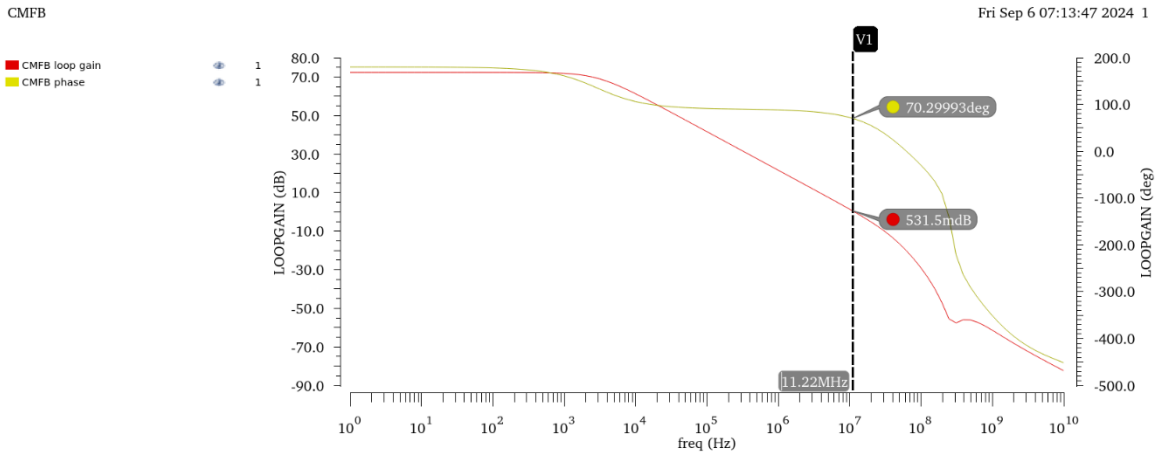

Figure 43: CMFB loop (magnitude and phase)

$Spec$	$diff - loop$	$CMFB - loop$
GBW	7.3 MHz	11.22 MHz
PM	88^o	70^o

Table 6: diff vs CMFB simulations

- GBW is larger in the CMFB as the CMFB loop GBW is nearly the open-loop GBW times 1/2 as gm of the input pair and tail CM are almost the same and it's halved as in the CM half circuit the two branches of the output appears in parallel so the Cout is doubled and the diff loop GBW is the open-loop GBW times β which is less than 1/3 so $diff\ GBW = 2\beta * CMFB\ GBW$.
- The PM of the CMFB loop is less than that of the diff loop as the have near poles but different UGFs so the one with smaller UGF (diff loop) will maintain better stability and better PM.

$Spec$	$closed - loop$	$open - loop$	$mapped\ open\ to\ closed$
$diff\ loop\ gain$	61 dB	70.6 dB	60.9 dB
GBW	7.3 MHz	51.7 MHz	8 MHz

Table 7: comparison with open-loop simulations

- The specs from open-loop are mapped as following:

$$\beta = \frac{C_F}{C_F + C_{in} + C_{in_{ota}}} = 0.328, loop\ gain = A_{ol}(dB) + 20\log(\beta)$$

$$GBW_{LG} = GBW_{ol} * \frac{C_L + C_{out_p}}{C_L + C_{out_p} + \left(C_F \parallel (C_{in} + C_{inota})\right)} * \beta$$

- As we see the GBW is different as in fact the loop gain GBW is UGF not GBW so as it's not a 1st order system so they are not equal that's one of the causes, other reason is that the loading of the CMFB circuit at the output (parasitics) is not accurate from the simulator as a value.

Part 6: Closed Loop Simulation (Transient Analysis)

1. Differential input pulse

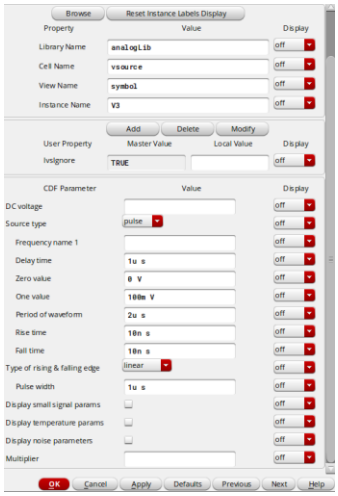

Figure 44: Vsource setup

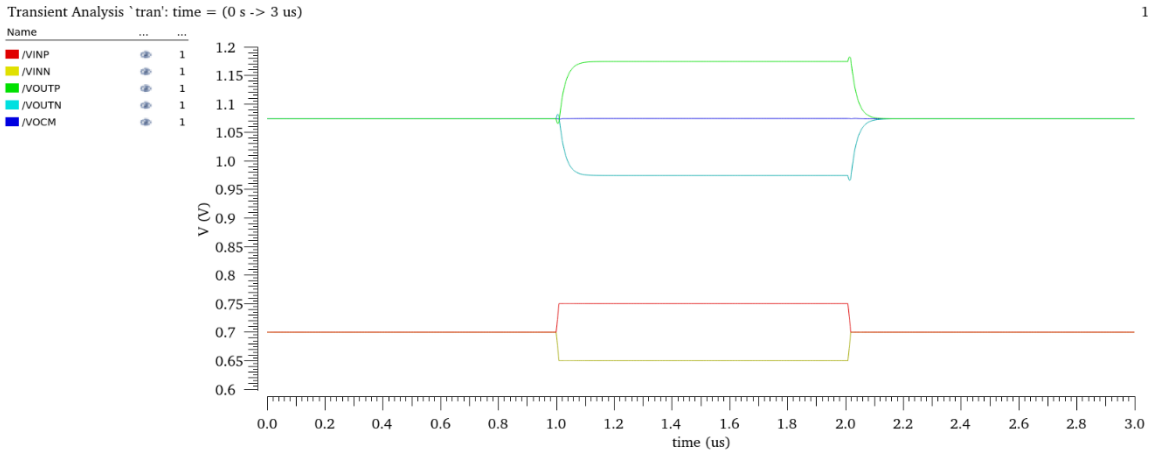

Figure 45: Vinp, Vinn, Voutp, Voutn & Vocm vs time in diff pulse response

- No differential ringing as the PM in the diff loop is much greater than 76.3^o (88^o) and the CMFB PM is less than 76.3^o so it will face ringing but it's very small or even doesn't exist as the circuit is symmetric so the change in V_{outp}&V_{outn} is differentially symmetric and as the CMFB is so fast (high GBW) so its response to any change between the output nodes will be handled instantly.
- Note that the V_{incm} doesn't matter but I put it 0.7 V to make the graph clearer.

```
riseTime(v("/VODIFF" ?result "tran") 0 nil 0.2 nil 0 99 nil "time")
```

Figure 46: settling time expression

Test	Output	Nominal	Spec
ITI_labs:lab11_TB2:1	settling time	97.98n	< 100n

Figure 47: settling time evaluation

- The spec is satisfied.
- A possible solution if the spec is not met is to decrease C_{in} & C_F values as they limit the closed-loop bandwidth but this may make a problem in the spec too as they are the main reason of the small spark which appears in the output as they make voltage divider for few nano seconds, and another solution is to increase the current in the OTA by only increasing the devices widths using cross multiplication.

2. CM input pulse

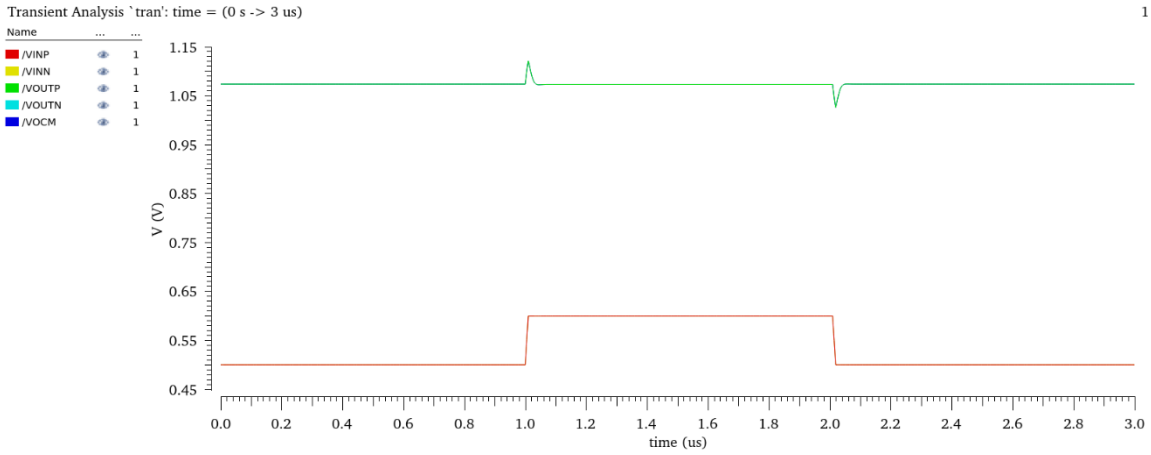

Figure 48: Vinp, Vinn, Voutp, Voutn & Vocm vs time in CM pulse response

- No differential ringing as the PM in the diff loop is much greater than 76.3^o (88^o) and the CMFB PM is less than 76.3^o so it will face ringing but it's very small as the CMFB is so fast (high GBW) so its response to any transient change will be handled instantly.
- The small spark which appears in the output is due to the capacitive feedback as they make voltage divider for the first few nano seconds in the transient response.
- V_{incm} value doesn't matter but I made the pulse from 0.5 to 0.6 V to make the graph clearer.

3. Output swing

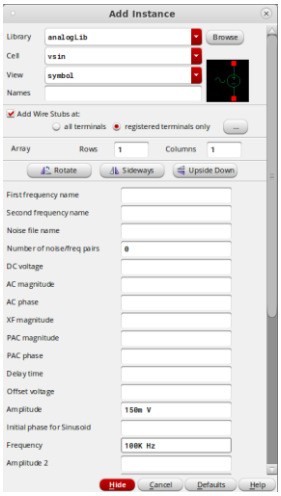

Figure 49: sine wave setup

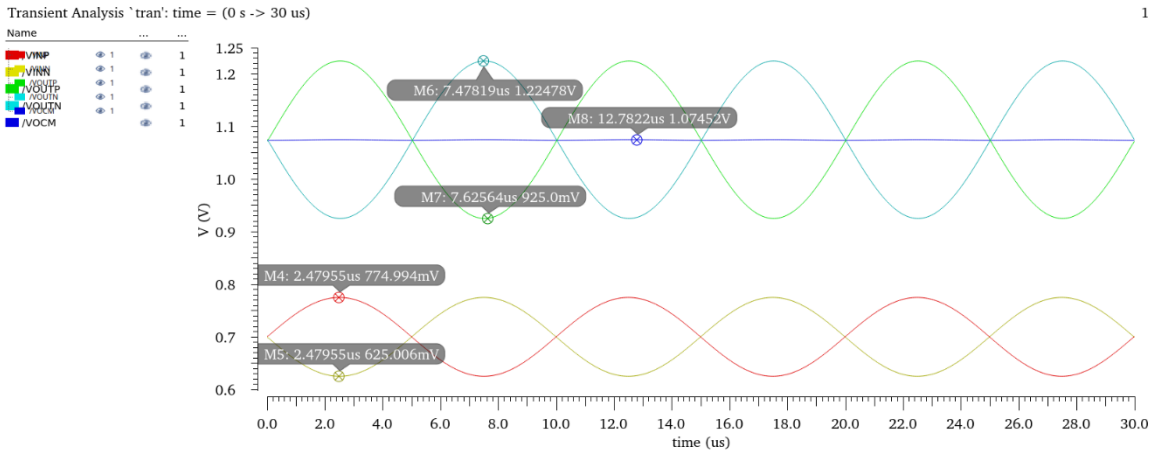

Figure 50: Vinp, Vinn, Voutp, Voutn & Vocm vs time in diff sine wave response

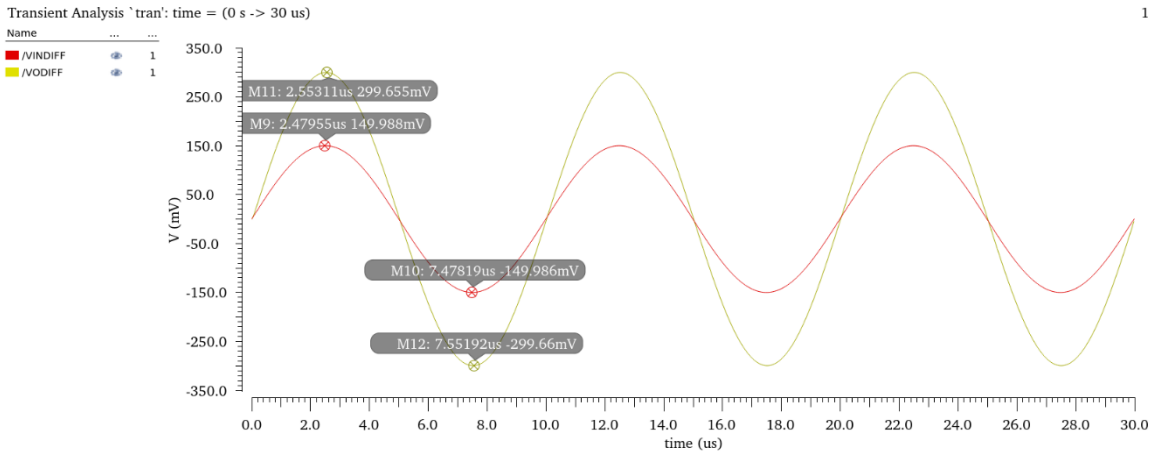

Figure 51: VINDIFF & VODIFF vs time

- Diff input and output peak-to-peak swings are 300 mV and 599.3 mV respectively. So $A_{CL} = 1.998$ the same 4-digits precision as calculated from AC analysis.

Now apply a sine wave of 300 mV as an input to test the maximum differential swing.

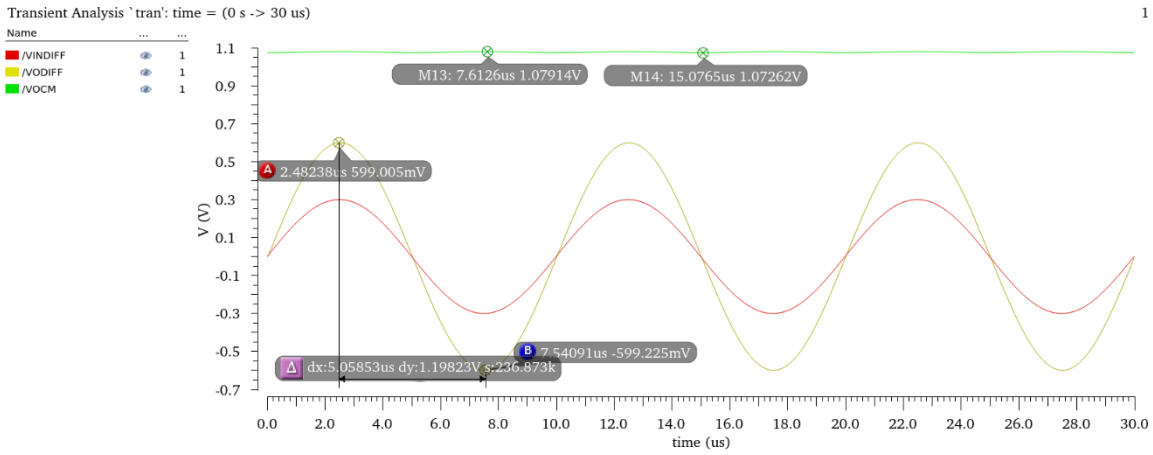

Figure 52: VINDIFF & VODIFF vs time

- Diff input and output peak-to-peak swings are 600 mV and 1.198 V respectively. So $A_{CL} \approx 1.997$ i.e. error of 0.15 % from the Spec (note that the error is in the fourth digit). Also the V_{outcm} deviates to 1.07 V (1% maximum error from V_{ref}) So the peak-to-peak maximum output swing spec is justified (1.2 V).

Part 7: Design Specs

Spec	*Required*	*Achieved*
Supply Voltage	$2.5\ V$	$2.5\ V$
Closed loop gain	2	1.998
Phase margin at the required ACL	$\geq 70°$	$88°$
CMIR - low	$\leq 0\ V$	$-0.5\ V$
CMIR - high	$\geq 1\ V$	$1.1\ V$
Differential output swing	$1.2\ V_{pk2pk}$	$1.2\ V_{pk2pk}$
Load	$500\ fF$	$500\ fF$
DC loop gain	$60\ dB$	$61\ dB$
CL settling time for 1% error	$100\ ns$	$98\ ns$
$Total\ Current\ consumption\ (including\ the\ CM\ branches)$	$-$	$63.5\ \mu A$
$Total\ devices\ area\ (OTA + CMFB)$	$-$	$55.3 + 105.3 = 160.6\ (\mu m)^2$

Table 8: Design specs