Final Project

SAR ADC

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Part 1: SAR Logic

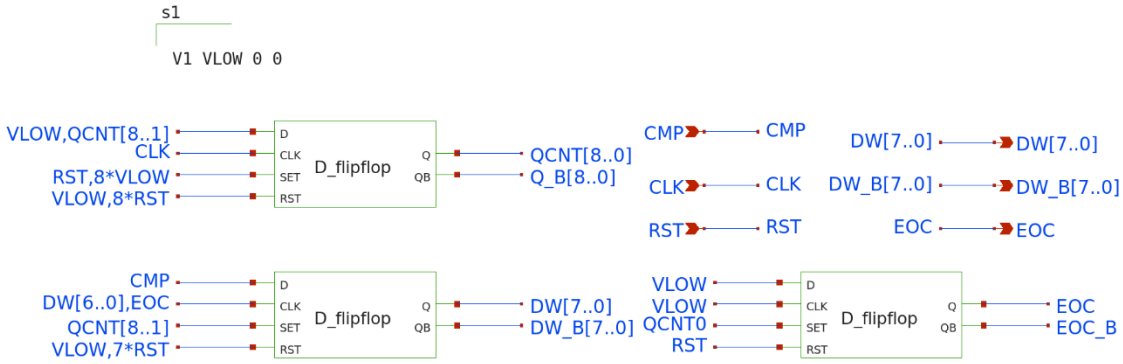

Figure 1: 8-bit SAR logic schematic

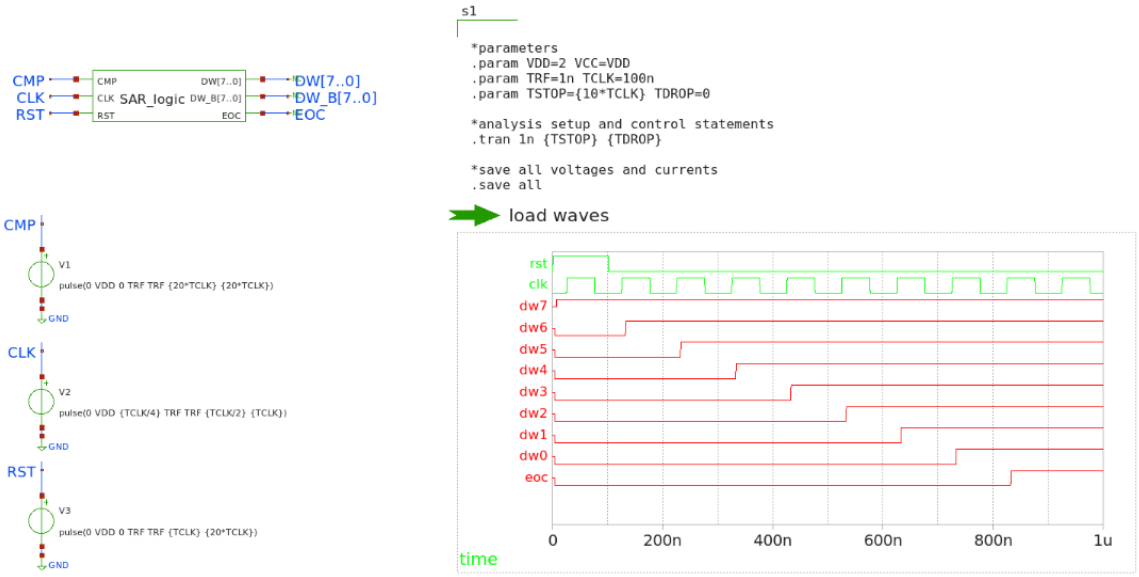

Figure 2: 8-bit SAR logic testbench

3) Report transient simulation results for the ring counter output, the code register output, and the EOC signal

a. CMP is all zeros

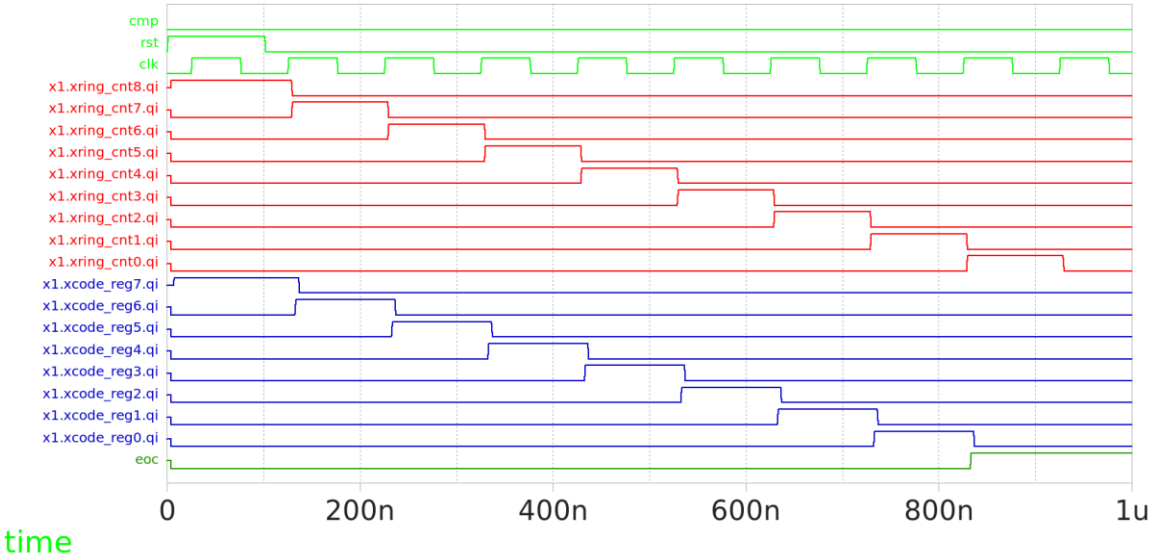

Figure 3: SAR transient signals in all zeros case

b. CMP is all ones

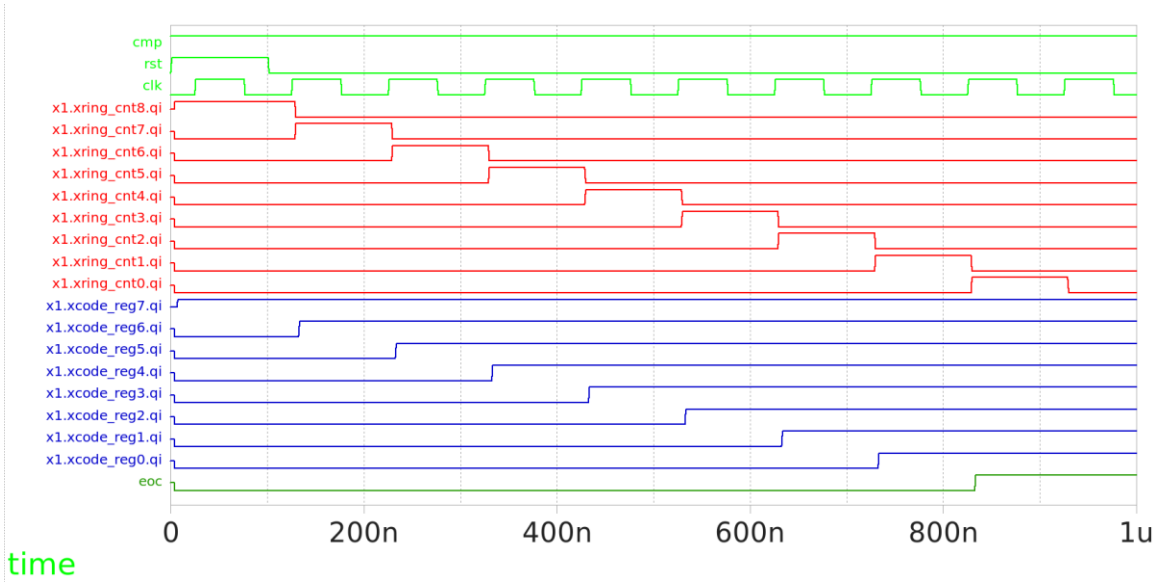

Figure 4: SAR transient signals in all ones case

c. CMP is alternating ones and zeros

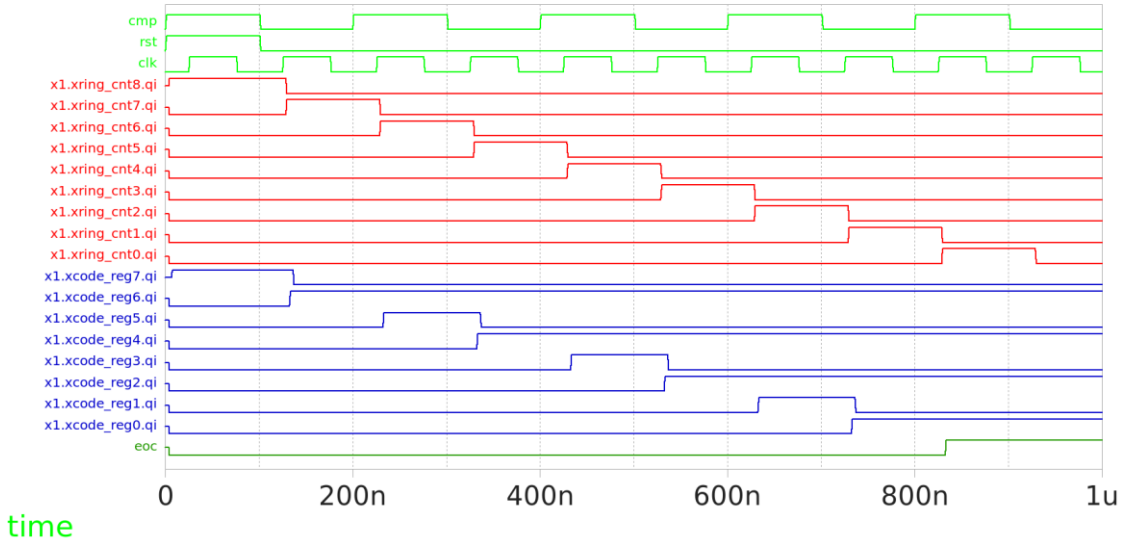

Figure 5: SAR transient signals in alternating zeros and ones case

The SAR logic implementation works as follows:

At first, the reset (RST) – which will be the start of conversion (SOC) i.e. the sampling clock – resets the end of conversion (EOC), the least 8 significant bits (LSBs) in the ring counter and the least 7 significant bits in the code register/digital output, and sets the most significant bit (MSB) in the ring counter so the ring counter starts with (100000000) and counts with the clock (CLK) where the 8 MSBs are the set for the code register so the digital output will be (10000000) which will be converted by the Digital to Analog converter (DAC) and compared by the comparator to the input and gives output CMP which is the D input to the code register which are synchronized by the 7 LSBs in the code register and the EOC. The next clock counts (010000000) in the ring counter so it sets DW[6] (digital word of the code register) to 1 which in turn is the CLK of DW[7] so the DW[6] positive edge transfers the CMP signal of the first comparison to DW[7] which is referred as B_7 **in Table 1**. The code register output ($B_7$1000000) is converted and compared to the input giving new CMP signal and the next cycle the ring couter counts (001000000) and DW[5] is set to 1 which is the clock of DW[6] so DW[6] will be B_6 (the second cycle CMP signal) and so on till the ring counter counts 000000001 which sets the EOC to 1 which in turn is the CLK of DW[0] so it sets DW[0] to B_0 and so, the digital output is ready to be read from the code register output at the positive edge of the EOC. So, it successfully implements the SAR algorithm.

Table 1: SAR logic table

Clock cycle	DW<7>	DW<6>	DW<5>	DW<4>	DW<3>	DW<2>	DW<1>	DW<0>	CMP
1 (reset)	1	0	0	0	0	0	0	0	
2	1	0	0	0	0	0	0	0	B7
3	B_7	1	0	0	0	0	0	0	B6
4	B_7	B_6	1	0	0	0	0	0	B5
5	B_7	B_6	B_5	1	0	0	0	0	B4
6	B_7	B_6	B_5	B_4	1	0	0	0	B3
7	B_7	B_6	B_5	B_4	B_3	1	0	0	B2
8	B_7	B_6	B_5	B_4	B_3	B_2	1	0	B1
9	B_7	B_6	B_5	B_4	B_3	B_2	B_1	1	B0
10	B_7	B_6	B_5	B_4	B_3	B_2	B_1	B_0	EOC

Part 2: Transmission Gate

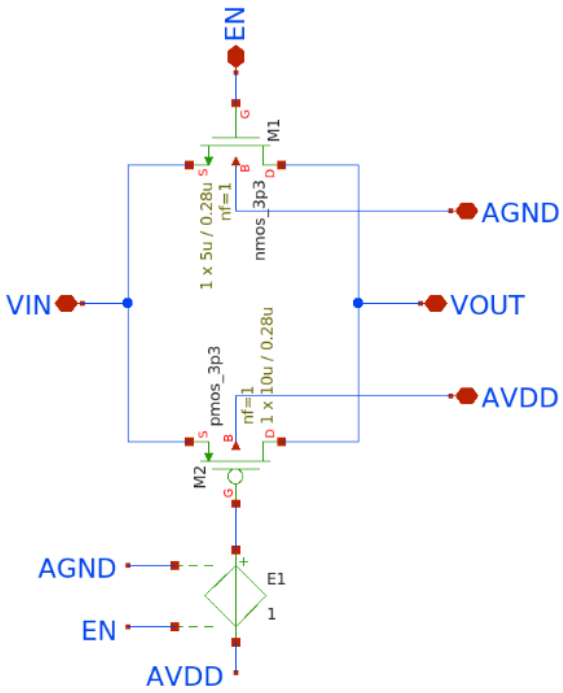

Figure 6: Transmission gate schematic

Part 3: Bottom-Plate Switch

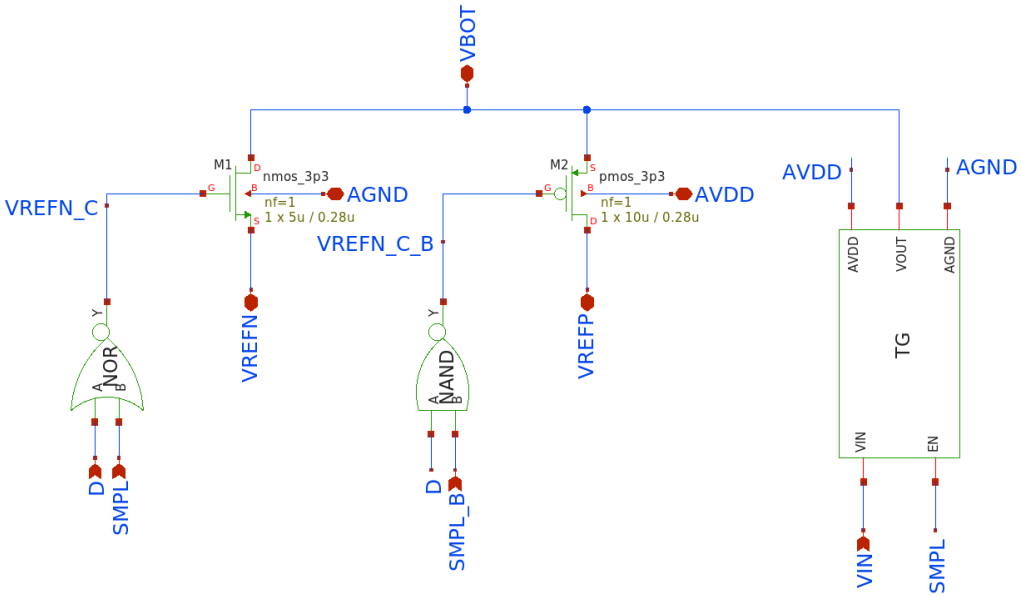

Figure 7: Bottom-plate switch schematic

Part 4: SAR ADC Design

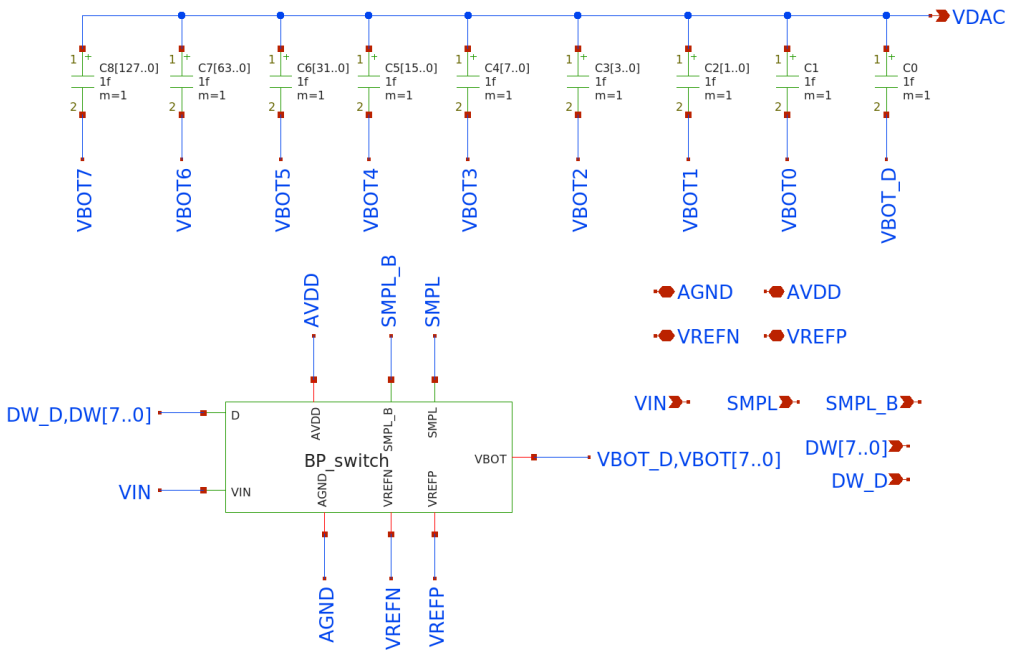

Figure 8: 8-bit capacitive DAC schematic

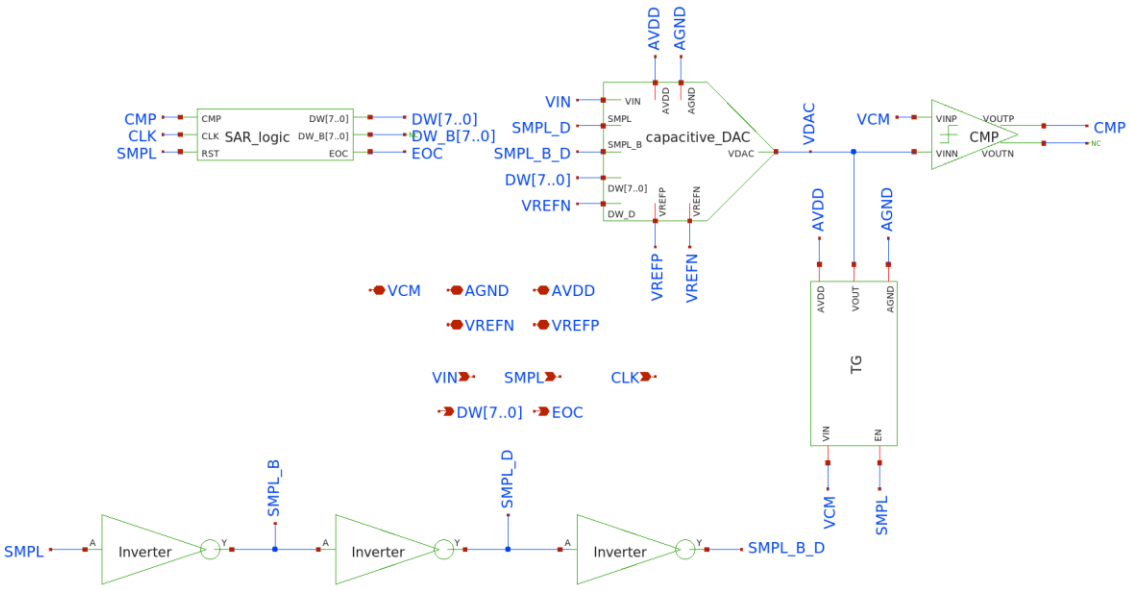

Figure 9: 8-bit SAR ADC schematic

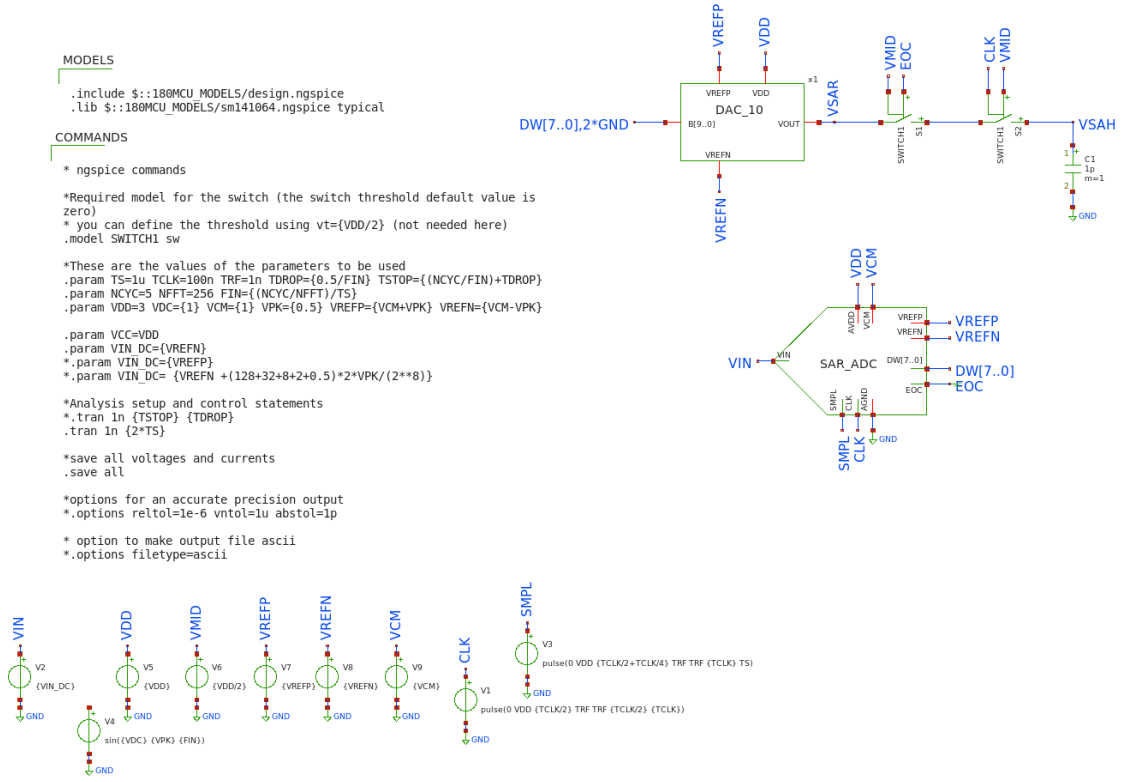

Figure 10: 8-bit SAR ADC testbench

Part 5: DC Functional Test

a. VIN = VREFN

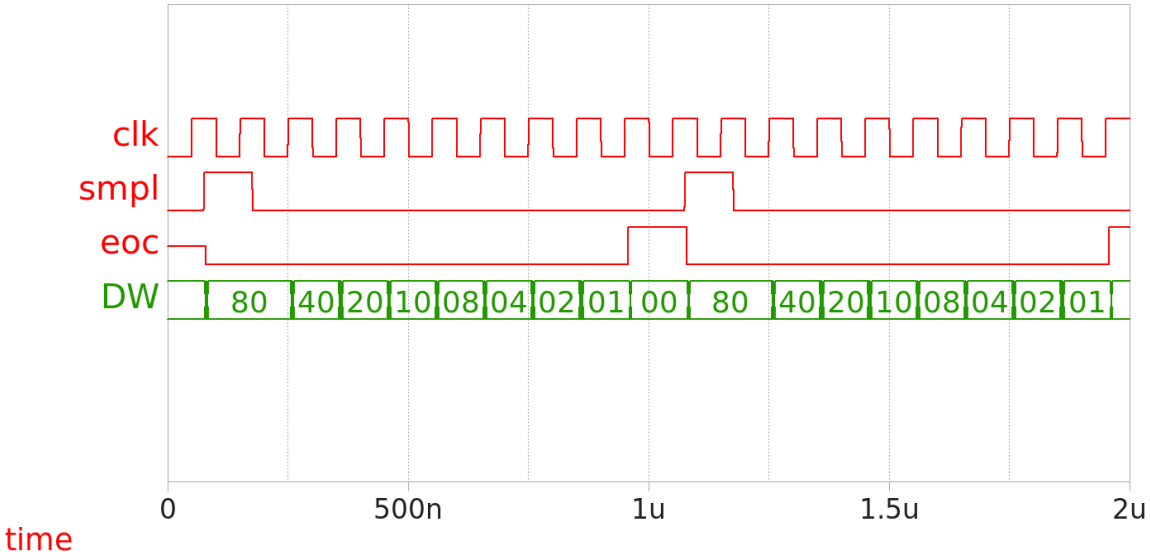

Figure 11: Transient waveforms in the V_{REFN} case

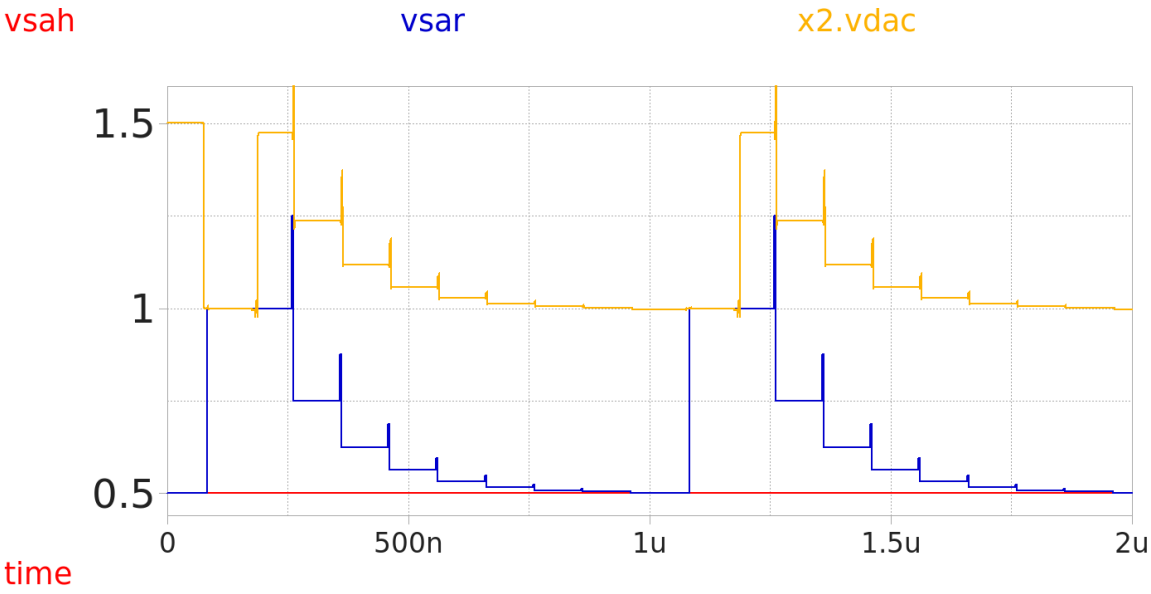

Figure 12: Transient V_{SAH}, V_{SAR} &V_{DAC} in the V_{REFN} case

b. VIN = VREFN + (128+32+8+2+0.5)*VLSB

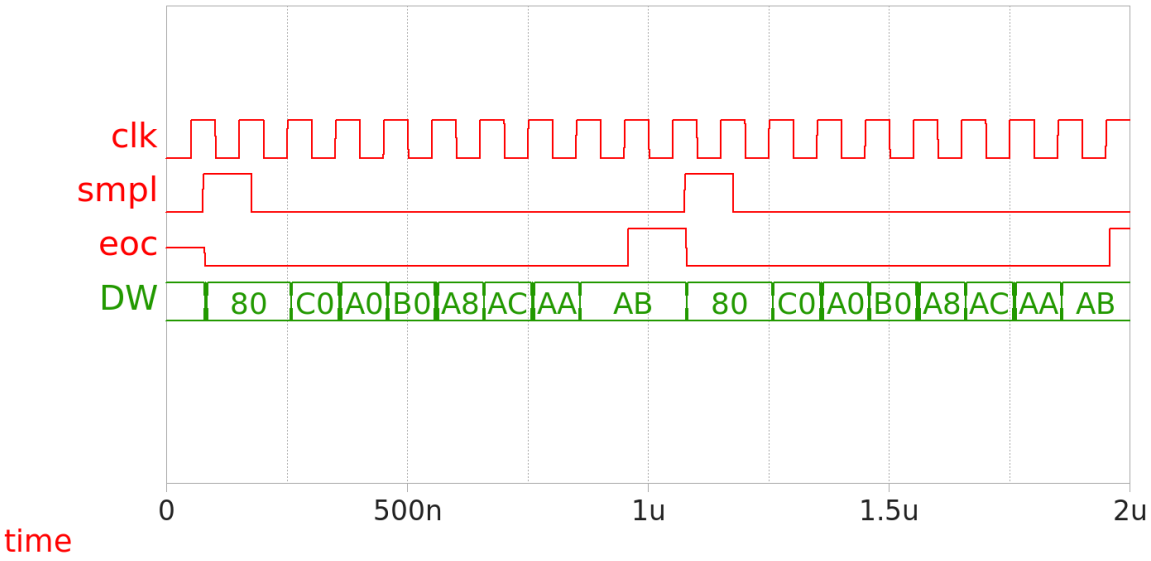

Figure 13: Transient waveforms in the V_{REFN} + (128+32+8+2+0.5)V_{LSB} case*

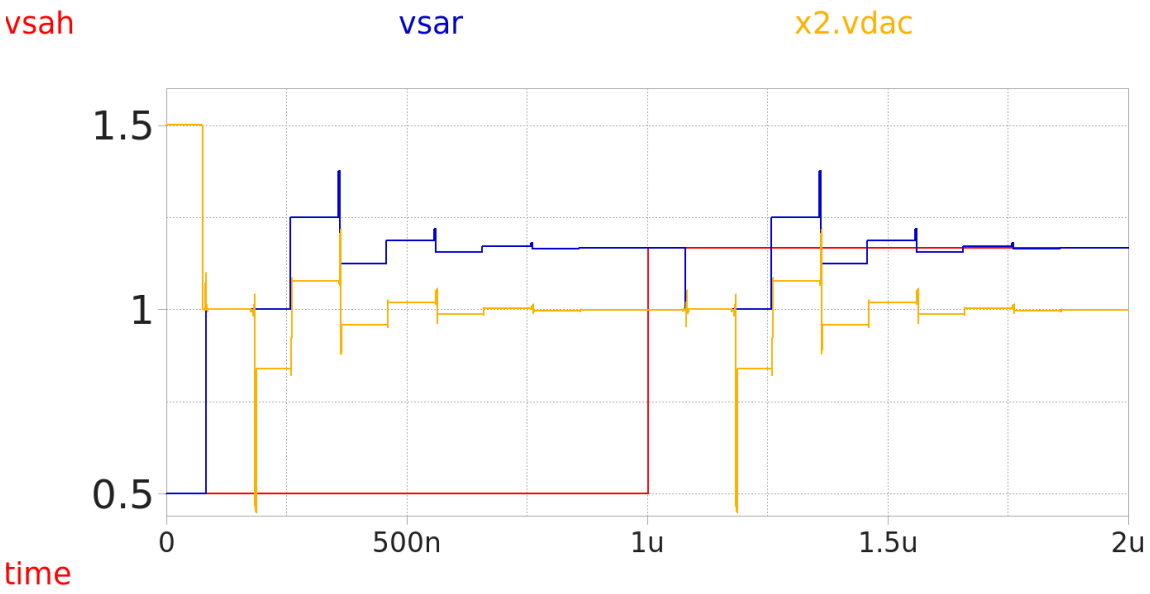

Figure 14: Transient V_{SAH}, V_{SAR} &V_{DAC} in the V_{REFN} + (128+32+8+2+0.5)V_{LSB} case*

c. VIN = VREFP

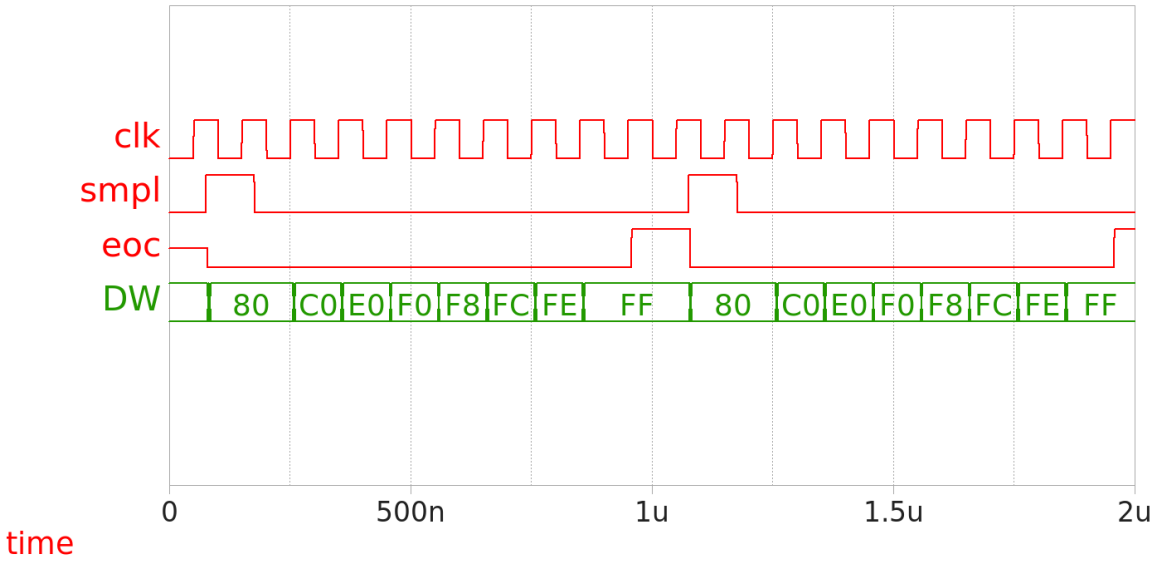

Figure 15: Transient waveforms in the V_{REFP} case

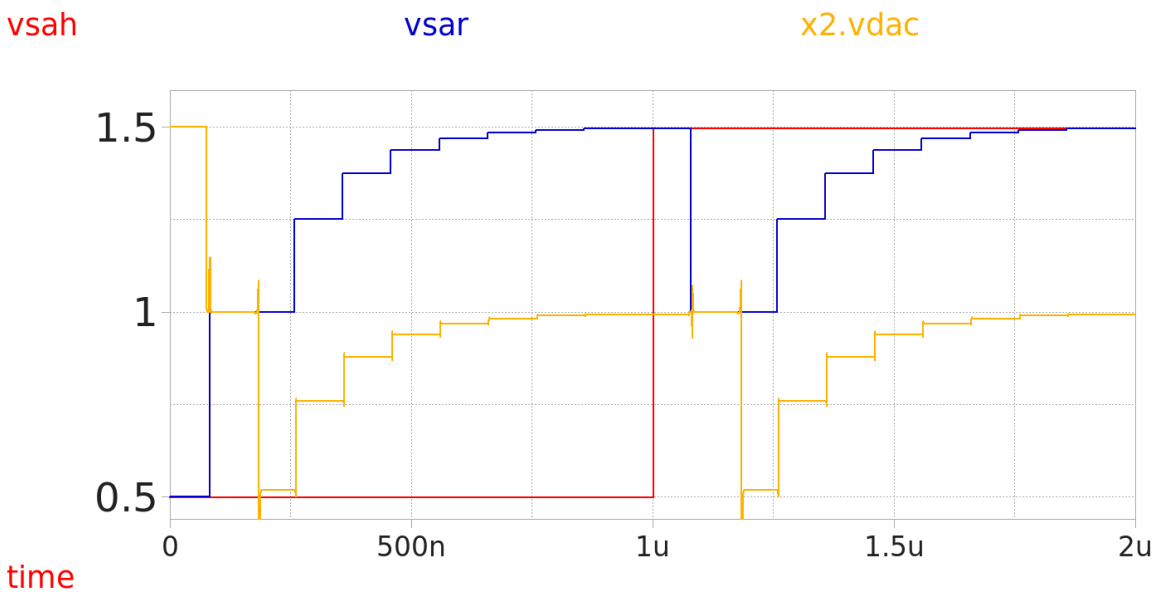

Figure 16: Transient V_{SAH}, V_{SAR} &V_{DAC} in the V_{REFP} case

The SAR DC functionality is good and the SAR works in a correct way as it compares with the analog value of (10000000) and the comparison decides the MSB then switches to the next bit and compares and so on.

Part 6: Sine Wave Test

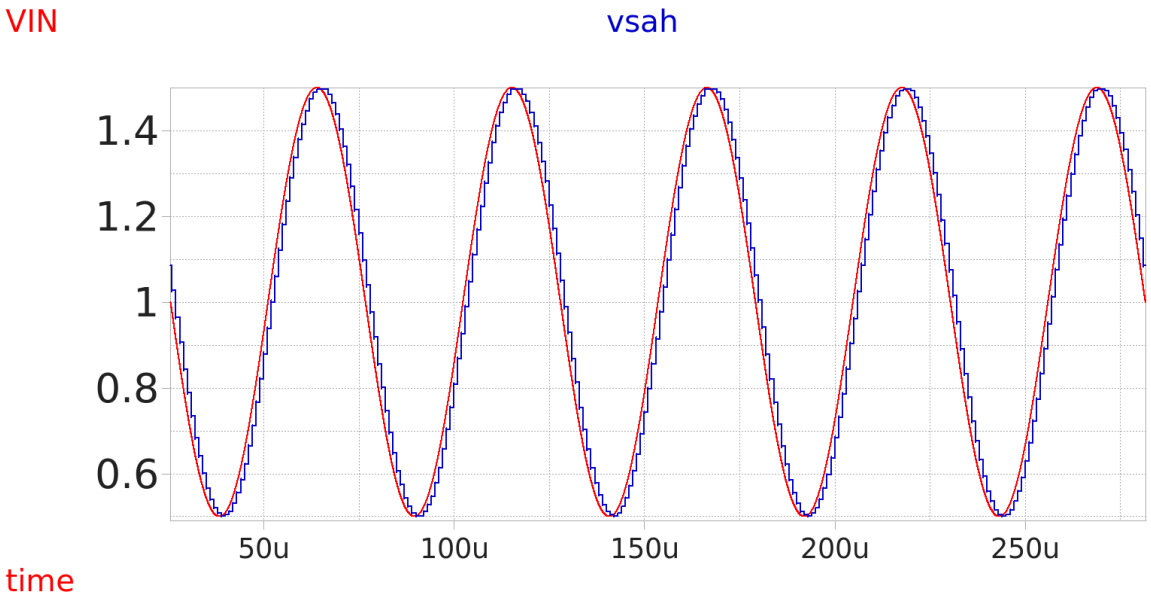

Figure 17: Transient Vin &Vsah

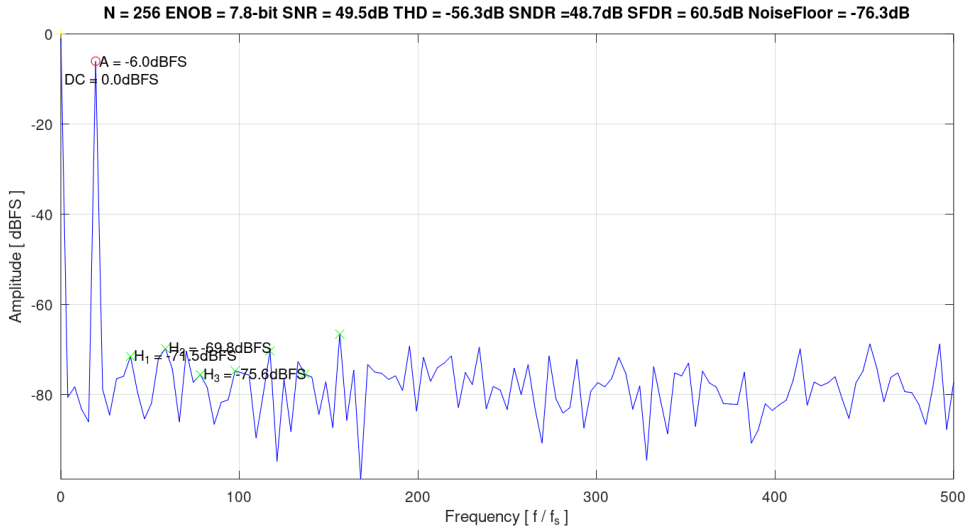

Figure 18: V_{SAH} spectrum

Table 2: SAR specs

Spec	8-bit SAR
ENOB	7.8 bits
SINAD	48.7 dB
SNR	49.5 dB
SFDR	60.5 dB
THD	-56.3 dB
Signal power	-6 dB
DC power	0 dB

- The ENOB is less than 8 due to the quantization error, pedestal step errors (clock feedthrough and charge injection) and may be also parasitics error.
- The noise are thermal noise and also quantization noise which are approximated to white noise as the test is coherent and the resolution is relatively high (huge number of levels) and the distortion is from the system non-linearities as the non-linear parasitics and the comparator non-linearity.
- The pedestal step errors are linear due to the bottom plate sampling so it enhances the total harmonic distortion.
- The signal amplitude is 0.5V and the power is evaluated as $20\log(Amplitude)$ not $20\log RMS$ so its value is -6 dB.
- The DC value is 1V so it's 0 dB.

Part 7: Fully-Differential SAR ADC

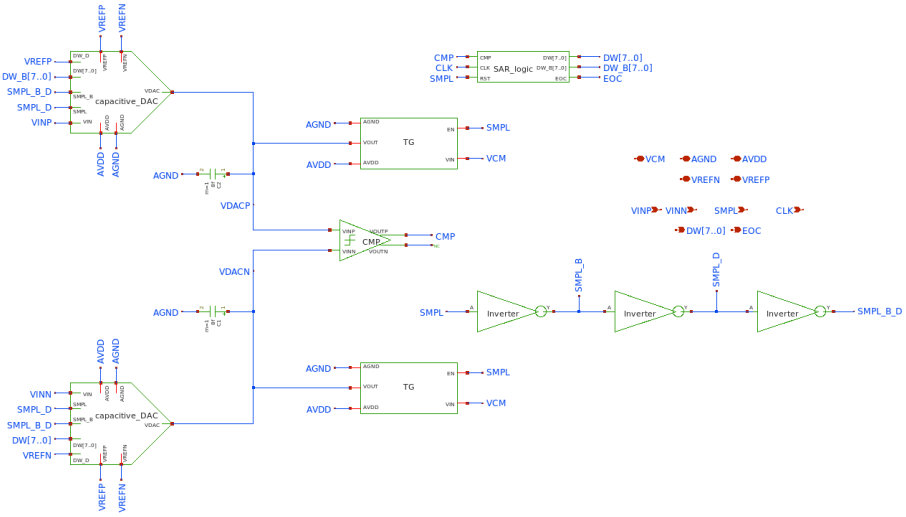

Figure 19: Differential 8-bit SAR ADC schematic

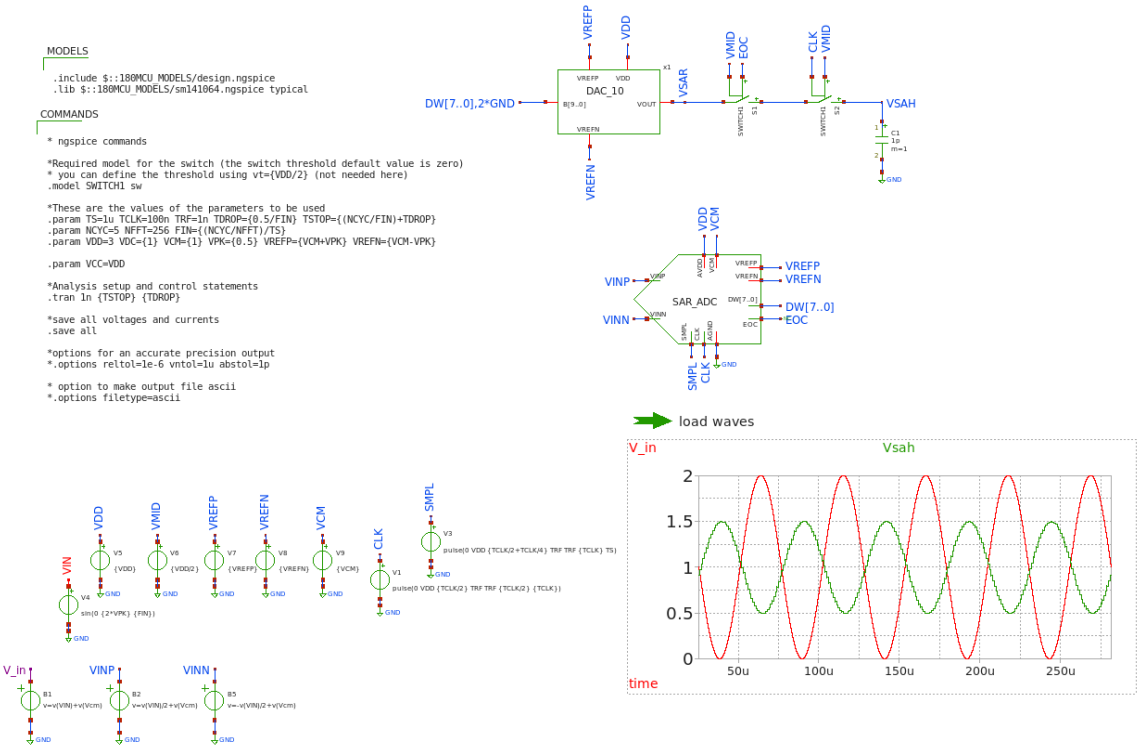

Figure 20: Differential 8-bit SAR ADC testbench

Sine wave test

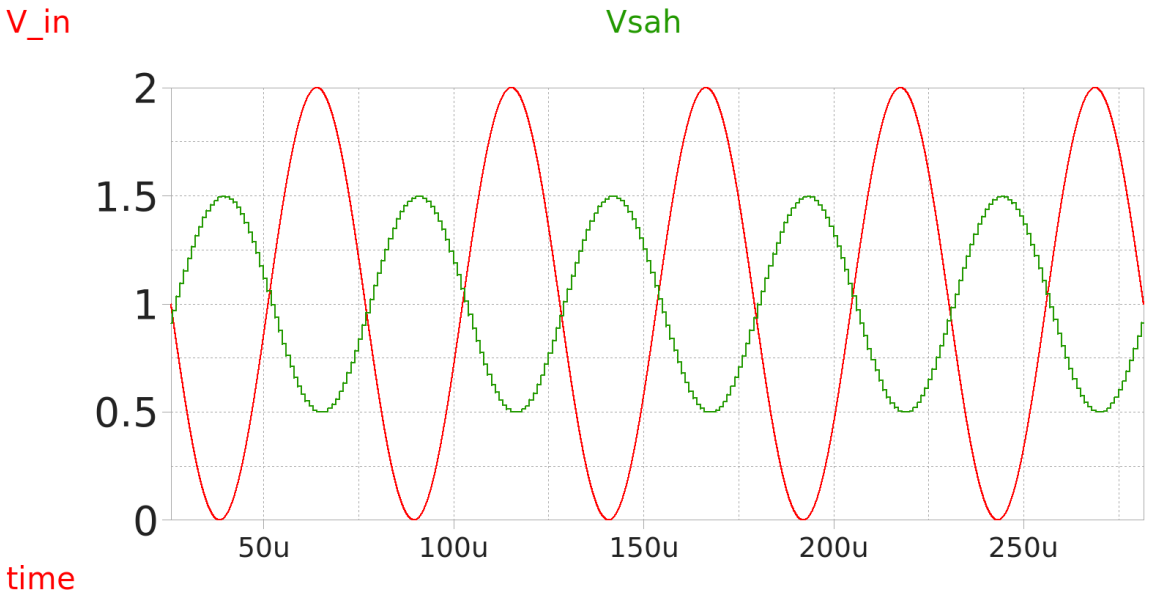

Figure 21: Transient V_{in} and V_{SAH}

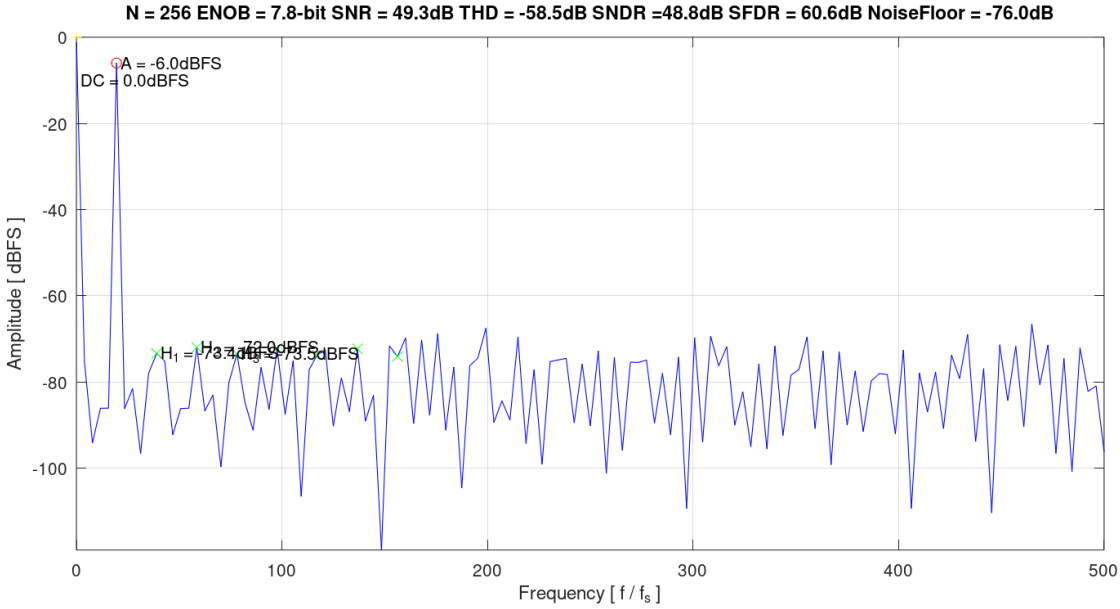

Figure 22: V_{SAH} spectrum in the differential topology

Table 3: SAR specs

FOC	8-bit SAR	Differential 8-bit SAR
ENOB	7.8 bits	7.8 bits
SINAD	48.7 dB	48.8 dB
SNR	49.5 dB	49.3 dB
SFDR	60.5 dB	60.6 dB
THD	-56.3 dB	-58.5 dB
Signal power	-6 dB	-6 dB
DC power	0 dB	0 dB
Highest harmonic	2^{nd} = -69.8 dB	3^{rd} = -72 dB

- The only difference between the differential and single-ended is the larger input signal swing and the linearity enhancement as the differential removes the even harmonics in the capacitive DAC so, there are small differences in SINAD, SFDR and THD.
- The enhancement would be larger if it was fully-differential as it would enhance the linearity of the whole system (the whole SAR ADC) but in the current case the other system components non-linearities still exist (e.g. the comparator) and adds more parasitics, noise and pedestal step errors to the system as there are more switches which generate thermal noise and adds linear errors by bottom plate switches. The enhancement would be better at higher full scale too as the non-linearities would increase in the single-ended and the differential will remove the even harmonics.
- The DC power is not removed as the Vsah output is single-ended and the SAR ADC is not fully-differential while the second harmonic is attenuated and now the thisd harmonic is the highest harmonic component.
- The differential signal amplitude is 1V to use the full scale in each terminal in the differential SAR (from V_{REFN} to V_{REFP}) and the output power is evaluated as $20\log(Amplitude)$ not $20\log RMS$ so its value is -6 dB.
- The V_{SAH} is inverted as the input terminals V_{inp} and V_{inn} are reversed.
- The parasitic caps Cp values are not given so I put them 8 fF.