

Self-Biased Sub-1V Bandgap Reference Circuit

Bilal Ramadan

Supervisor: Dr. Hesham Omran

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Part 1: Design Required Specs

Technology	65 nm CMOS
Supply Voltage	2 V
Change versus Temperature	< 1 mV
Change across Corners	< 10 mV
Current consumption	< 10 μ A
Phase margin	> 60°

Table 1: Required specs

The Design will be on three phases as follows:

Part 2: BGR Core Circuit

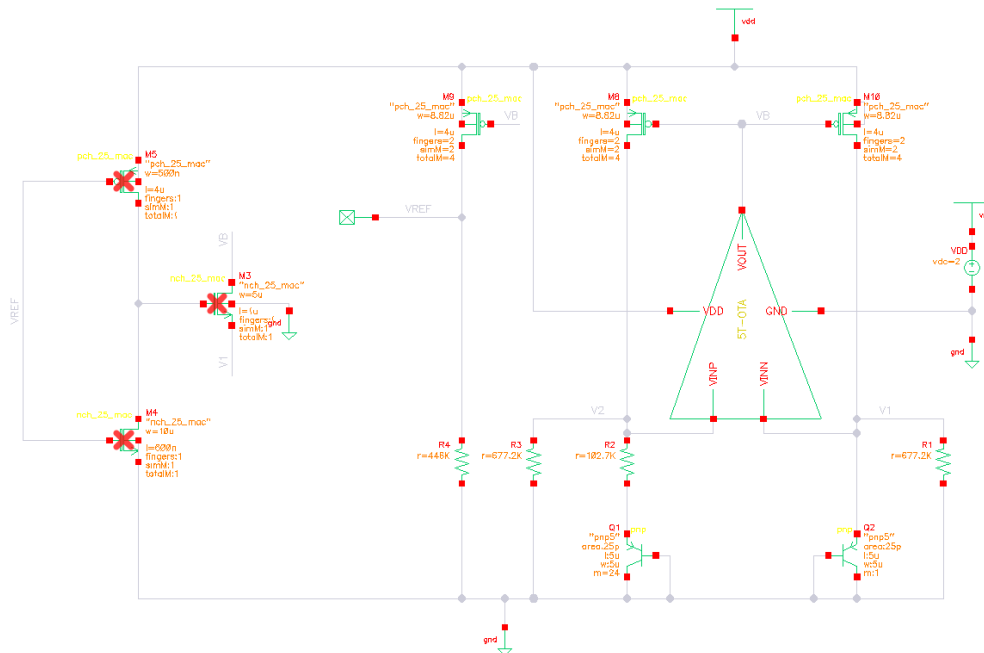


Figure 1: schematic

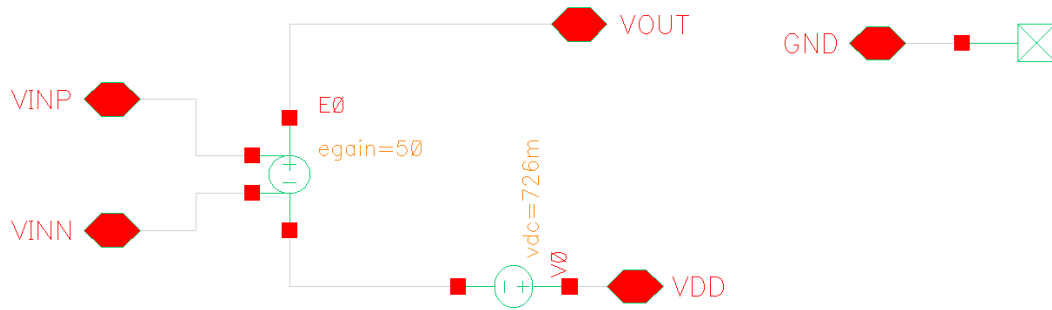


Figure 2: Error amplifier behavioral model

1. OP simulation

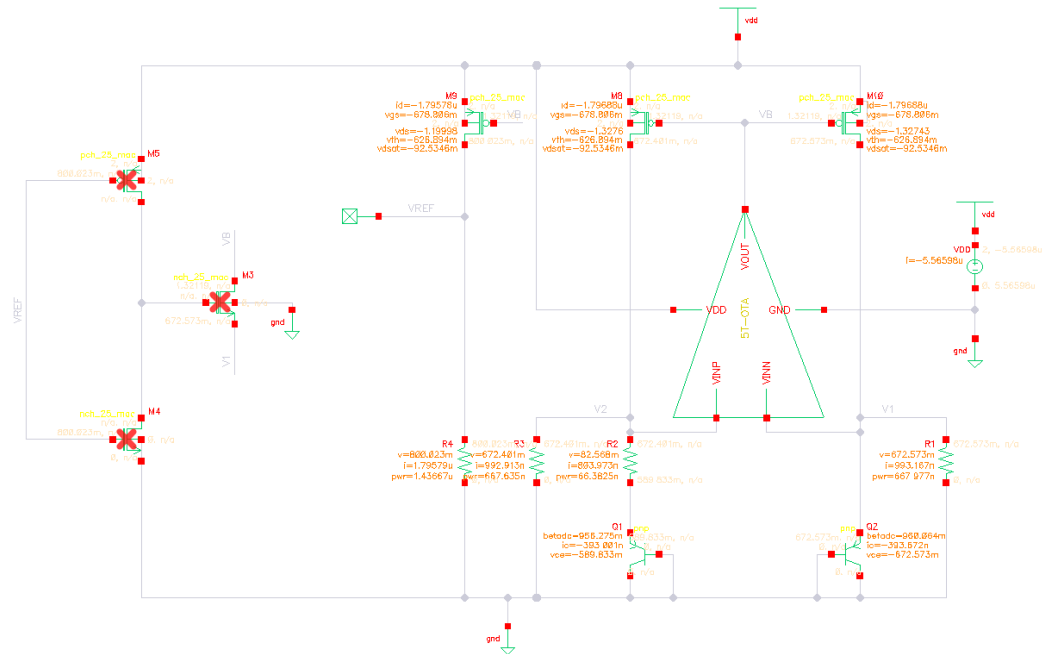


Figure 3: schematic with DC OP and node voltages annotated

2. DC temperature sweep simulation

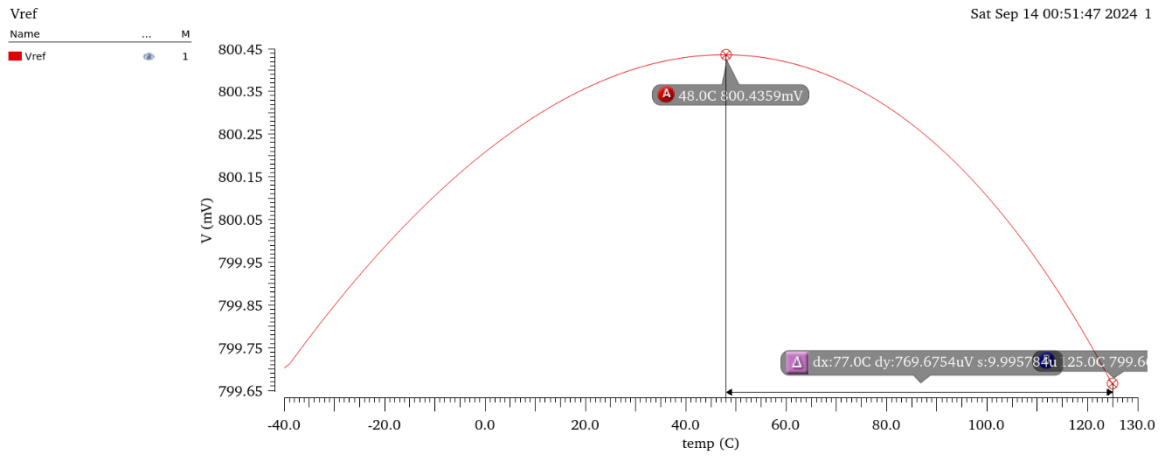


Figure 4: Vref vs temperature with 0.8 mV change

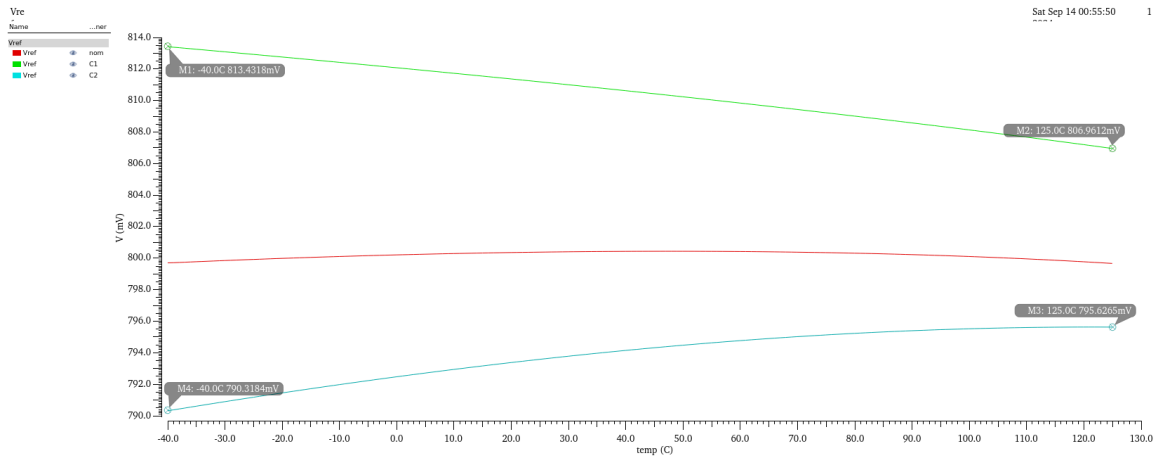


Figure 5: Vref across corners with 6 mV change

Part 3: Error Amplifier

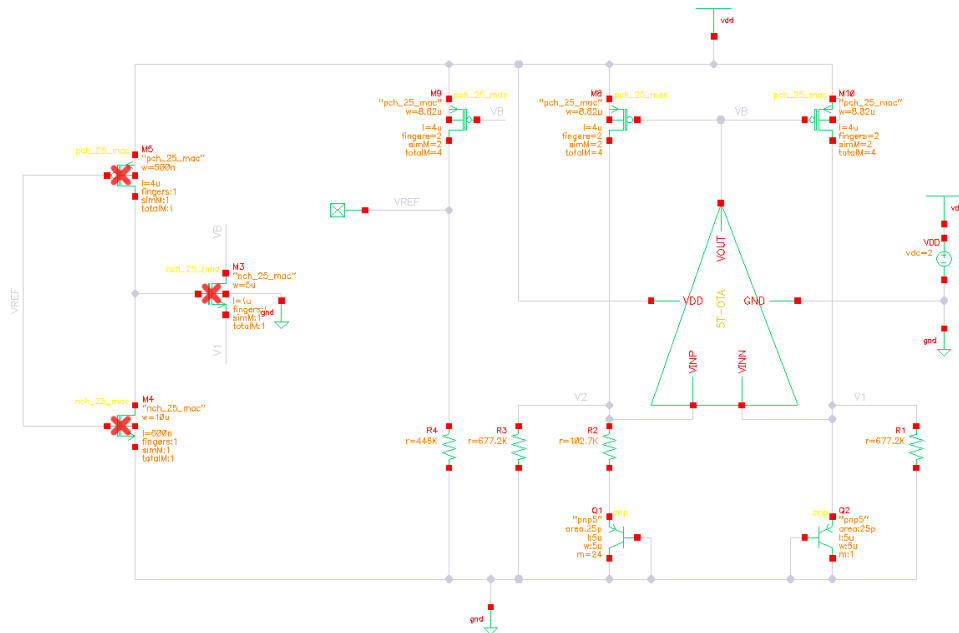


Figure 6: schematic

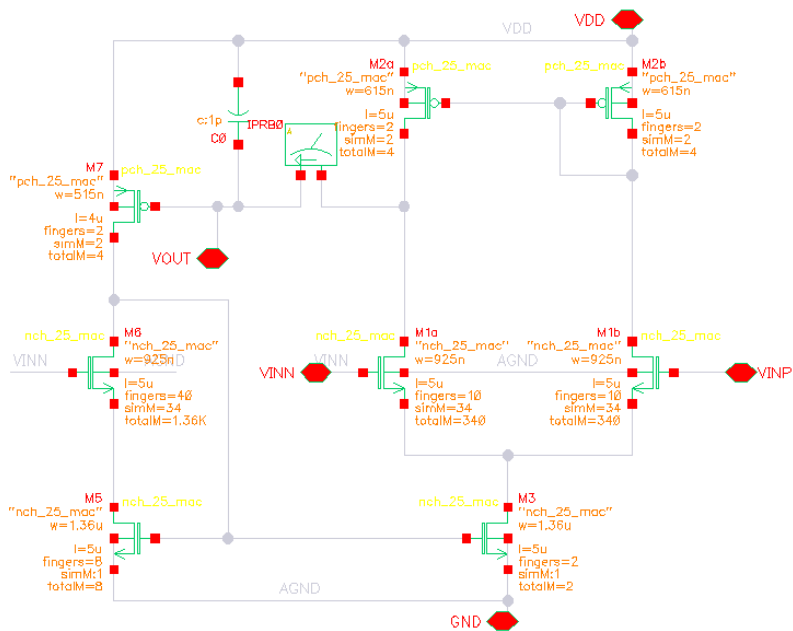


Figure 7: Error amplifier schematic

1. OP simulation

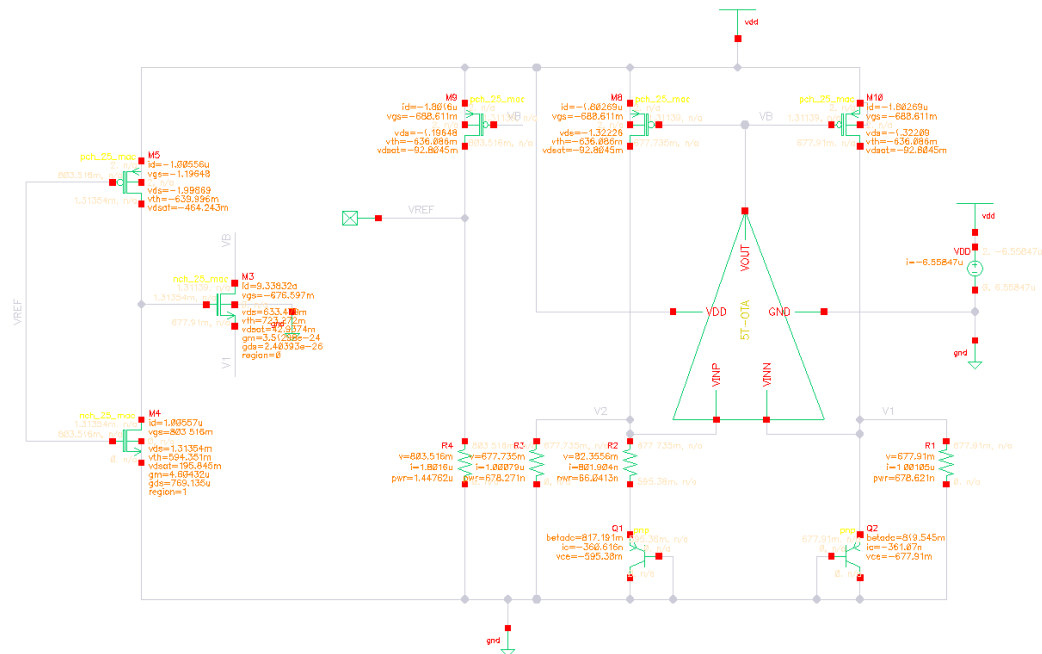


Figure 8: schematic with DC OP and node voltages annotated

Total power consumption = 6.6 μ A

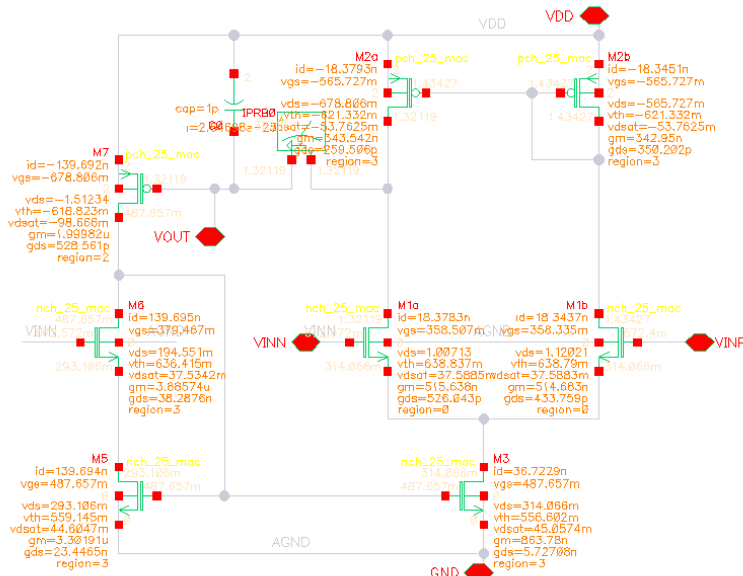


Figure 9: Error amplifier schematic with DC OP and node voltages annotated

2. DC temperature sweep simulation

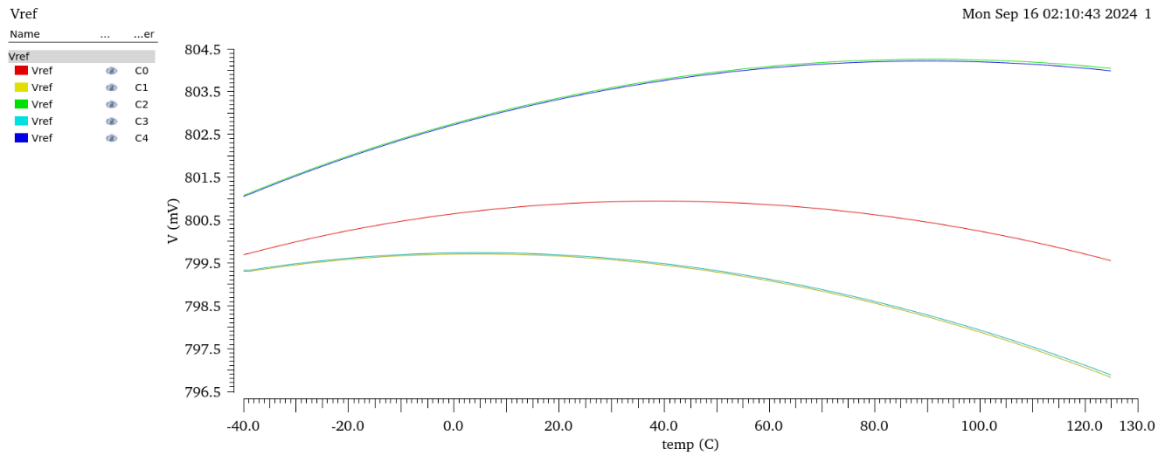


Figure 10: Vref across corners

3. Stability analysis

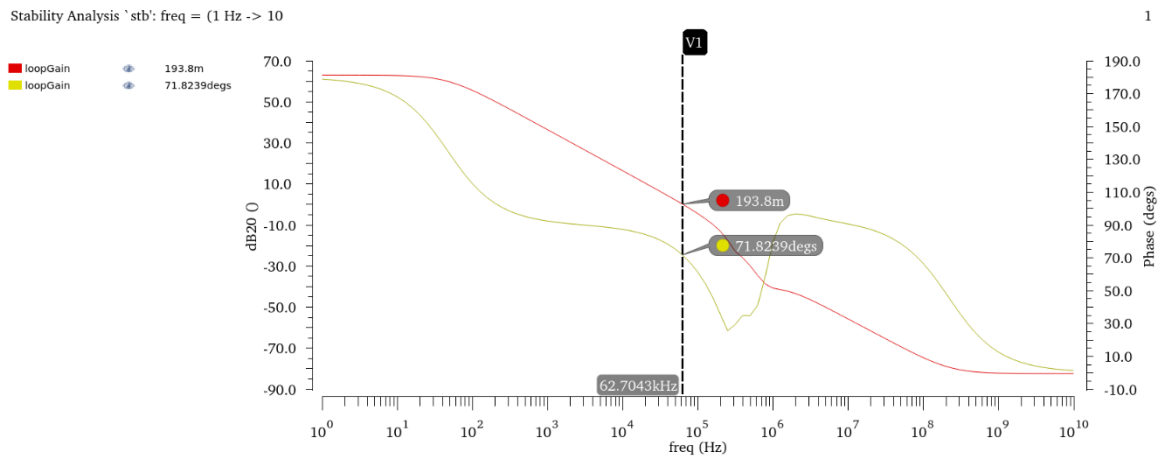


Figure 11: Gain crossover frequency

$$PM = 72^{\circ}$$

Part 4: Startup Circuit

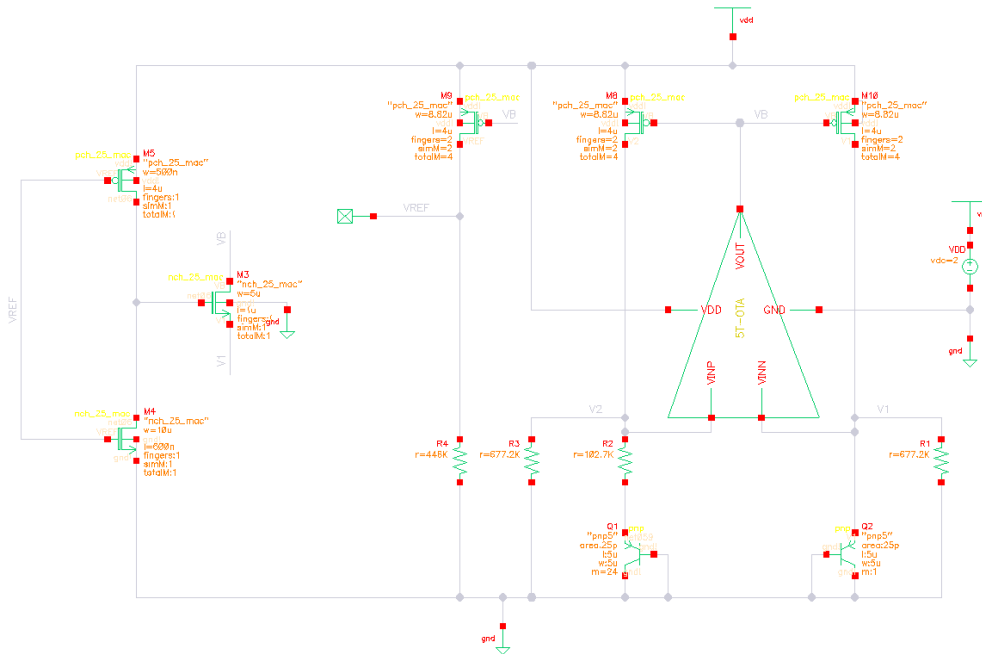


Figure 12: schematic

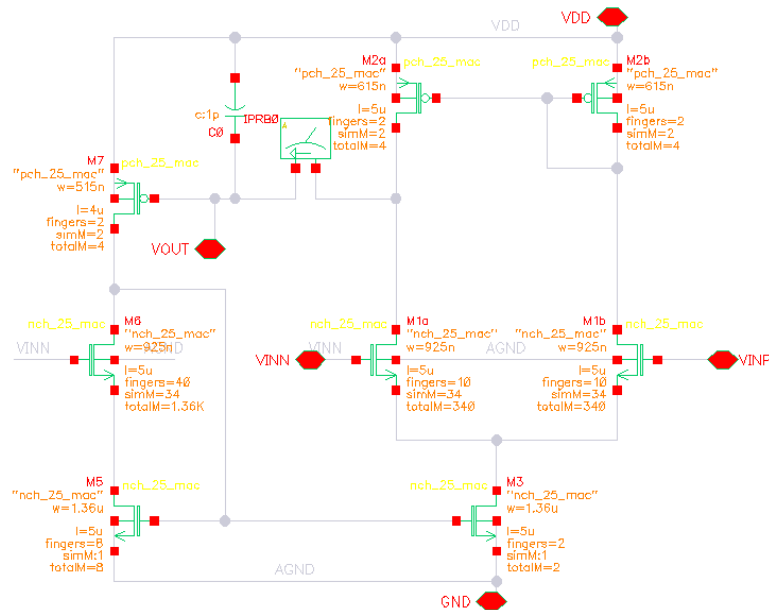


Figure 13: Error amplifier schematic

1. OP simulation

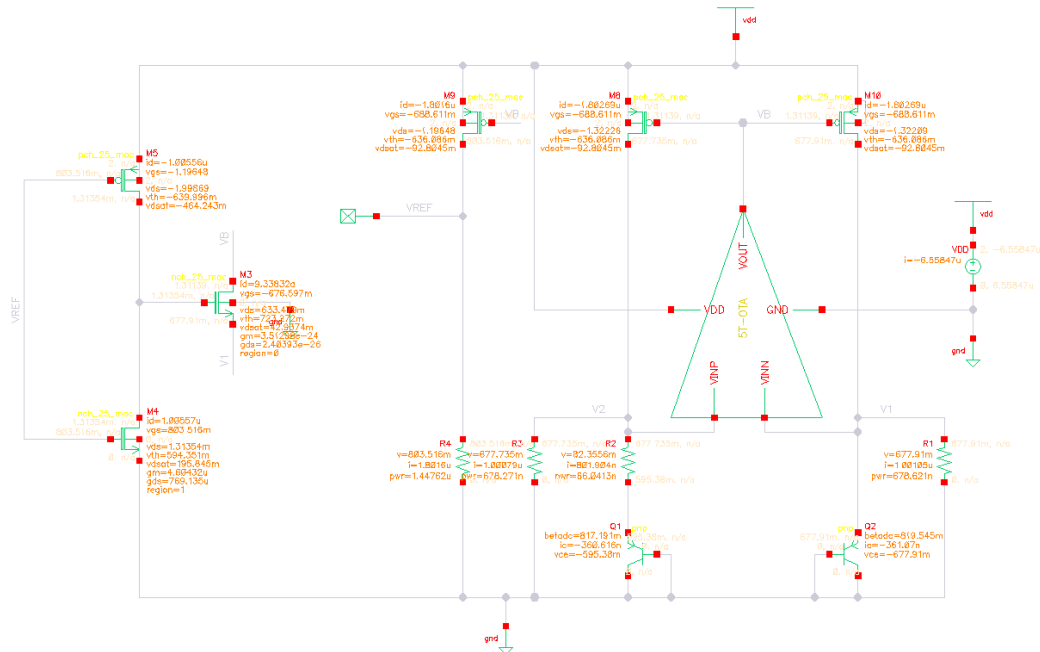


Figure 14: schematic with DC OP and node voltages annotated

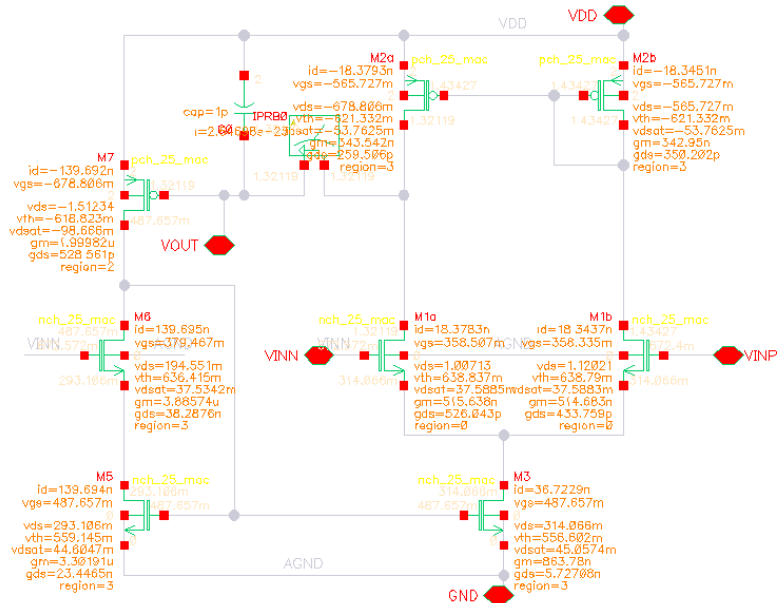


Figure 15: Error amplifier schematic with DC OP and node voltages annotated

2. Transient analysis supply ramp

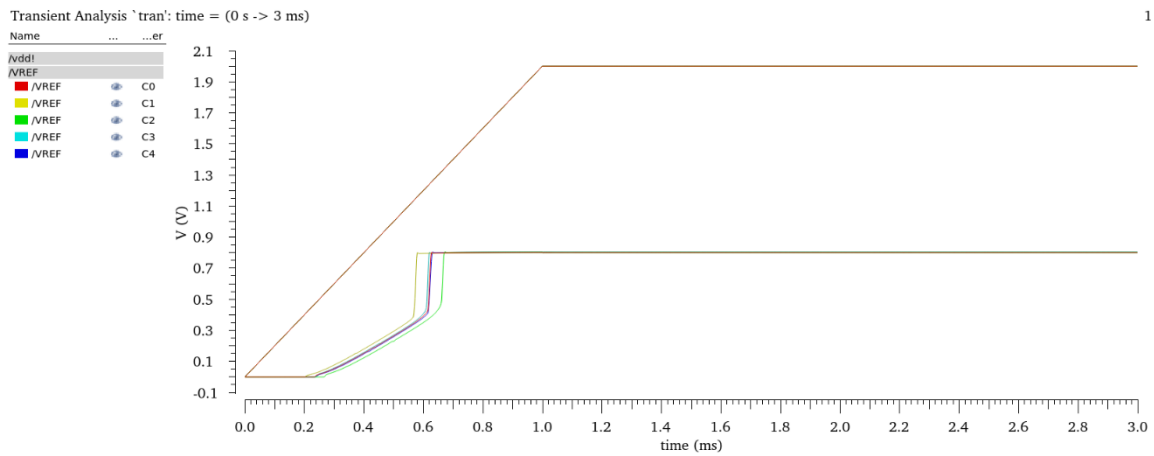


Figure 16: Transient Vref across corners at room temperature

Part 5: Achieved Specs

Spec	Required	Achieved
Supply Voltage	2 V	2 V
Change versus Temperature	< 1 mV	0.8 mV
Change across Corners	< 10 mV	6 mV
Current consumption	< 10 μ A	6.6 μ A
Phase margin	> 60°	72°

Table 2: Achieved specs