IEEE Egypt Section
Solid-State Circuits Society (SSCS) Chapter
2024 Student Design

The IEEE Egypt Section SSCS Chapter is holding a student design competition in the summer of 2024. This contest asks students to design a low-dropout regulator (LDO) with the specs given below. The operation of the circuit should be demonstrated by a report that includes the simulation results of all the specs and the transient response FOM_T. Monetary awards will be provided for the top three designs. The registration deadline is July 25, 2023. Please, register your team (1-4 students) by filling in **this form** before the deadline.

Eligibility Criteria

The competition is particularly intended for undergraduate students from public, private, or national universities within Egypt. Students graduating this year aren't qualified to enter the competition.

2024 Competition Technical Details

This competition aims to design and simulate a low-drop regulator (LDO) with the specifications given in Table 1 with the highest FOM. The LDO designs will be compared based on the FOM given that all the specifications are met.

Table 1. Required LDO Specifications

Parameter	Name	Min	Typ	Max	Units	Comments
Power Supply Voltage	V_{in}	2.4		3.5	V	
Output Voltage	V_{out}	0.85	1	1.25	V	Programmable with 12.5 mV step
Untrimmed Output Voltage Accuracy			±6		%	
Load Current	I_{out}	0.1		150	mA	
Vin Ramp Rate	dV_{in}/dt			0.2	mV/µs	
Rate of Iout Change	dI_{out}/dt			5	mA/ns	Load transient regulation for maximum load variation at maximum capacitance
Undershoot/Overshoot				50	mV/µs	
Load Capacitance	C_L			1	nF	
Power Supply Rejection at 1 MHz	PSR_{1MHz}	30			dB	
Power Supply Rejection at 10 MHz	PSR_{10MHz}	20			dB	
Line Regulation			2		mV/V	
Load Regulation			50		mV/A	

Instructions

1. Use a single supply DC voltage source.
2. Make sure that the phase margin is > 45° for all the negative feedback loops in your design.
3. Load transient profile from 1mA to 150mA within 30nsec and from 150mA to 1mA within 30nsec.
4. Transient response $FOM_T = \frac{C_L * \Delta V_{out} * I_q}{I_{L,max}^2}$
5. Assume any missing information.

Deliverables

You should submit a report that includes the simulation results of all the specifications in Table 1 in addition to the quiescent current and the FOM_T. The table should look like Table 2.

Table 2. Required Table Format

Parameter	Name	Specifications			Simulation Results			Units
		Min	Typ	Max	Min	Typ	Max	
Power Supply Voltage	V_{in}	2.4		3.5				V
Output Voltage	V_{out}	0.85	1	1.25				V
Untrimmed Output Voltage Accuracy			±6					%
Load Current	I_{out}	0.1		150				mA
Vin Ramp Rate	dV_{in}/dt			0.2				mV/µs
Rate of Iout Change	dI_{out}/dt			5				mA/ns
Undershoot/Overshoot				50				mV/µs

Load Capacitance	C_L			1				nF
Power Supply Rejection at 1 MHz	PSR_{1MHz}	30						dB
Power Supply Rejection at 10 MHz	PSR_{10MHz}	20						dB
Line Regulation			2					mV/V
Load Regulation			50					mV/A
Quiescent Current	I_q							µA
FOM_T								nSec

Timeline for submission

Students should submit a report summarizing their designs by September 15, 2024. The winners will be announced by September 30, 2024.

Awards

Gold Award: $350

Silver Award: $250

Bronze Award: $150