وَمَا أُوتِيتُمْ مِنَ الْعِلْمِ إِلَّا قَلِيلًا

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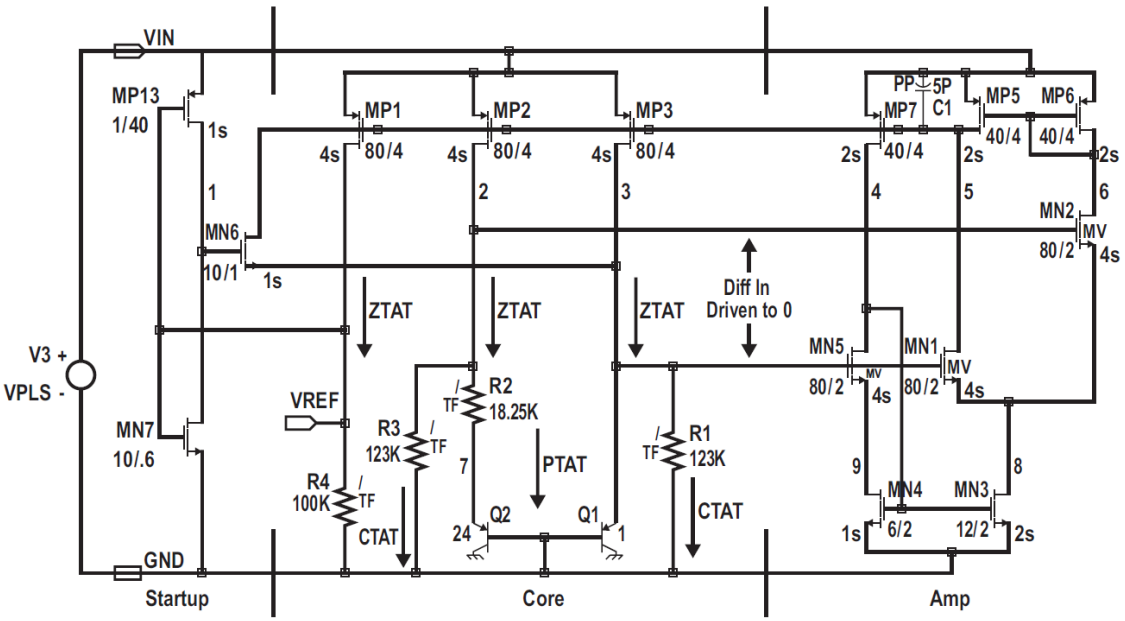
Analog IC Design
Design Challenge – 2024
Self-Biased Sub-1V Bandgap Reference Circuit

Intended Learning Objectives

In this design challenge you will:

- Learn how to design a sub-1V self-biased BGR circuit.
- Learn how to analyze and redesign an existing circuit.
- Learn how to size an analog circuit on your own.
- Learn how variations affect the circuit.
- Learn how to design a startup circuit.

Design Specs



It is required to redesign the BGR circuit shown above according to the following specifications.

Technology	65nm
Supply voltage	**2**
Corners	**Temp: -40 to 125** **Process: SS, SF, FS, FF**
Output voltage	**0.8**
Bias current	**< 10uA**
Phase margin	**> 60°**

Deliverables

- Part 1 (6 pts): BGR core circuit
  - Design the core BGR circuit only
  - Do not use a startup circuit
  - Replace the amplifier by a behavioral amplifier (VCVS)
  - Present the following:
    - Hand analysis
    - Schematics with device sizing.
    - Schematics with DC OP and node voltages annotated.
    - Vout vs temperature (-40 to 125) at TT, SS, FF, SF, FS
- Part 2 (4 pts): Replace the behavioral amplifier with the actual self-biased amplifier
  - Present the following:
    - Hand analysis
    - Schematics with device sizing.
    - Schematics with DC OP and node voltages annotated.
    - Vout vs temperature (-40 to 125) at TT, SS, FF, SF, FS
    - STB analysis results
  - From the closed loop specs, use hand analysis to find the worst-case open loop specs of the OTA (CLeff, DC Gain, UGF, PM).
- Part 3 (2 pts BONUS): Design the startup circuit
  - Present the following:
    - Schematics with device sizing.
    - Schematics with DC OP and node voltages annotated.
    - Transient simulation of Vout vs time
      - Apply VDD as a ramp from (0,0) to (1ms,2V).

Acknowledgements

Thanks to all who contributed to these labs. If you find any errors or have suggestions concerning these labs, contact Hesham.omran@eng.asu.edu.eg.