

Self-Biased Sub-1V Bandgap Reference Circuit

Bilal Ramadan

Supervisor: Dr. Hesham Omran

Table of Contents

Part 1: Design Required Specs.....	3
Part 2: BGR Core Circuit	3
1. OP simulation	4
2. DC temperature sweep simulation.....	5
Part 3: Error Amplifier.....	6
1. OP simulation	7
2. DC temperature sweep simulation.....	8
3. Stability analysis.....	8
Part 4: Startup Circuit	9
1. OP simulation	10
2. Transient analysis supply ramp	11
Part 5: Achieved Specs	11

Tables

Table 1: Required specs.....	3
Table 2: Achieved specs	11

Table of Figures

Figure 1: schematic	3
Figure 2: Error amplifier behavioral model.....	4
Figure 3: schematic with DC OP and node voltages annotated	4
Figure 4: Vref vs temperature with 0.8 mV change	5
Figure 5: Vref across corners with 6 mV change	5
Figure 6: schematic	6
Figure 7: Error amplifier schematic	6

Figure 8: schematic with DC OP and node voltages annotated	7
Figure 9: Error amplifier schematic with DC OP and node voltages annotated.....	7
Figure 10: Vref across corners	8
Figure 11: Gain crossover frequency	8
Figure 12: schematic	9
Figure 13: Error amplifier schematic	9
Figure 14: schematic with DC OP and node voltages annotated	10
Figure 15: Error amplifier schematic with DC OP and node voltages annotated.....	10
Figure 16: Transient Vref across corners at room temperature	11

Part 1: Design Required Specs

Technology	65 nm CMOS
Supply Voltage	2 V
Change versus Temperature	< 1 mV
Change across Corners	< 10 mV
Current consumption	< 10 μ A
Phase margin	> 60°

Table 1: Required specs

The Design will be on three phases as follows:

Part 2: BGR Core Circuit

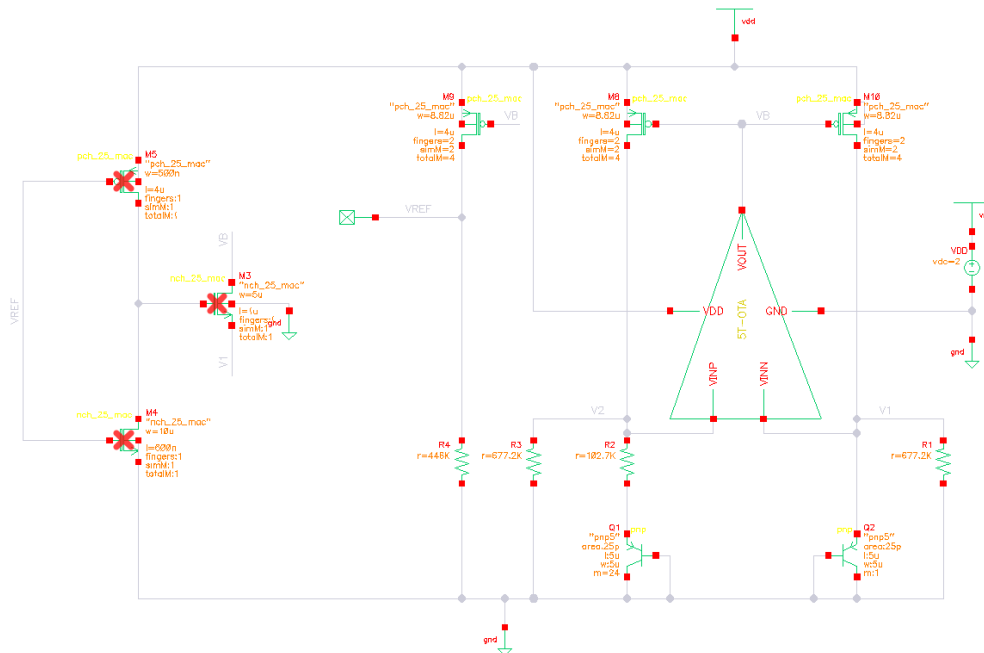


Figure 1: schematic

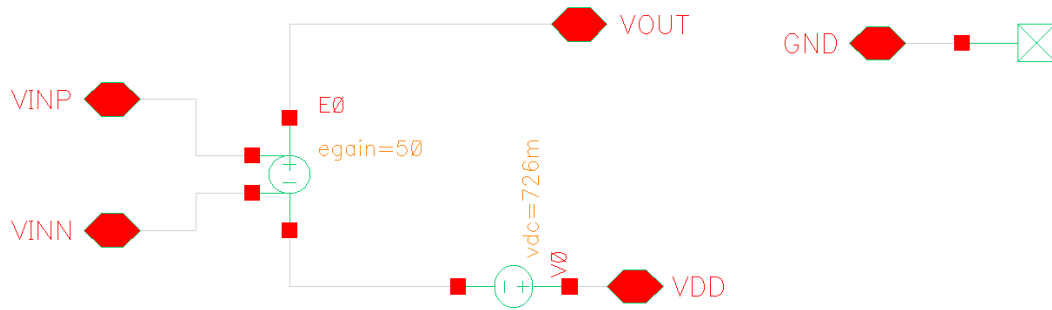


Figure 2: Error amplifier behavioral model

1. OP simulation

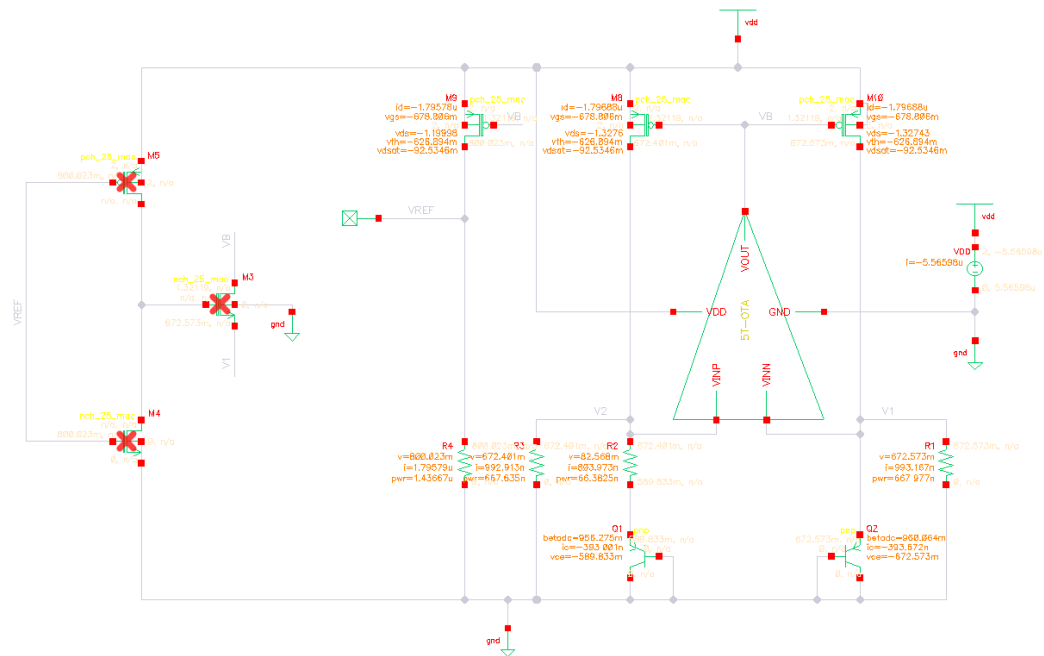


Figure 3: schematic with DC OP and node voltages annotated

2. DC temperature sweep simulation

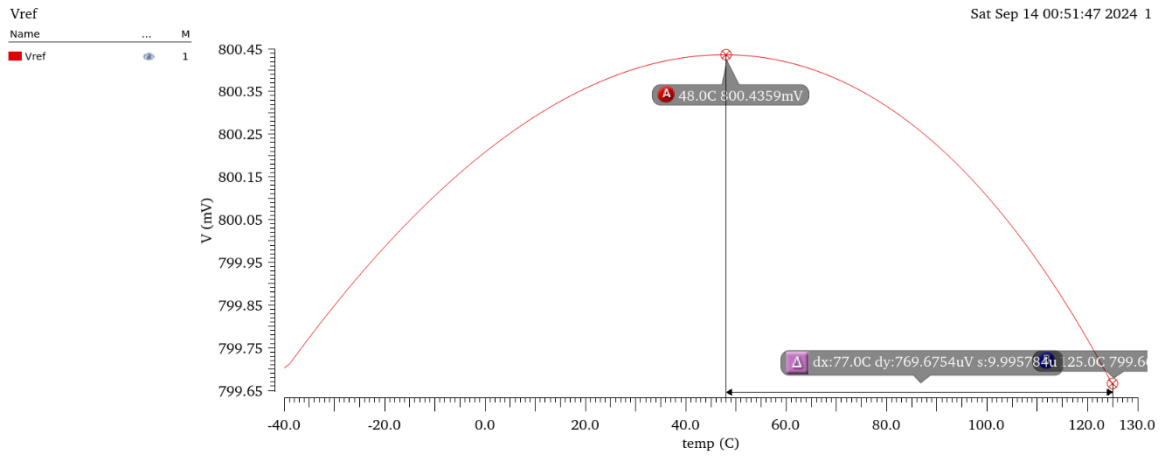


Figure 4: Vref vs temperature with 0.8 mV change

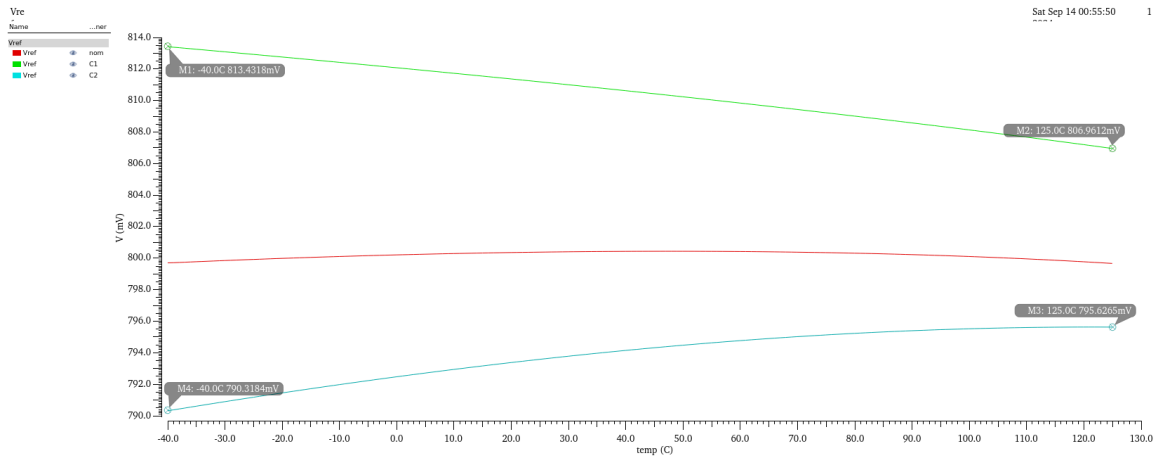


Figure 5: Vref across corners with 10 mV change

Part 3: Error Amplifier

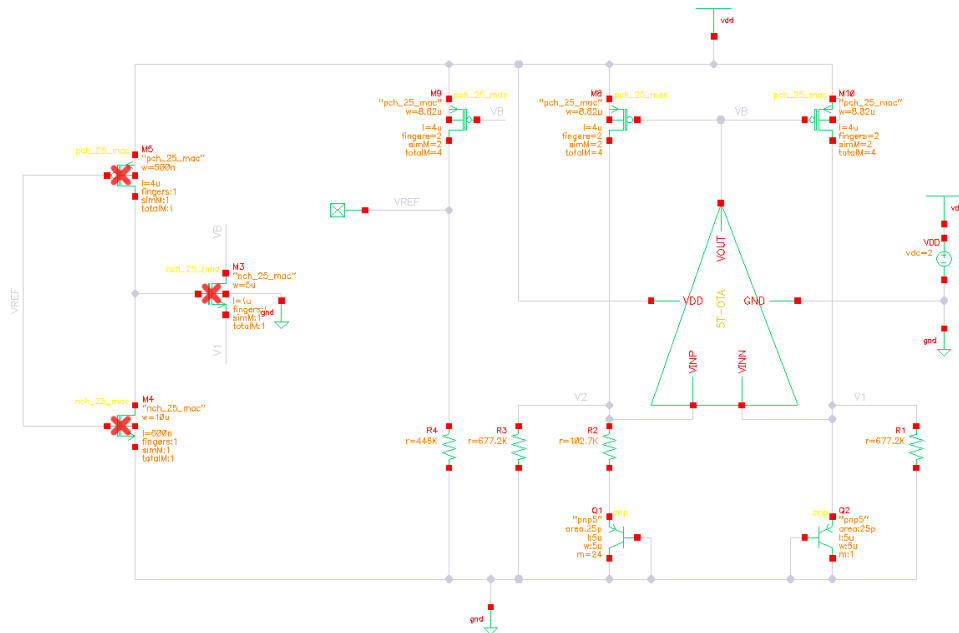


Figure 6: schematic

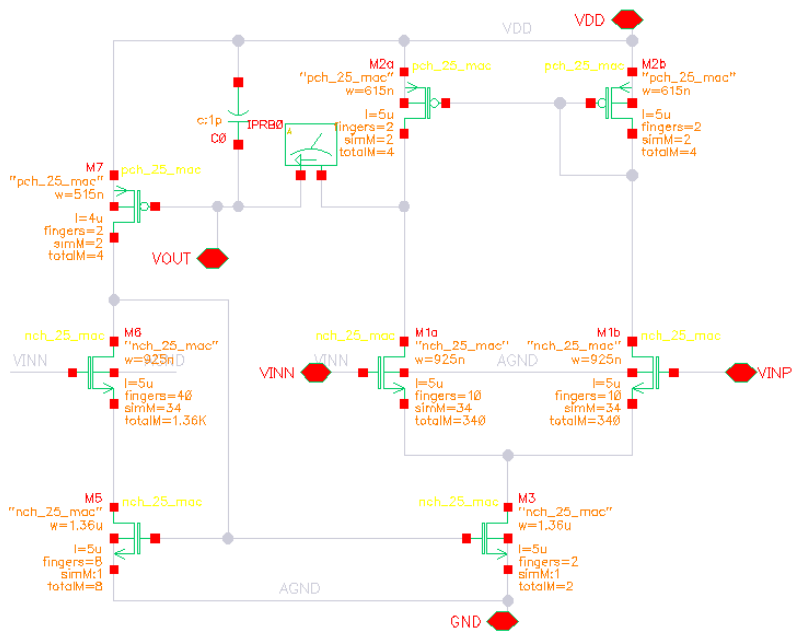


Figure 7: Error amplifier schematic

1. OP simulation

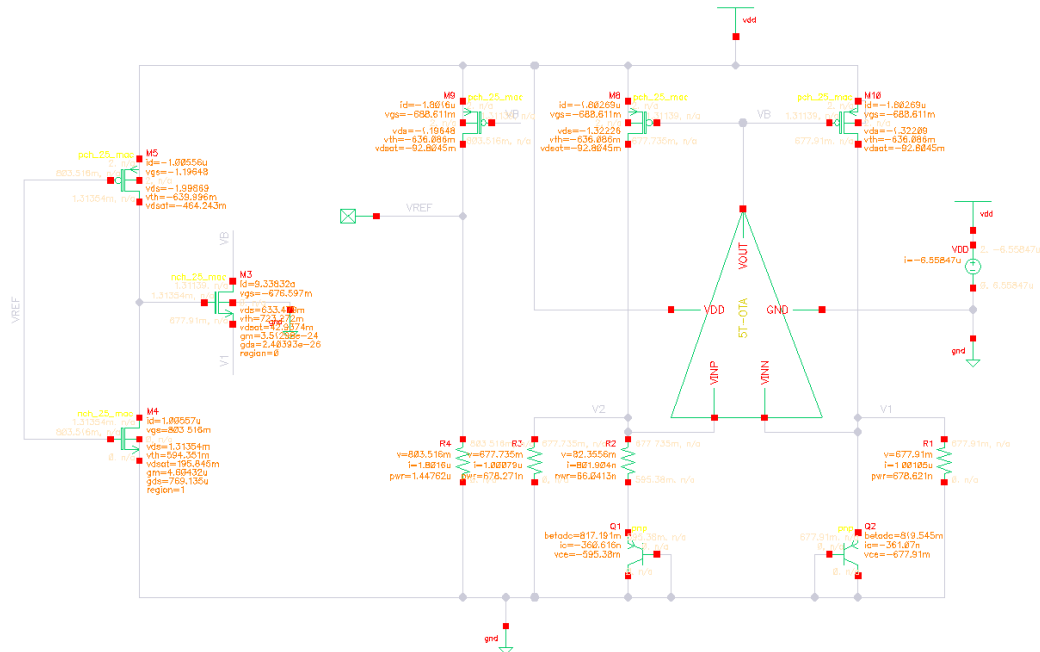


Figure 8: schematic with DC OP and node voltages annotated

Total power consumption = 6.6 μ A

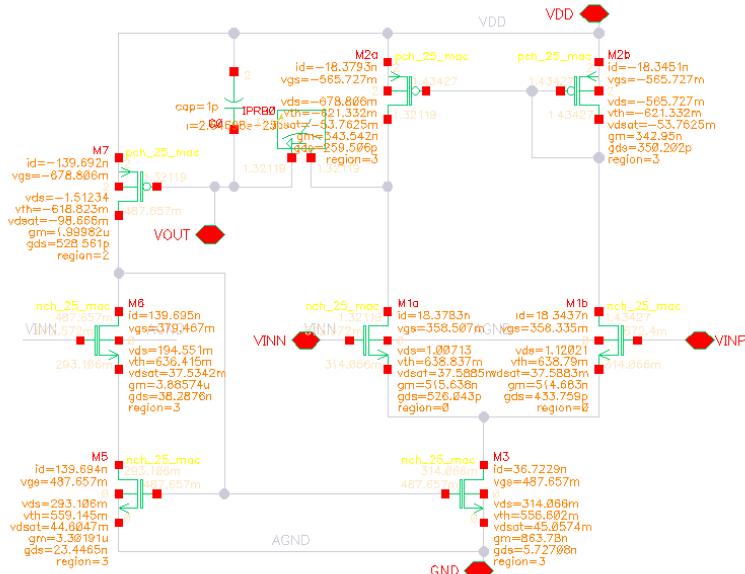


Figure 9: Error amplifier schematic with DC OP and node voltages annotated

2. DC temperature sweep simulation

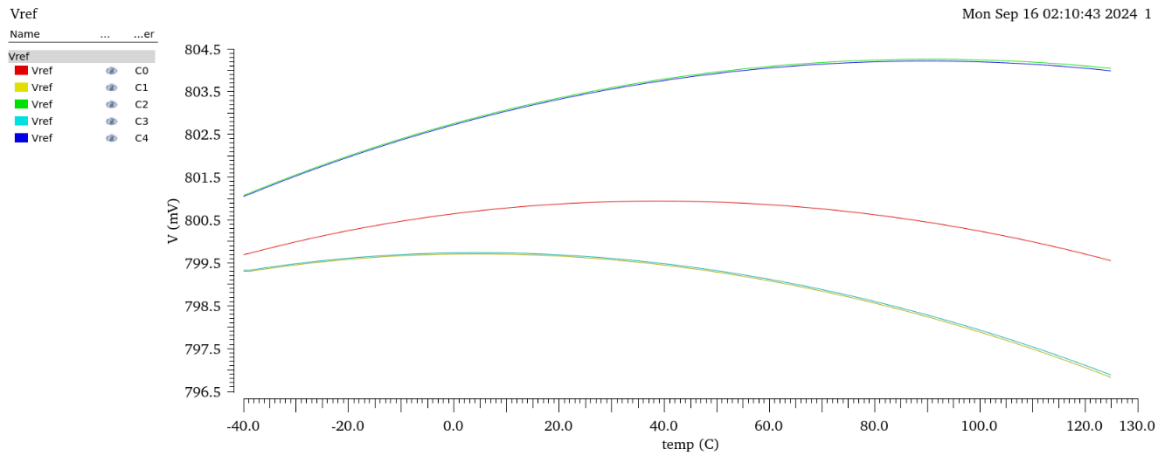


Figure 10: Vref across corners

3. Stability analysis

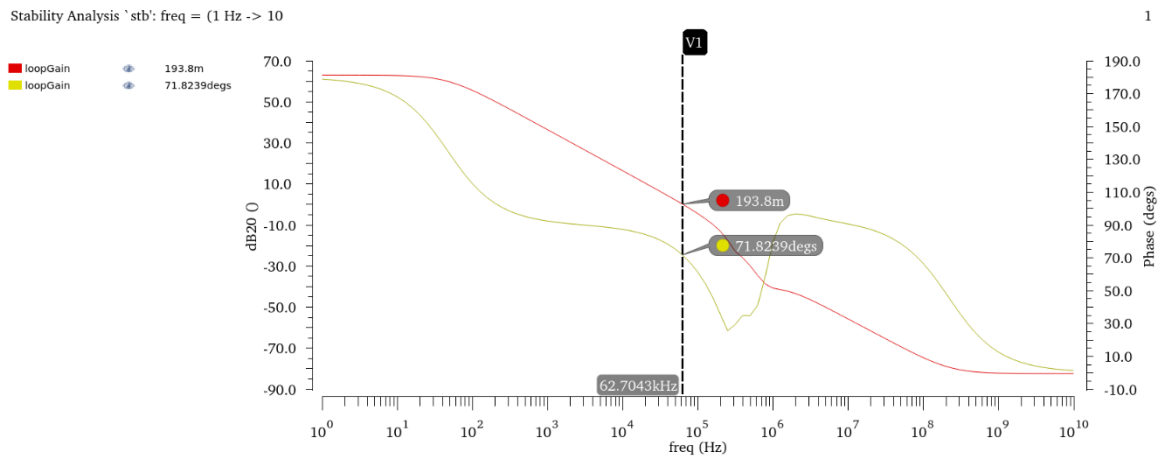


Figure 11: Gain crossover frequency

$$PM = 72^{\circ}$$

Part 4: Startup Circuit

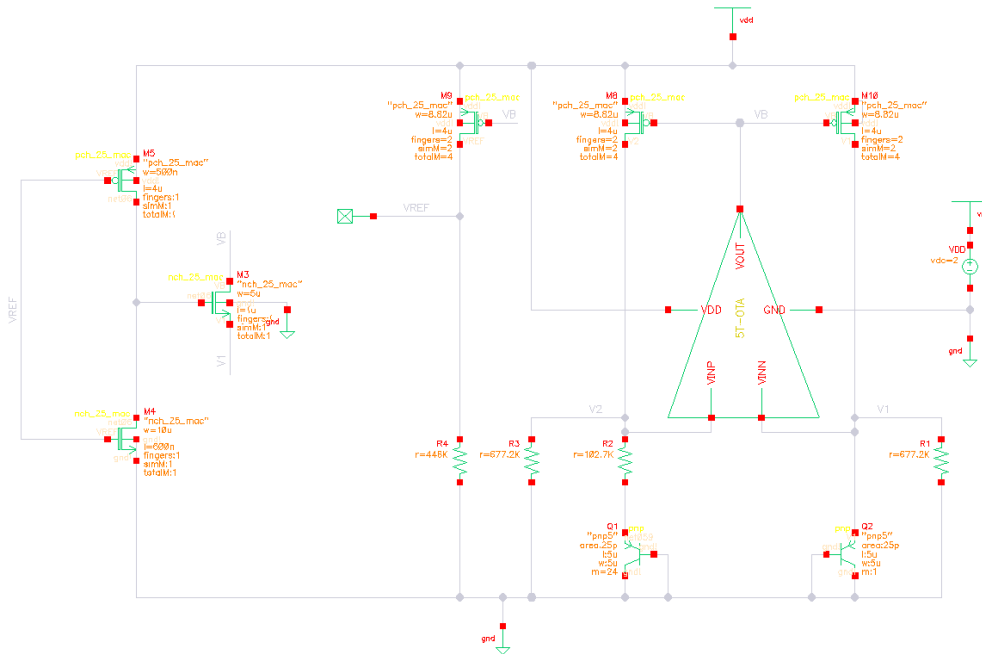


Figure 12: schematic

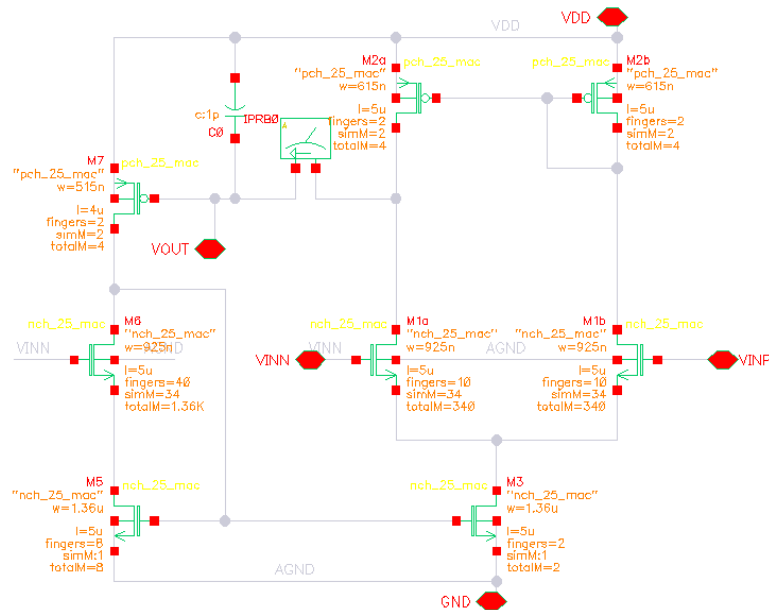


Figure 13: Error amplifier schematic

1. OP simulation

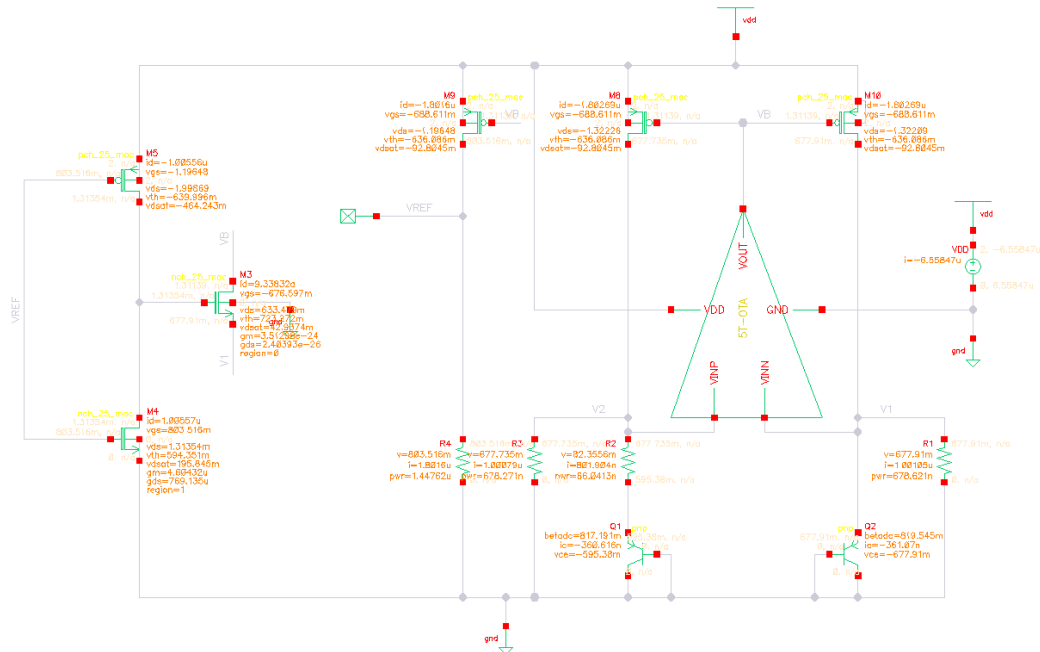


Figure 14: schematic with DC OP and node voltages annotated

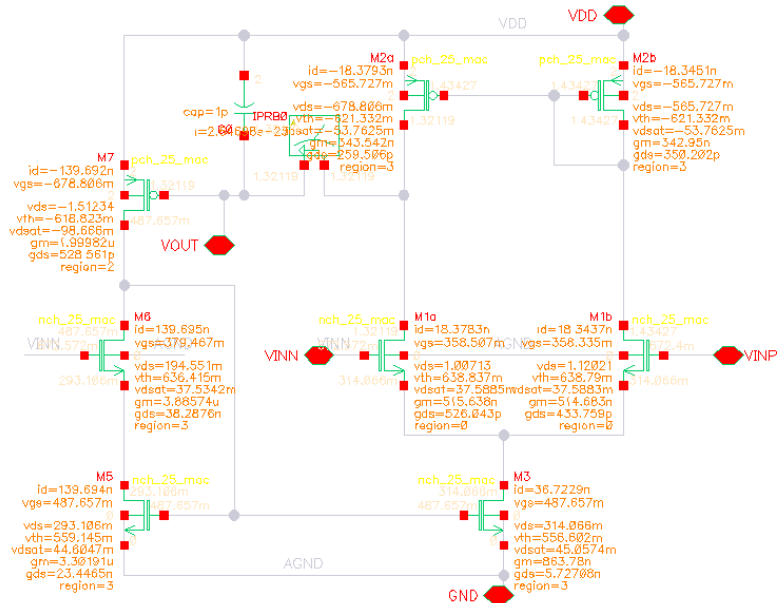


Figure 15: Error amplifier schematic with DC OP and node voltages annotated

2. Transient analysis supply ramp

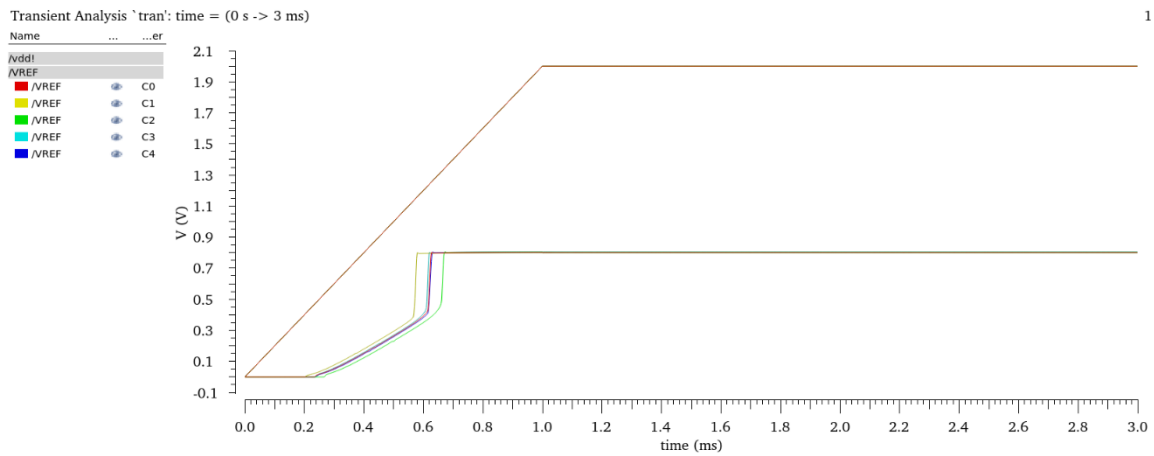


Figure 16: Transient V_{ref} across corners at room temperature

Part 5: Achieved Specs

Spec	Required	Achieved
Supply Voltage	2 V	2 V
Change versus Temperature	$< 1\text{ mV}$	0.8 mV
Change across Corners	$< 10\text{ mV}$	10 mV
Current consumption	$< 10\text{ }\mu\text{A}$	$6.6\text{ }\mu\text{A}$
Phase margin	$> 60^\circ$	72°

Table 2: Achieved specs