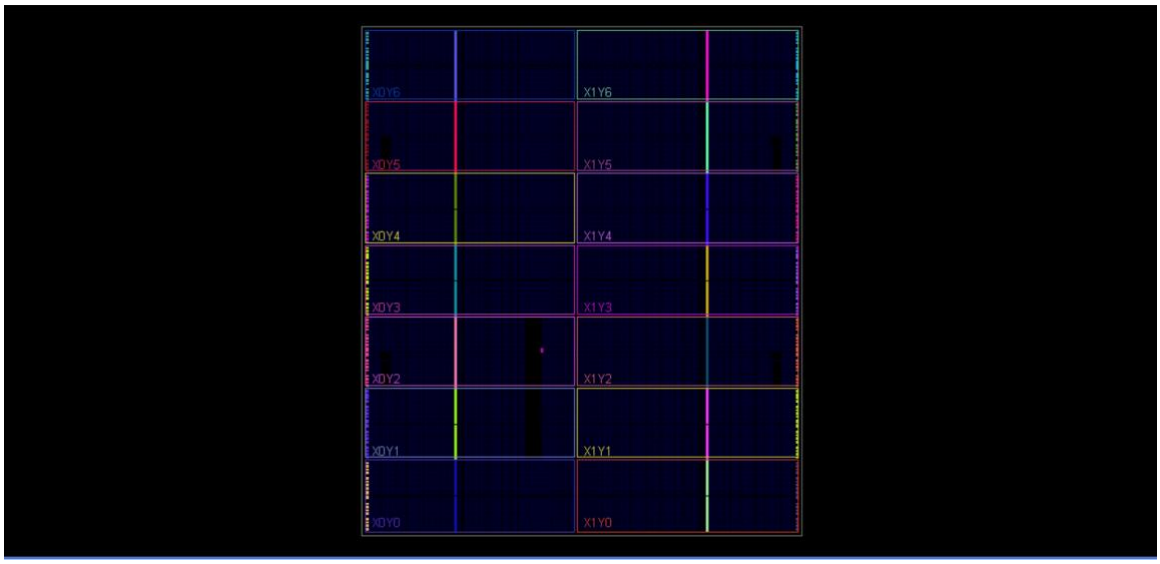
Bilal Ramadan

DSP48A1

FPGA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X1Y5
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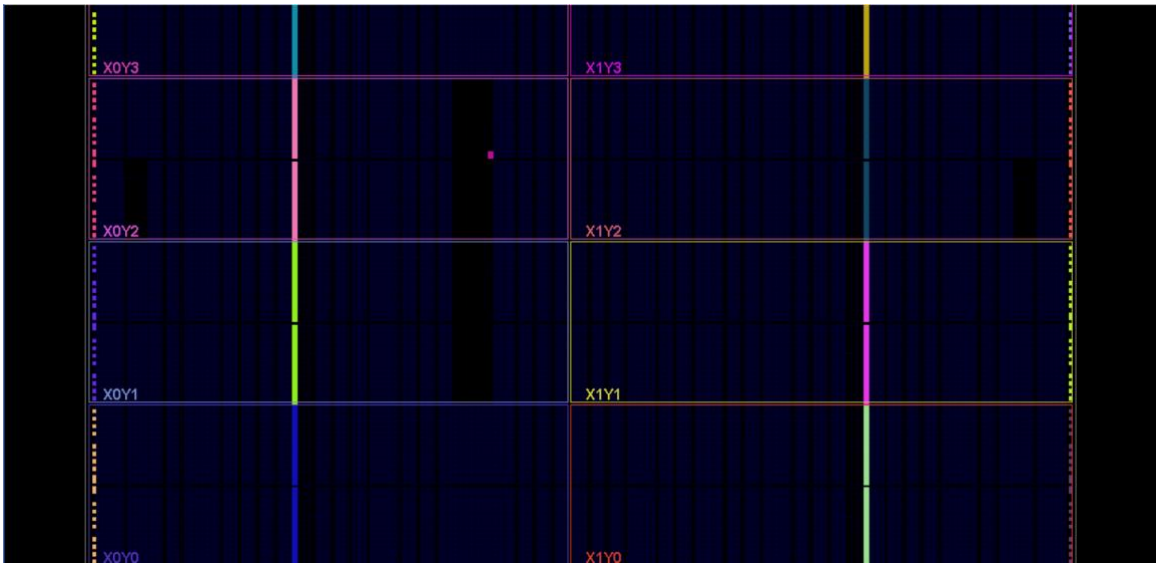
X0Y3
X1Y3
X0Y2
X1Y2
X0Y1
X1Y1
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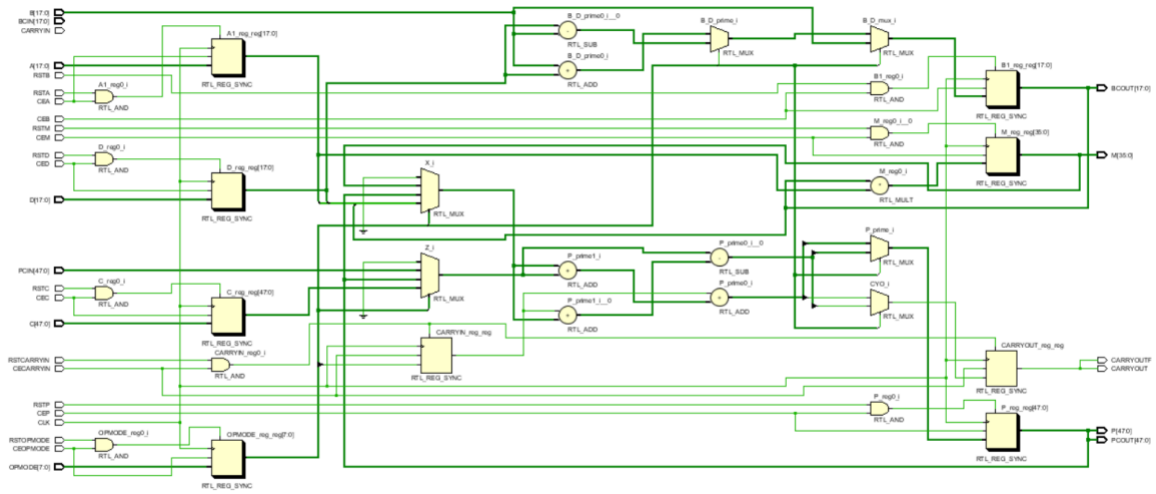
X1Y0

Schematic



Timing and bitstream errors