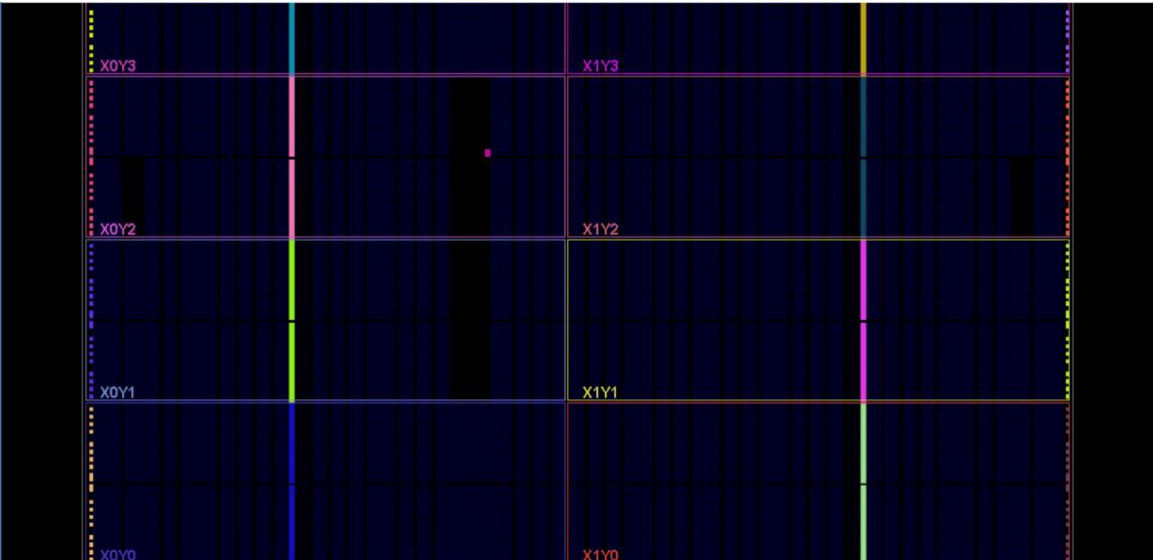
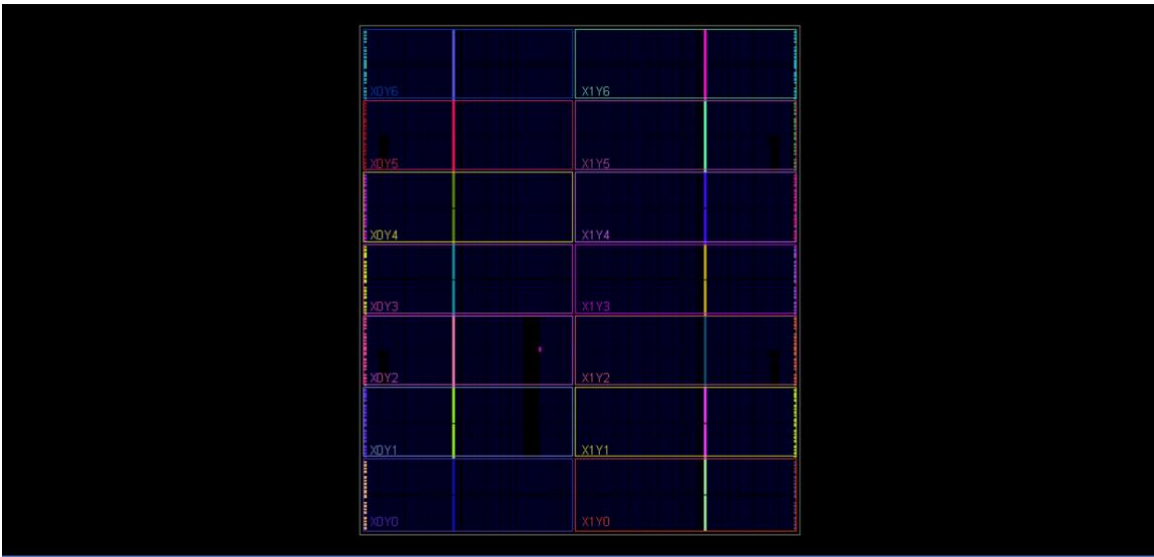


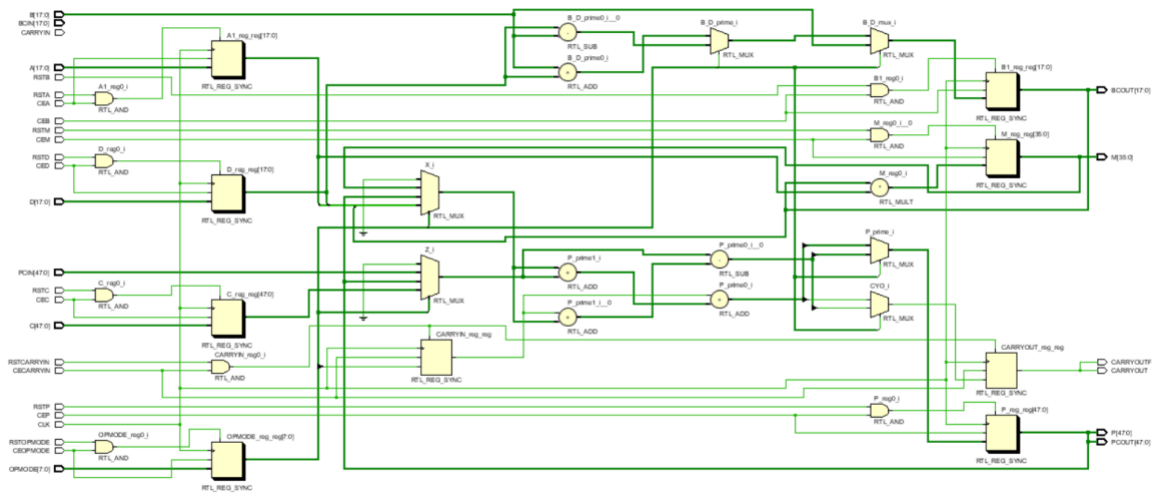
Bilal Ramadan

DSP48A1

FPGA



Schematic



Timing and bitstream errors

Design Timing Summary			
Setup	Hold	Pulse Width	
Worst Negative Slack (WNS): inf	Worst Hold Slack (WHS): inf	Worst Pulse Width Slack (WPWS): NA	
Total Negative Slack (TNS): 0.000 ns	Total Hold Slack (THS): 0.000 ns	Total Pulse Width Negative Slack (TPWS): NA	
Number of Failing Endpoints: 0	Number of Failing Endpoints: 0	Number of Failing Endpoints: NA	
Total Number of Endpoints: 693	Total Number of Endpoints: 693	Total Number of Endpoints: NA	
There are no user specified timing constraints.			

17 Infos, 45 Warnings, 2 Critical Warnings and 0 Errors encountered.

synth_design completed successfully

synth_design: Time (s): cpu = 00:01:26 ; elapsed = 00:01:59 . Memory (MB): peak = 1028.789 ; gain = 729.371

WARNING: [Constraints 18-5210] No constraint will be written out.

INFO: [Common 17-1381] The checkpoint 'E:/Assignments/Digital/Project/project.runs/synth_1/DSP48A1.dcp' has been generated.

INFO: [runtcl-4] Executing : report_utilization -file DSP48A1_utilization_synth.rpt -pb DSP48A1_utilization_synth.pb

report_utilization: Time (s): cpu = 00:00:00 ; elapsed = 00:00:00.523 . Memory (MB): peak = 1028.789 ; gain = 0.000