Two-Stage Miller Design

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Part 1: OTA Design

1. Desired specs

Technology	$180\ nm\ CMOS$
Supply Voltage	$1.8\ V$
Static gain error	$\leq 0.05\ \%$
CMRR @DC	$\geq 74\ dB$
Phase Margin	$\geq 70°$
OTA current consumption	$\leq 60\ \mu A$
CMIR - high	$\geq 1\ V$
CMIR - low	$\leq 0.2\ V$
Output swing	$0.2\ V - 1.6\ V$
Load	$5\ pF$
Buffer closed loop rise time (10% to 90%)	$\leq 70\ ns$
Slew rate	$5\ V/\mu s$

Table 1: Desired Specs

At first, we need to identify the topology.

Since the CMIR is near to GND, therefore the topology we will use in the Two-Stage Miller OTA is the PMOS for the 1st stage input pair and NMOS in the 2nd input stage to match VGS in order to avoid the zero systematic offset.

2. OTA Schematic

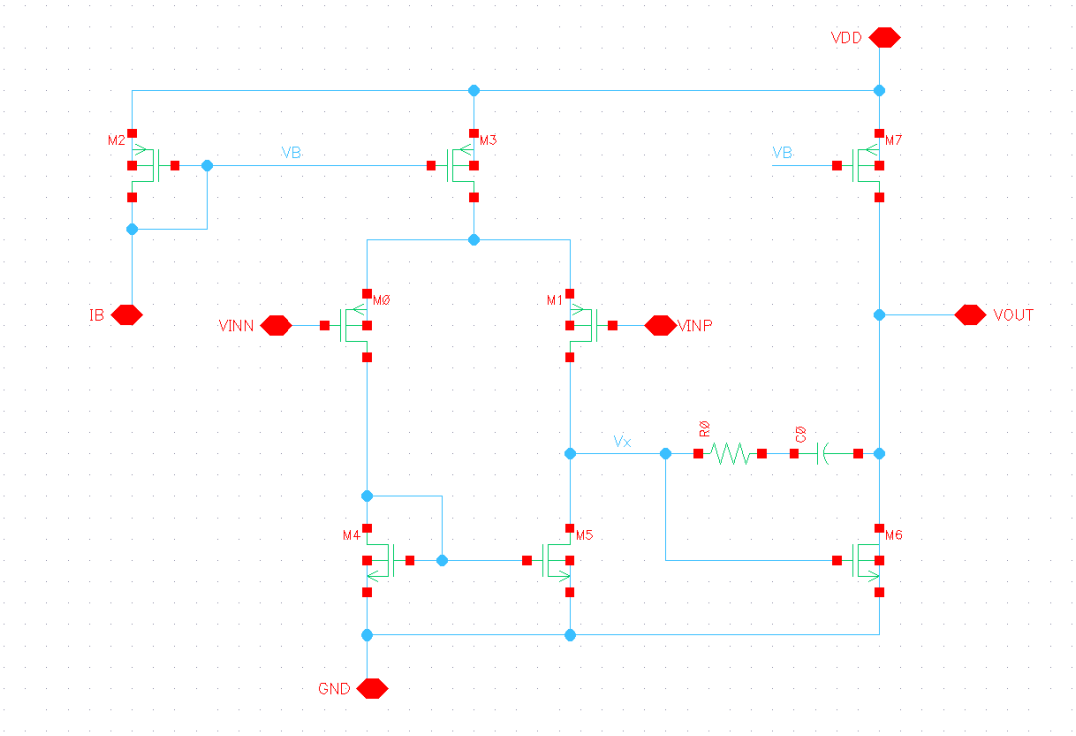

Figure 1:OTA schematic

3. OTA Devices Sizing

Device	M_2 *(input CM)*	M_3 *(tail CM)*	$M_{0,1}$ $\left(\begin{matrix}1^{st}stage\\input\ pair\end{matrix}\right)$	$M_{4,5}$ *(load CM)*	M_6 $\left(\begin{matrix}2^{nd}\ input\\stage\end{matrix}\right)$	M_7 $\left(\begin{matrix}2^{nd}\ stage\\CM\ load\end{matrix}\right)$
W	13.24 μm	18.543 μm	26.77 μm	17.354 μm	126.38 μm	61.34 μm
L	350 nm	350 nm	720 nm	1.3 μm	1.3 μm	350 nm
g_m	140 μS	177.8 μS	95.25 μS	104.78 μS	762 μS	646.52 μS
I_D	10 μA	12.7 μA	6.35 μA	6.35 μA	46.18 μA	46.18 μA
g_m/I_D	14	14	15	16.5	16.5	14
$\lvert V_{DSsat}\rvert$	122.4 mV	121.7 mV	105 mV	92.8 mV	92.8 mV	122.4 mV
V_{ov}	75.95 mV	75.95 mV	62.2 mV	31.6 mV	31.6 mV	75.95 mV
V^*	143 mV	143 mV	133 mV	121 mV	121 mV	143 mV

Table 2: OTA Devices Sizing

Part 2:Open −loop OTA simulation

1. OP simulation

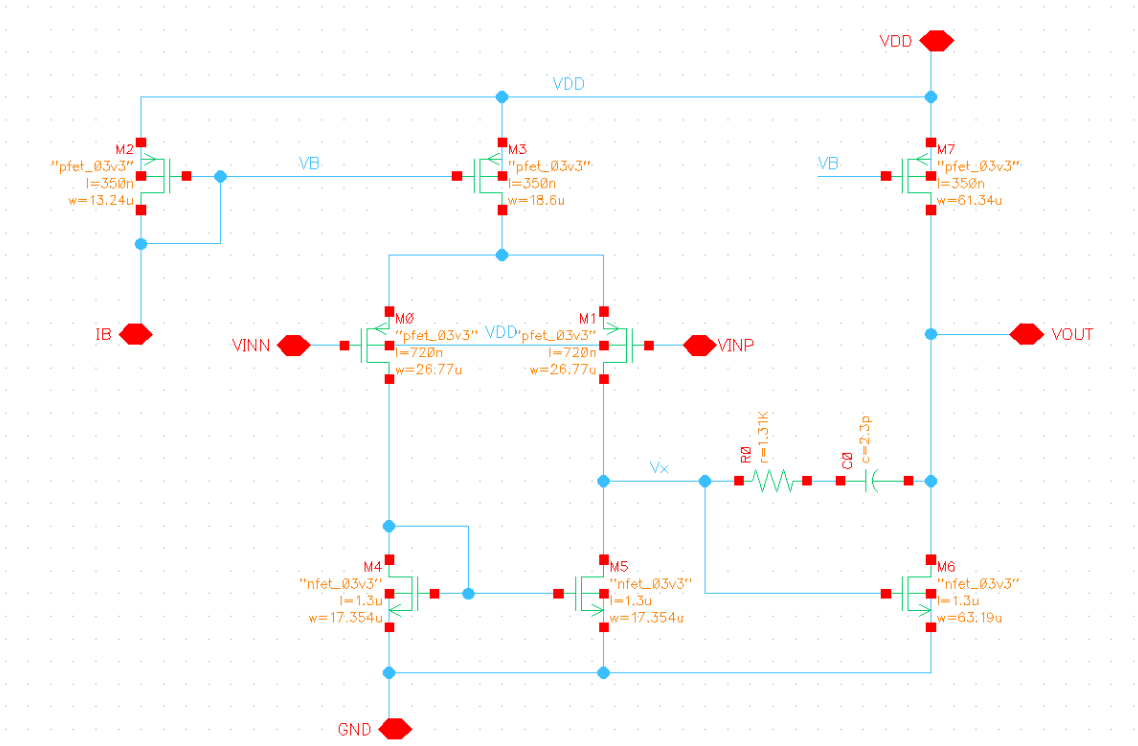

Figure 2: Final design schematic

Note: M6 has multiplier of 2.

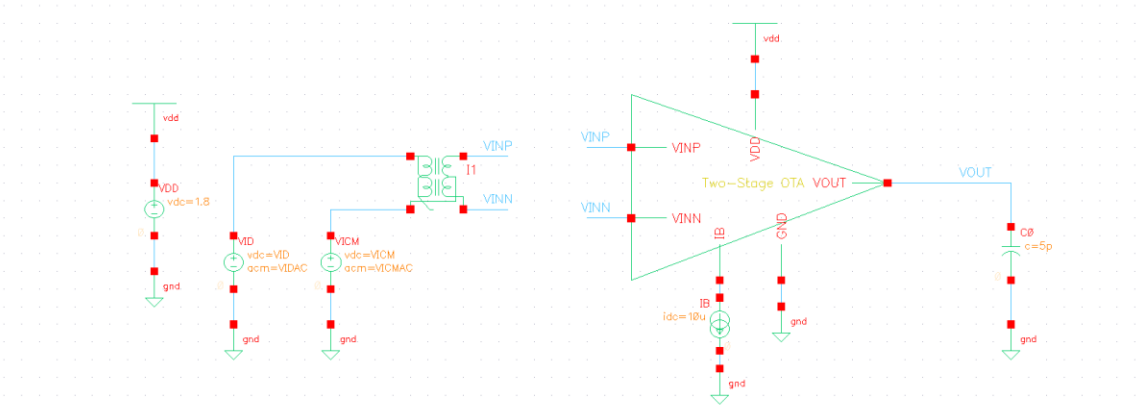

Figure 3: Open-loop testbench

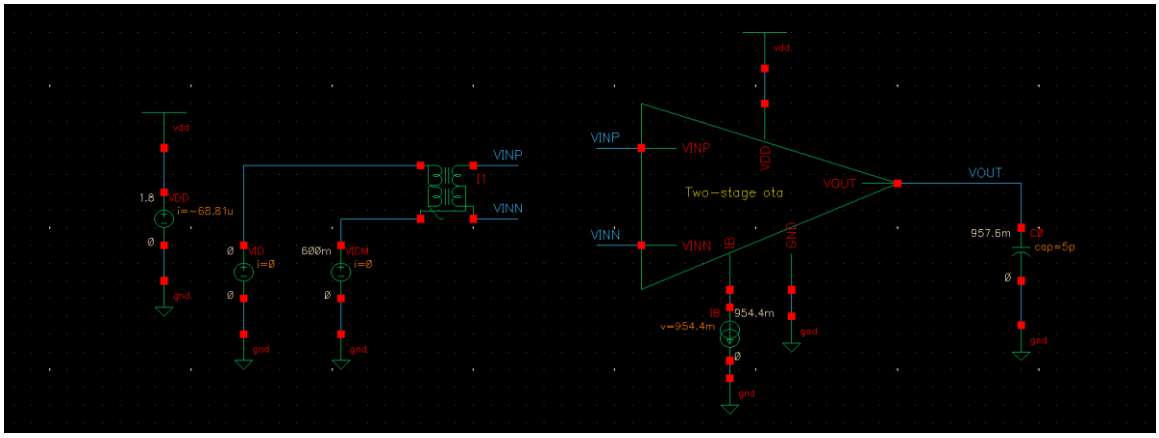

Figure 4: bias circuit with DC node voltages annotated

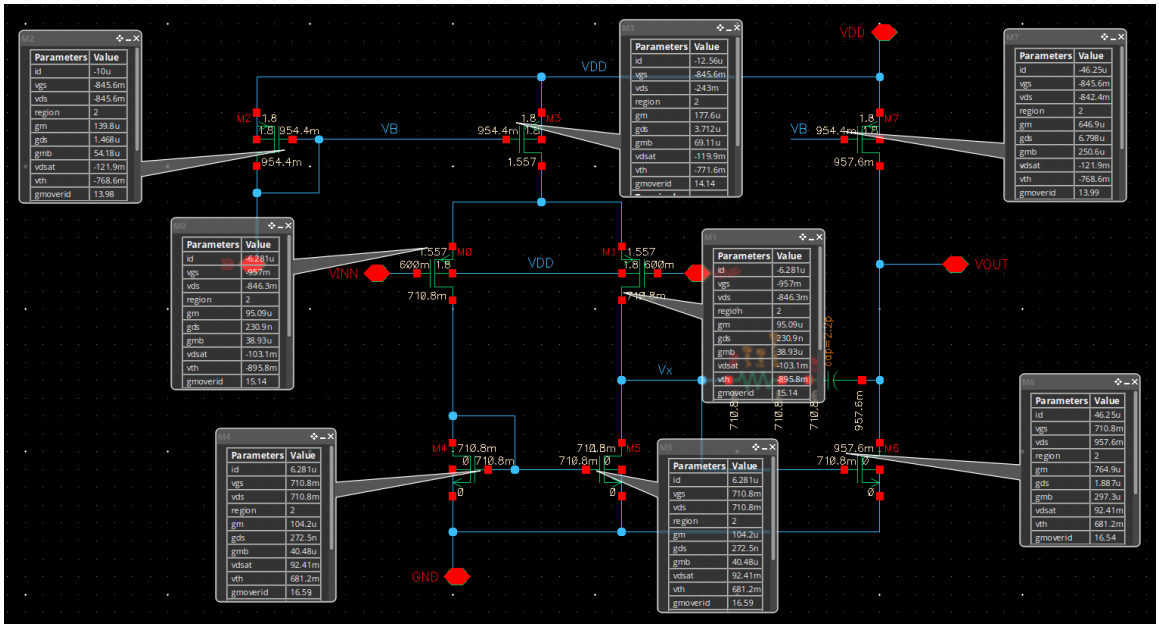

Figure 5: OTA schematic with DC node voltages and OP parameters annotated

- All devices are in sat.
- If we check the branches currents we will find out that it's near from what we expected as we took VDS into consideration in the ID/W charts. Also, for that reason, $V_{outdc} = 957.6\ mV$ close to 0.9 V we targeted.
- The current consumption spec is achieved ($58.8\ \mu A$).
- The current and gm in the input pair exactly equal, due to the absence of differential signal and dc offset and no mismatch between the devices.
- The dc level of $V_x = V_{GS4}$ as it follows the mirror node at zero differential input to balance the current in the two branches.

- The dc level of V_{out} is 957.6 mV as it's a high impedance node so it's ill-defined but we recovered that problem by taking VDS into consideration in the ID/W charts.

2. Diff small signal ccs

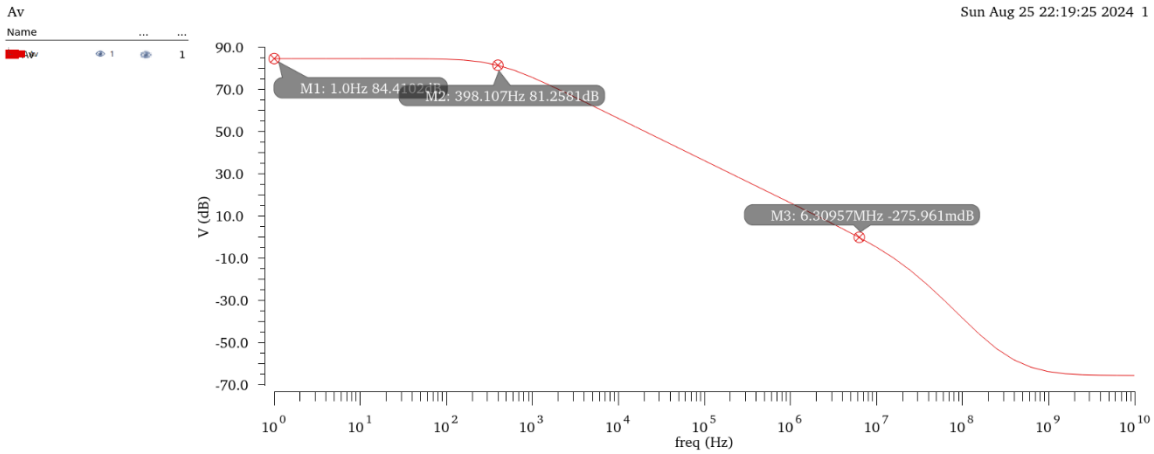

Figure 6: diff gain bode plot (magnitude)

Test	Output	Nominal	Spec
ITI_labs:lab9_TB1:1	Av	16.62k	> 2k
ITI_labs:lab9_TB1:1	Av in dB	84.41	> 66
ITI_labs:lab9_TB1:1	BW	385.4	
ITI_labs:lab9_TB1:1	Fu	6.19M	> 5M
ITI_labs:lab9_TB1:1	GBW	6.418M	

Figure 7: diff small signal results

$$DC\ diff\ gain = g_{m0,1}(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7}),$$

$$BW \approx \frac{1}{2\pi(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7})C_c}, GBW = \frac{g_{m0,1}}{2\pi C_c}$$

Spec	*Simulation*	*Hand analysis*
DC diff gain	84.41 dB	84.42 dB
BW	385.4 Hz	391 Hz
GBW	6.4 MHz	6.6 MHz

Table 3: simulation vs hand analysis

- UGF and GBW are almost the same and that's an indicator to a good PM.
- BW & GBW hand analysis are different from the simulation as the parasitic caps are large due to the large sizes and they are not taken into consideration in the hand analysis.

- The dc diff gain is way larger than the spec as the input pair suffer from body effect so we biased them at large g_m/I_D to make their V_{GS} smaller to get near from $CMIR_{high}$ spec and larger g_m/I_D for the 2nd stage NMOS to meet the PM spec (ratios of $g_m \geq 8$) as we can't use small current in the 1st stage due to the SR spec and can't use larger current in the 2nd stage due to current consumption spec. And the load CM has high gm/gds to meet the gain we need at the 1st stage to meet the CMRR which are matched to the 2nd stage NMOS to avoid the systematic zero offset. And the three upper PMOS devices are matched as they are CMs and the one in the 1st stage has condition on g_{ds} to meet the CMRR spec so the load CM of the 2nd stage is small So the 2nd stage has higher gain than wanted.

3. CM small signal ccs

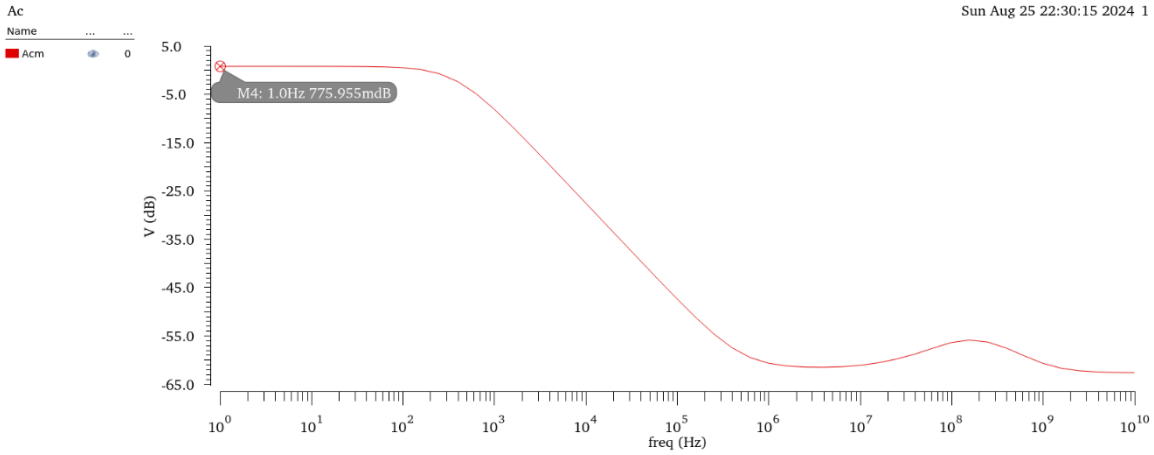

Figure 8: CM gain bode plot (magnitude)

Test	Output	Nominal
ITI_labs:lab9_TB1:1	Avcm	1.093
ITI_labs:lab9_TB1:1	Avcm in dB	776m

Figure 26: CM gain

$$DC\ CM\ gain \approx \frac{-g_{m0,1}}{2(g_{m0,1}+g_{mb0,1})g_{m4,5}r_{o3}} * g_{m6}(r_{o6} \parallel r_{o7})$$

Spec	*Simulation*	*Hand analysis*
$\lvert DC\ CM\ gain \rvert$	1.093	1.11

Table 4: simulation vs hand analysis

4. CMRR

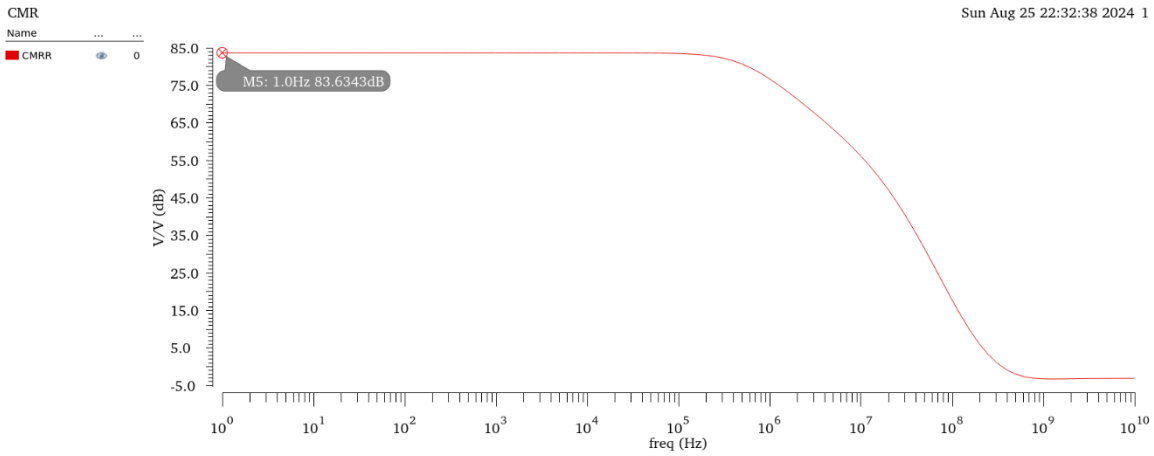

Figure 27: CMRR bode plot (magnitude)

Spec	*Simulation*	*Hand analysis*
CMRR @DC	83.6 dB	$A_{vd} - A_{vcm} = 83.5\ dB$

Table 5: simulation vs hand analysis

5. Diff large signal ccs

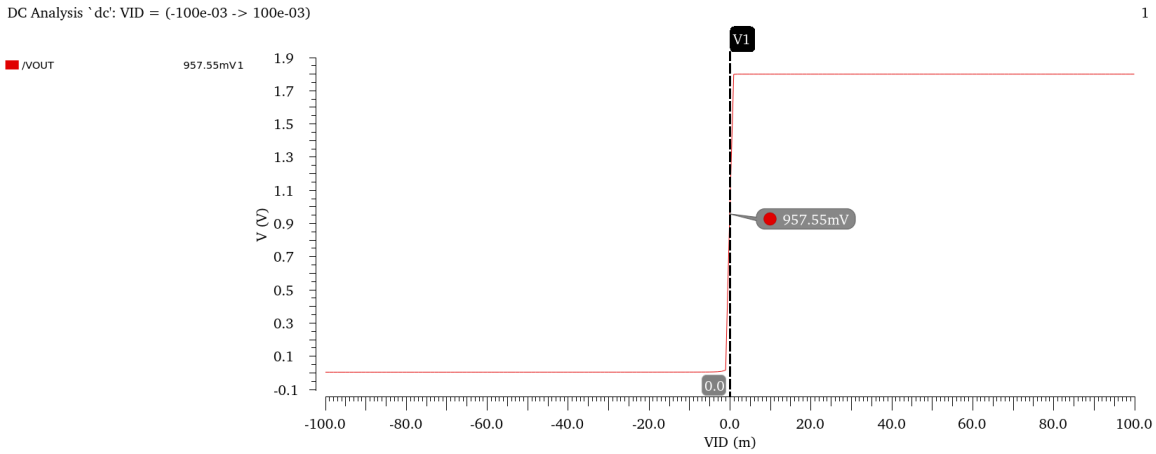

Figure 9: Vout vs VID

$V_{outdc} = 957.55\ mV$ almost the same from the OP part $(957.6\ mV)$ as there is no mismatch nor diff input.

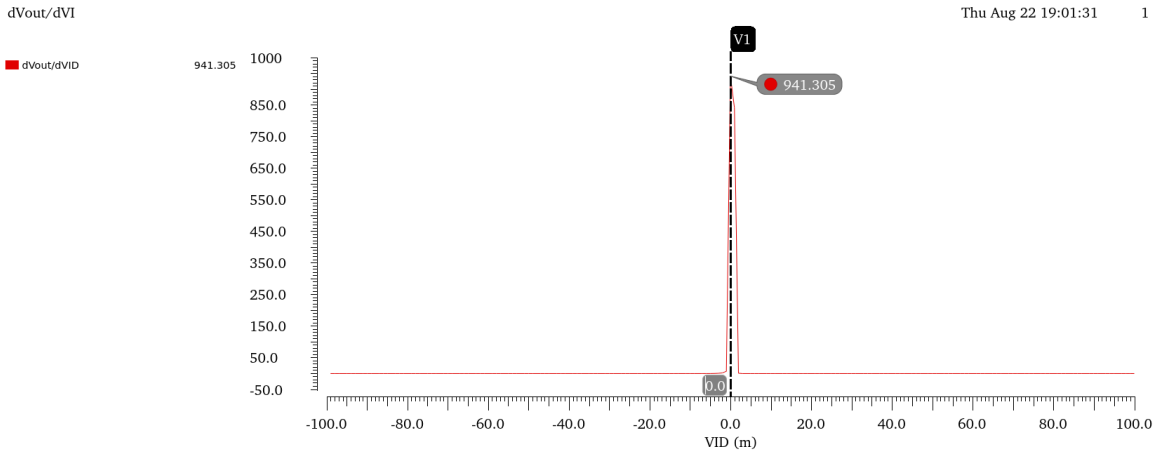

Figure 10: derivative(Vout) vs VID

The peak$= 941.3 \ll A_{vd}$ due to the very small swing of the differential input $(equals\ output\ swing/Avd = \frac{1.6}{16.62k})$ so the diff input swing is less than 0.1 mV and the step is 1 mV only so the results are inaccurate.

6. CM large signal ccs (region vs VICM)

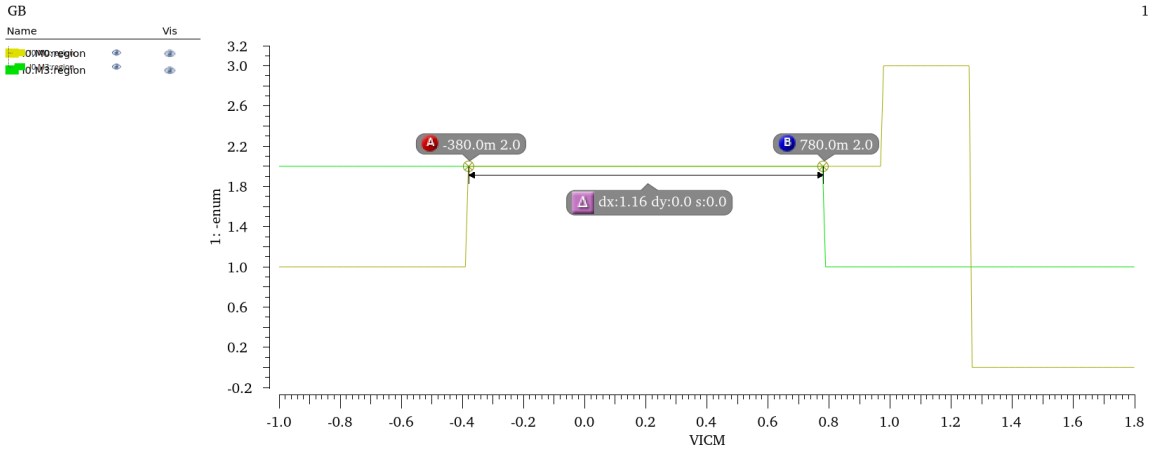

Figure 11: regions vs VICM

$$CMIR_{high} = V_{DD} - |V_{DSsat3}| - |V_{GS0,1}|$$
$$CMIR_{low} = -|V_{GS0,1}| + |V_{DSsat0,1}| + V_{GS4,5}$$

Spec	*simulation*	*analytic*
$CMIR_{low}$	$-380\ mV$	$-143\ mV$
$CMIR_{high}$	$780\ mV$	$693\ mV$

Table 6: CMIR simulation vs hand analysis

7. CM large signal ccs (GBW vs VICM)

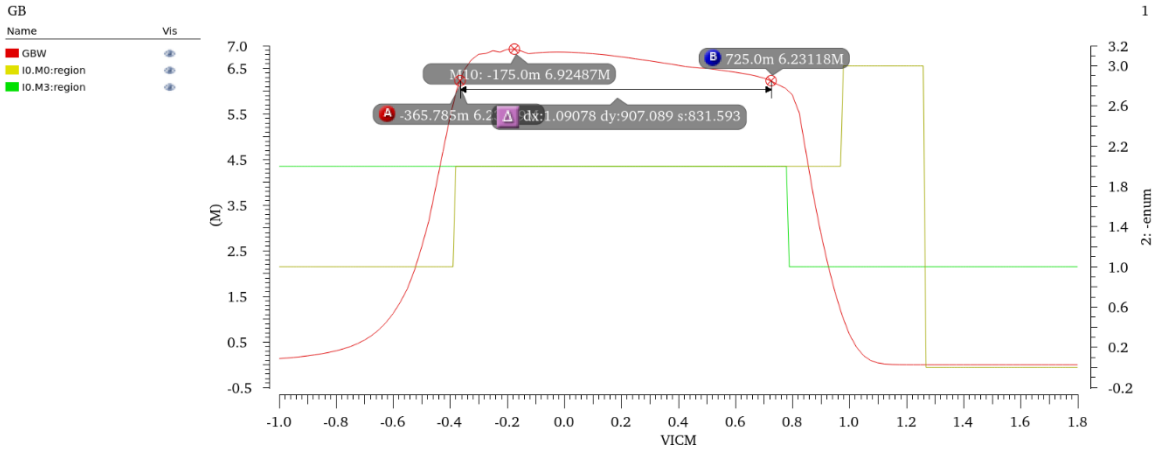

Figure 12: GBW vs VICM

$$CMIR_{high} = V_{DD} - |V_{DSsat3}| - |V_{GS0,1}|$$
$$CMIR_{low} = -|V_{GS0,1}| + |V_{DSsat0,1}| + V_{GS4,5}$$

Spec	*simulation*	*analytic*
$CMIR_{low}$	$-365\ mV$	$-143\ mV$
$CMIR_{high}$	$725\ mV$	$693\ mV$

Table 7: CMIR simulation vs hand analysis

The noticeable variance in the $CMIR$ is due to:

- The 90 % change in GBW is not an accurate value to detect the edge of saturation for the Diff Amp devices because the saturation happens gradually not eventually at a specific point.
- The body effect obstacles the $CMIR_{high}$ but it also advances $CMIR_{low}$ as the VGS increases and it appears in both specs in negative.

Part 3: Closed-Loop OTA Simulation

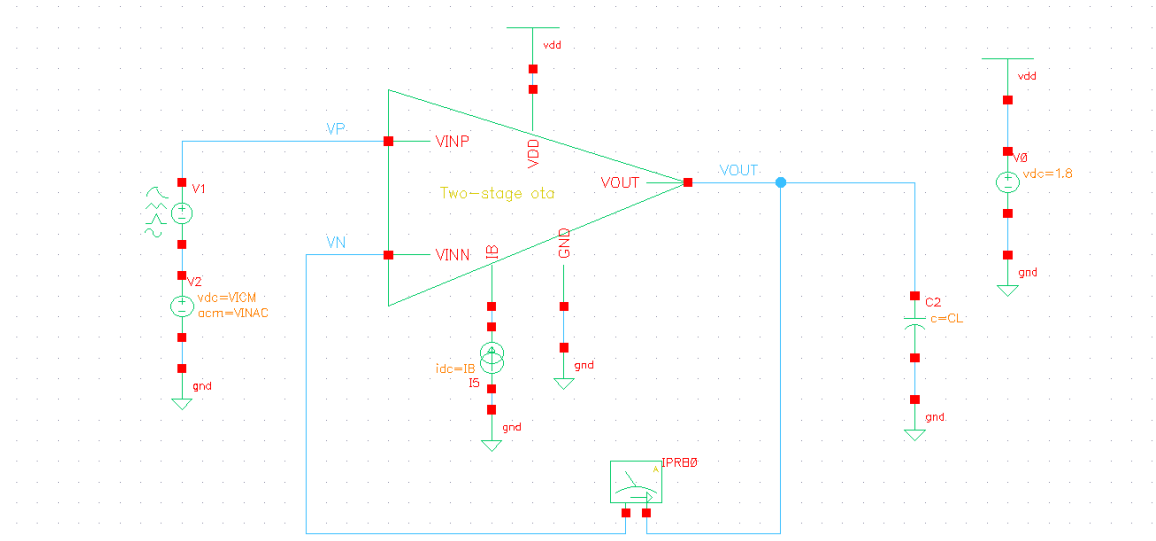

Figure 13: Closed-loop testbench schematic (CL=5 pF, IB=10 uA)

1. OP simulation

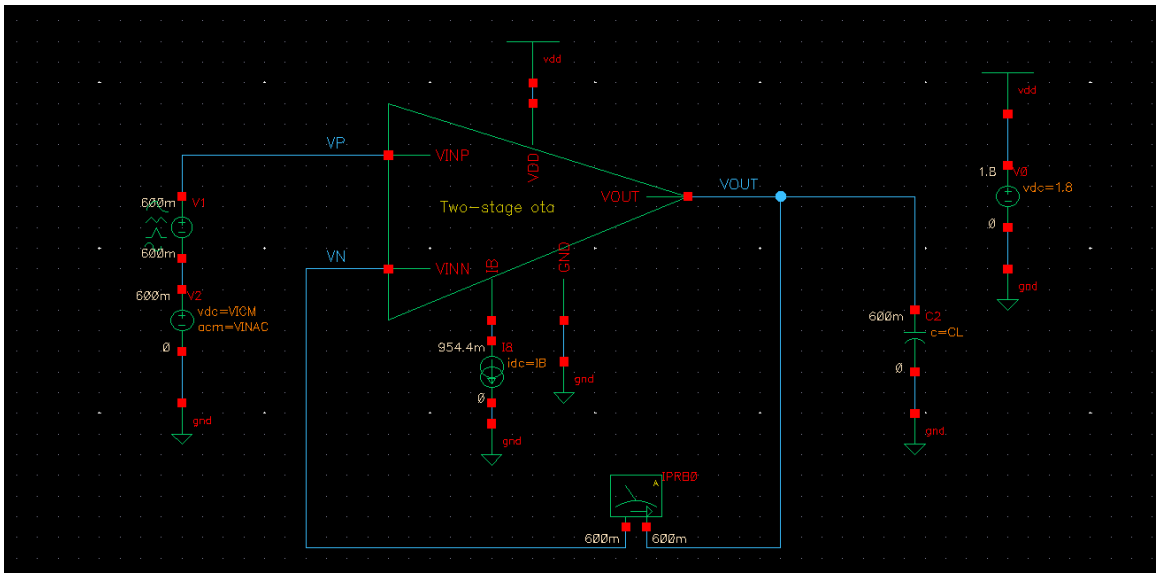

Figure 14: bias circuit with DC node voltages annotated

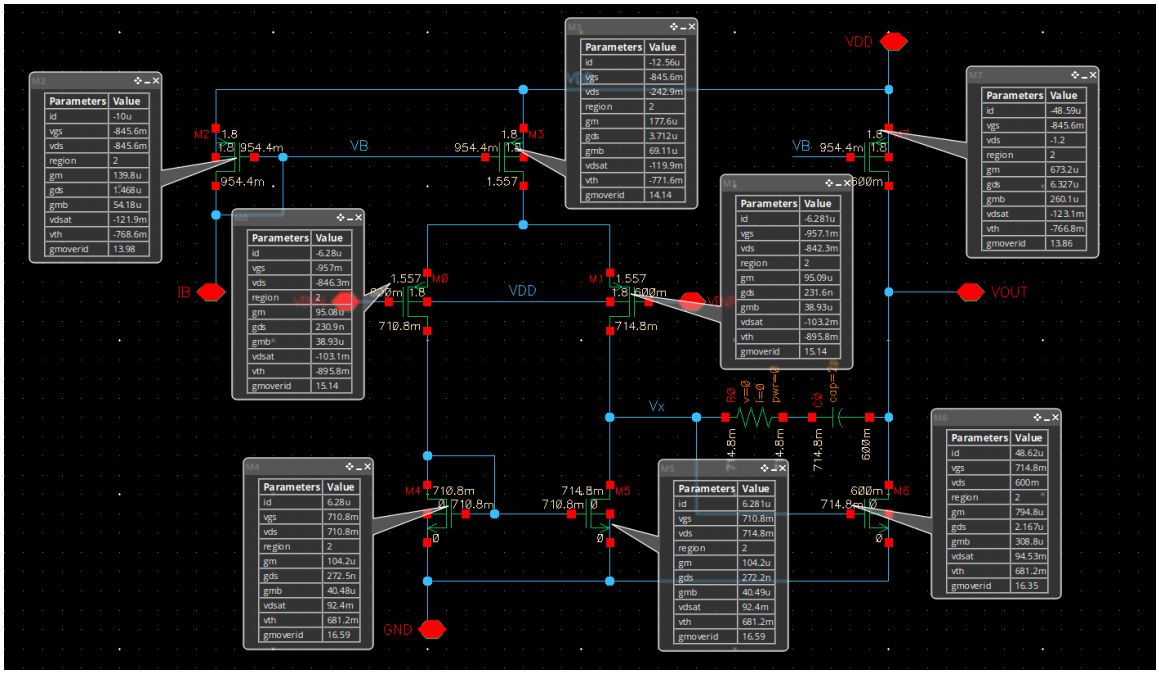

Figure 15: OTA schematic with DC node voltages and OP parameters annotated

- The voltage difference across the OTA's terminals (differential input/error signal) is nearly zero due to the very high open-loop gain which minimizes the error signal. As the error signal equals the output deviation from its dc level divided by the amplifier's open-loop gain$= \frac{(957.6-600)\,mV}{16.62\,K} \approx 21.5\,\mu V$.
- The output of the 1st stage dc level is different from its value in the open-loop simulation as the gain of the 2nd stage alone is finite and the error at this node is the output deviation from its dc level divided by the 2nd stage gain $\frac{(957.6-600)\,mV}{93} \approx 3.8\,mV$.
- The change in g_m *and* I_D $(about\ 0.02\%)$ is due to the amplifier's very high open-loop gain which minimizes the error across its input terminals.

2. Loop gain

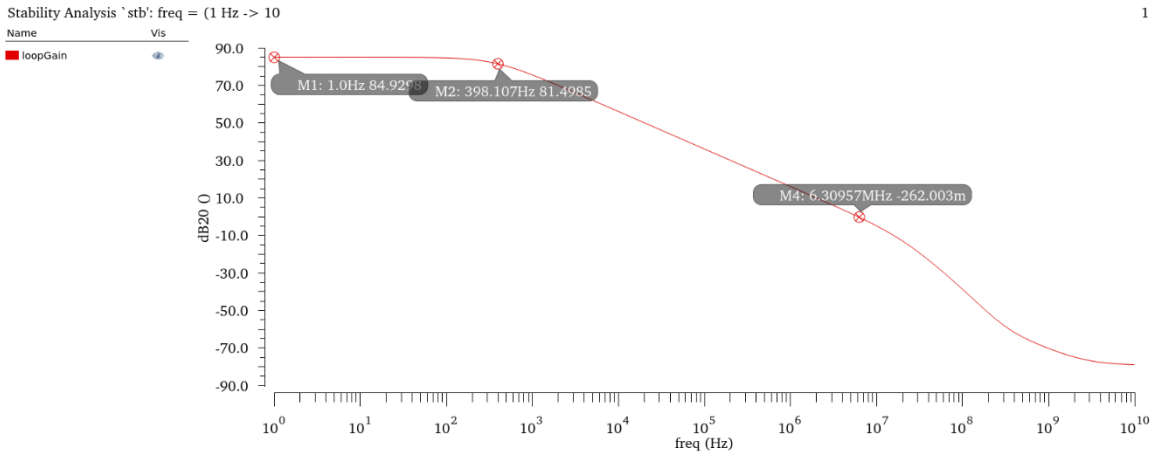

Figure 16: loop gain bode plot (magnitude)

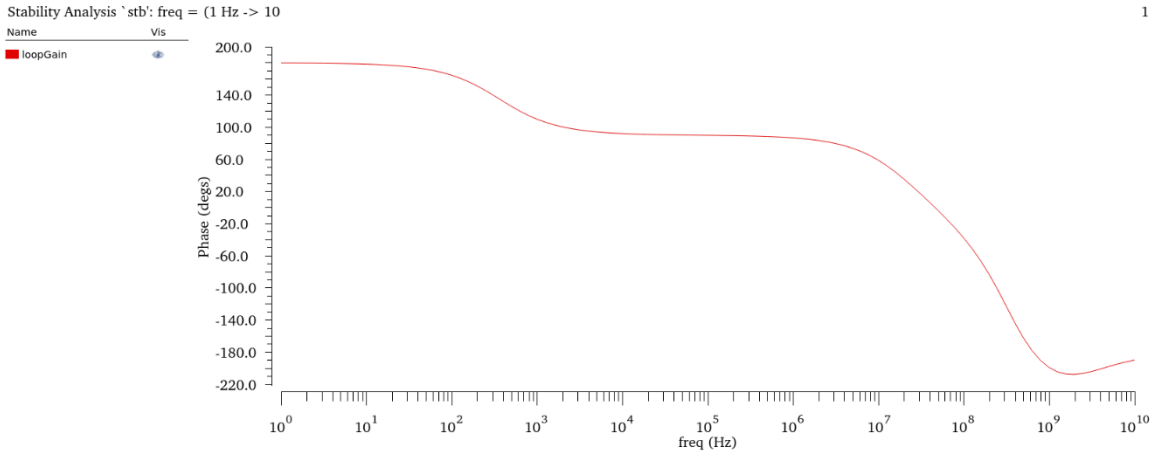

Figure 17: loop gain bode plot (phase)

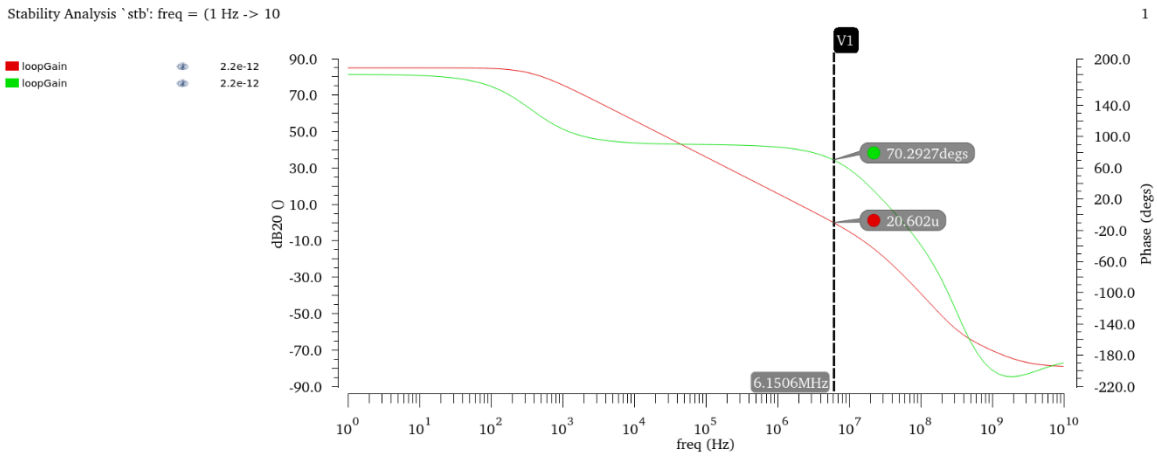

Figure 18: loop gain Gx

Test	Output	Nominal	Spec
ITI_labs:lab9_TB2:1	dc loop gain	17.64k	> 2k
ITI_labs:lab9_TB2:1	dc loop gain in dB	84.93	> 66
ITI_labs:lab9_TB2:1	BW	363.1	
ITI_labs:lab9_TB2:1	Fu	6.167M	> 5M
ITI_labs:lab9_TB2:1	GBW	6.42M	> 5M
ITI_labs:lab9_TB2:1	PM	70.33	> 70

Figure 19: STB analysis results

The open-loop results changed as Cc value changed as said in the report in the few coming pages.

Spec	*open loop simulation*	*closed loop simulation*
DC gain	84.41 dB	84.93 dB
BW	385.4 Hz	363.1 Hz
GBW	6.4 MHz	6.4 MHz

Table 8: open loop vs closed loop simulation

The specs variance between open and closed loop simulations is because V_{outDC} is changed so Vx too and there is error signal at the input therefore OP parameters are changed.

$$DC\ diff\ gain = g_{m0,1}(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7}),$$

$$BW \approx \frac{1}{2\pi(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7})C_c}, GBW = \frac{g_{m0,1}}{2\pi C_c}$$

$$PM = 90 - \tan^{-1}\left(\frac{\omega_u}{\omega_{p2}}\right), \frac{\omega_u}{\omega_{p2}} = \frac{g_{m0,1}}{C_c} * \frac{C_L}{g_{m6}}$$

Spec	*closed loop simulation*	*hand analysis*
DC gain	84.93 dB	84.93 dB
BW	363.1 Hz	472.6 Hz
GBW	6.4 MHz	6.58 MHz
PM	70.33^o	75.4^o

Figure 20: closed loop hand analysis

- BW, GBW & PM hand analysis are different from the simulation as the parasitic caps are large due to the large sizes and they are not taken into consideration in the hand analysis.

3. Slew rate

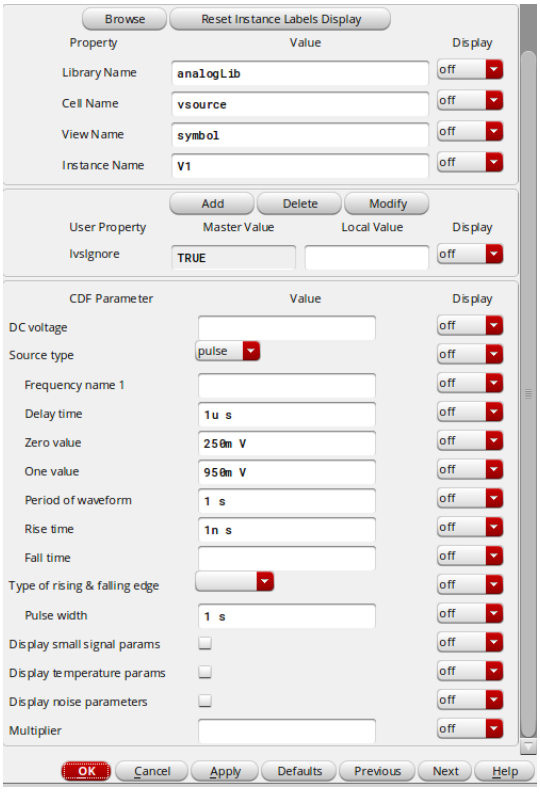

Figure 21: pulse settings

Test	Output	Nominal	Spec
ITI_labs:lab9_tb2:1	SR	4.501M	> 5M

Figure 22: Slew rate

We got SR less than expected due the large parasitic caps at node x so, after sweeping Cc we found that the SR & PM specs are met at $Cc = 2.3\ pF$.

Note: the results above are all with new Cc value.

Test	Output	Nominal	Spec
ITI_labs:lab9_TB2:1	SR	5.082936M	> 5M

Figure 23: Slew rate at Cc=2.3 pF

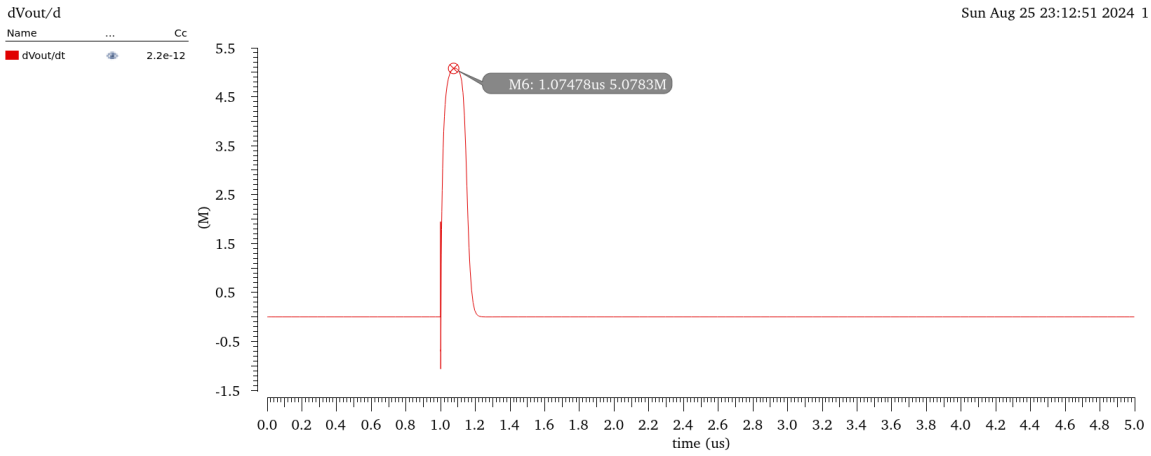

Figure 24: dVout/dt

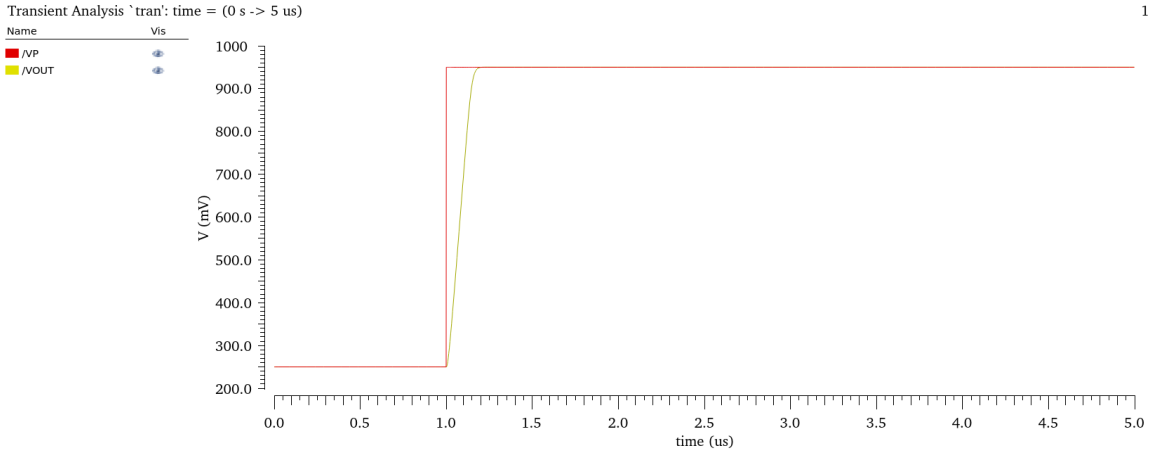

Figure 25: Transient analysis Vin & Vout vs time

$$SR \approx \frac{I_{B1}}{C_c}$$

Spec	*closed loop simulation*	*hand analysis*
Slew rate	$5.08\ V/\mu s$	$5.46\ V/\mu s$

Table 9: simulation vs hand analysis

- The hand analysis is less than simulation result due to the parasitic caps.

4. Settling time

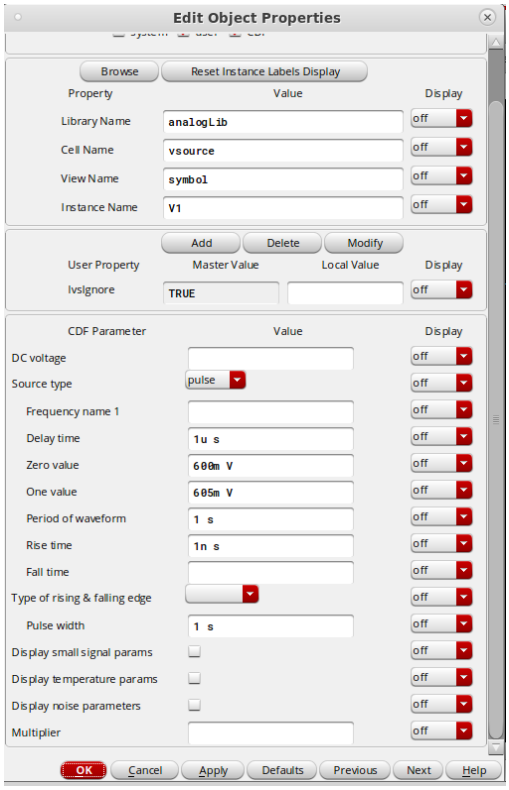

Figure 26: pulse settings

Test	Output	Nominal	Spec
ITI_labs:lab9_TB2:1	rise time	36.18n	< 70n

Figure 27: rise time

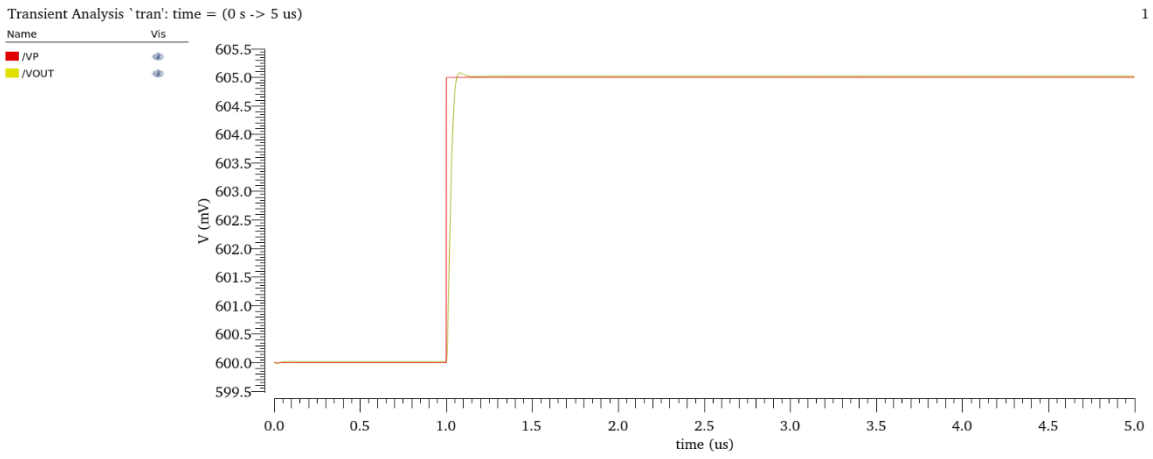

Figure 28: Vin & Vout vs time

$$T_{rise} = (\ln 9)\tau = \frac{\ln 9}{2\pi GBW}$$

Spec	*closed loop simulation*	*hand analysis*
rise time	$36.18\ ns$	$54.64\ ns$

- The simulation result is better as the hand analysis approximates the system to a 1st order system but in reality it's a 2nd order system which has faster response.
- There is ringing as $PM < 76^o$ so it's underdamped system.

Part 4: DC Closed Loop AC Open-Loop OTA Simulation

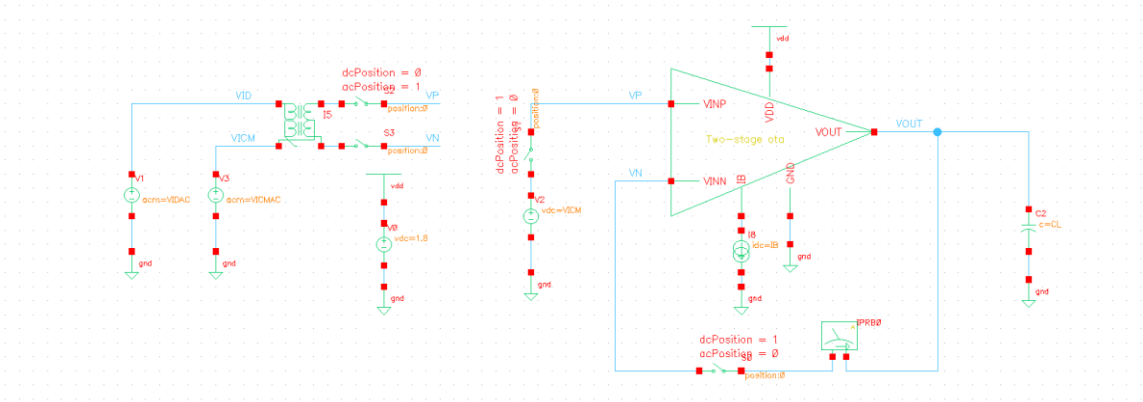

Figure 29: Testbench schematic (CL=5 pF, IB=10 uA)

1. OP simulation

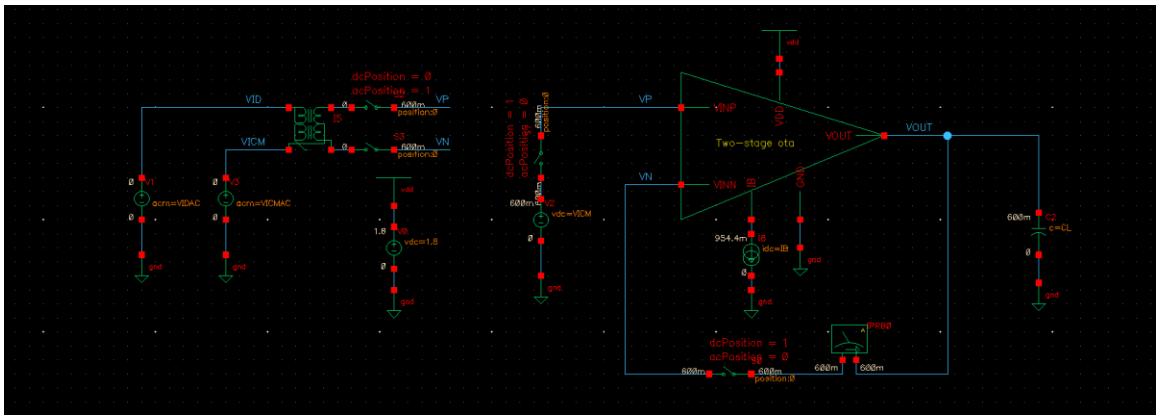

Figure 30: bias circuit with DC node voltages annotated

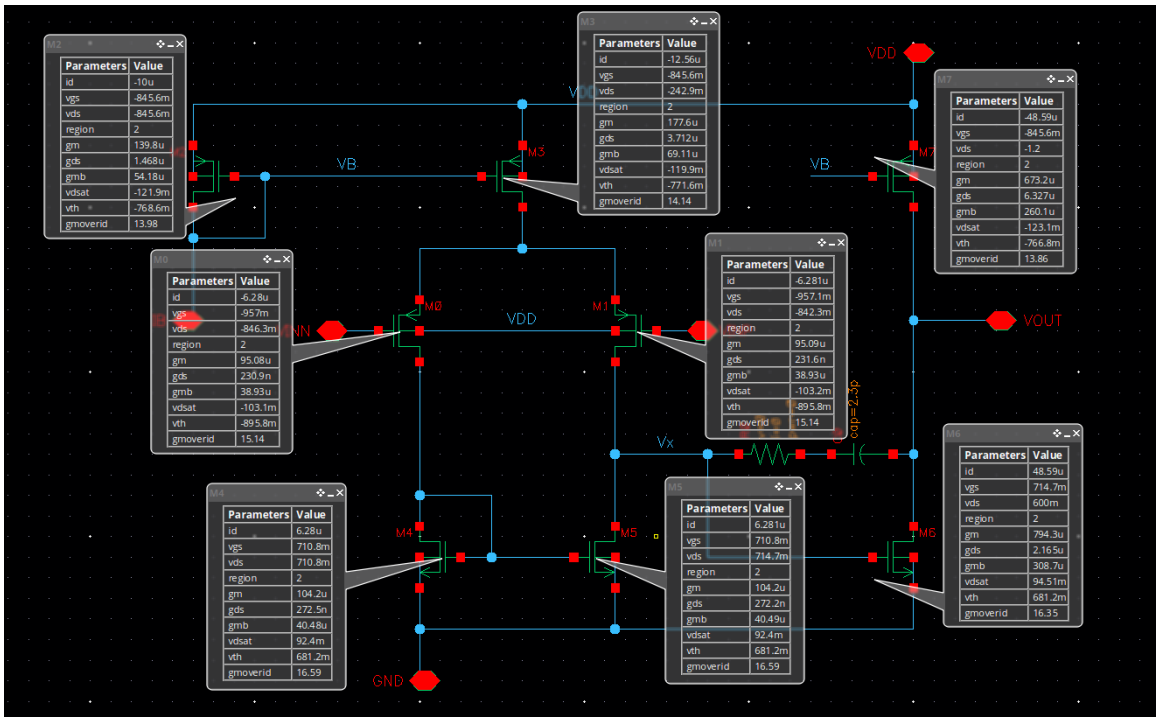

Figure 31: OTA schematic with DC node voltages and OP parameters annotated

- All devices are in sat.
- The change in g_m *and* I_D $(about\ 0.02\%)$ is due to the amplifier's very high open-loop gain which minimizes the error across its input terminals.
- The voltage difference across the OTA's terminals (differential input/error signal) is nearly zero due to the very high open-loop gain which minimizes the error signal. As the error signal equals the output deviation from its dc level divided by the amplifier's open-loop gain$= \frac{(957.6-600)\ mV}{16.62\ K} \approx 21.5\ \mu V$.
- The output of the 1st stage dc level is different from its value in the open-loop simulation as the gain of the 2nd stage alone is finite and the error at this node is the output deviation from its dc level divided by the 2nd stage gain $\frac{(957.6-600)\ mV}{93} \approx 3.8\ mV$.

2. Diff small signal ccs

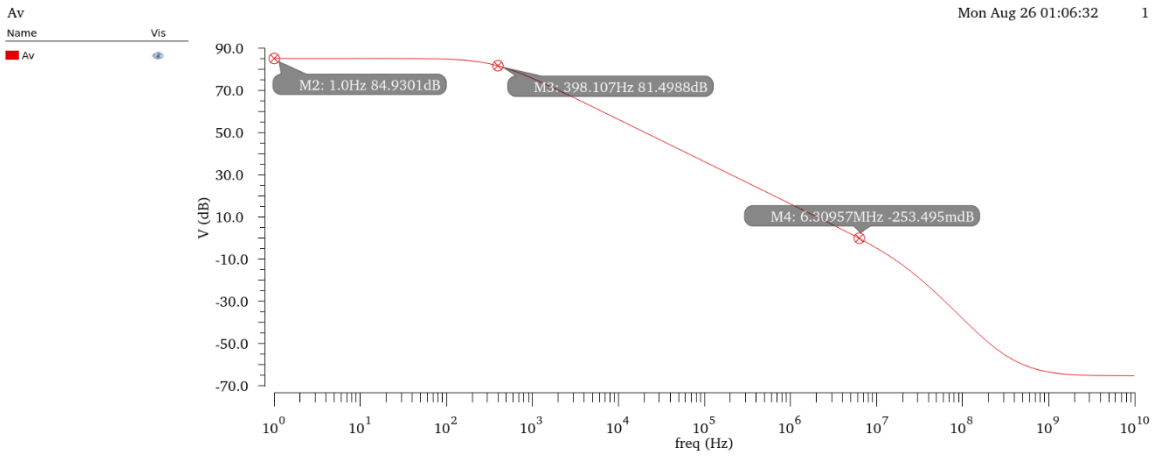

Figure 32: diff gain bode plot (magnitude)

Test	Output	Nominal	Spec
ITI_labs:lab9_TB3:1	Av	17.64k	> 2k
ITI_labs:lab9_TB3:1	Av in dB	84.93	> 66
ITI_labs:lab9_TB3:1	BW	363.1	
ITI_labs:lab9_TB3:1	Fu	6.172M	> 5M
ITI_labs:lab9_TB3:1	GBW	6.421M	

Figure 33: diff small signal results

$$DC\ diff\ gain = g_{m0,1}(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7}),$$

$$BW \approx \frac{1}{2\pi(r_{o1} \parallel r_{o5}) * g_{m6}(r_{o6} \parallel r_{o7})C_c}, GBW = \frac{g_{m0,1}}{2\pi C_c}$$

Spec	*Simulation*	*Hand analysis*
DC diff gain	84.93 *dB*	84.94 *dB*
BW	363.1 *Hz*	372.7 *Hz*
GBW	6.4 *MHz*	6.58 *MHz*

Table 10: simulation vs hand analysis

- BW & GBW hand analysis are different from the simulation as the parasitic caps are large due to the large sizes and they are not taken into consideration in the hand analysis.

3. CM small signal ccs

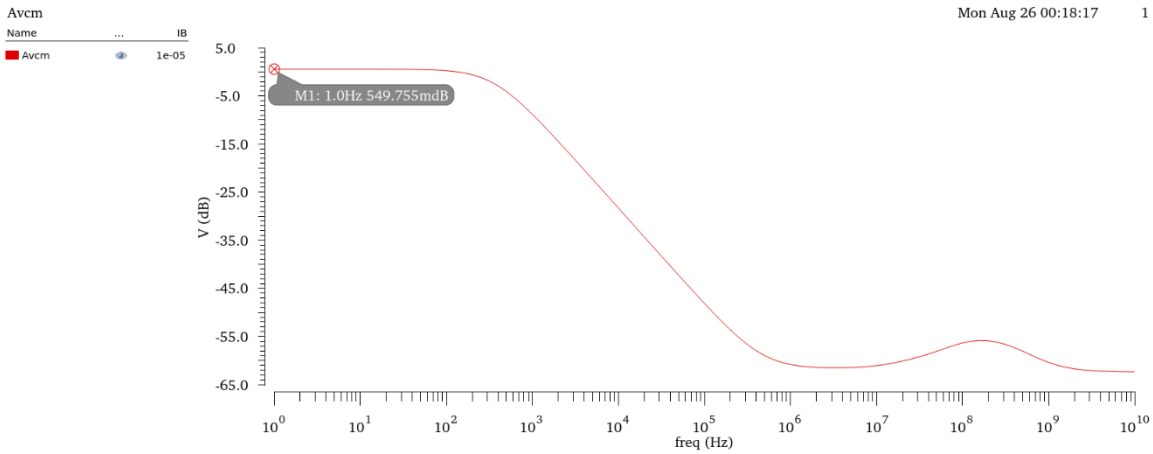

Figure 34: CM gain bode plot (magnitude)

Test	Output	Nominal
ITI_labs:lab9_TB3:1	Avcm	1.065
ITI_labs:lab9_TB3:1	Avcm in dB	549.8m

Figure 26: CM gain

$$DC\ CM\ gain \approx \frac{-g_{m0,1}}{2(g_{m0,1}+g_{mb0,1})g_{m4,5}r_{o3}} * g_{m6}(r_{o6} \parallel r_{o7})$$

Spec	*Simulation*	*Hand analysis*
$\lvert DC\ CM\ gain \rvert$	1.065	1.1

Table 11: simulation vs hand analysis

4. CMRR

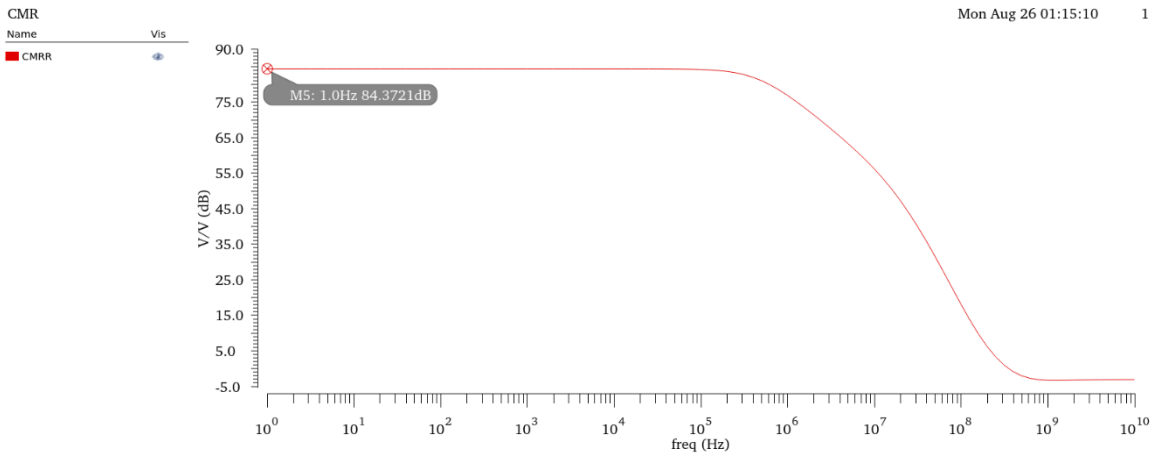

Figure 27: CMRR bode plot (magnitude)

Spec	*Simulation*	*Hand analysis*
CMRR	$84.37\ dB$	$A_{vd} - A_{vCM} = 84.1\ dB$

Table 12: simulation vs hand analysis

5. Diff large signal ccs

This simulation can't be done in this testbench as the diff input is OC in DC

6. CM large signal ccs (region vs VICM)

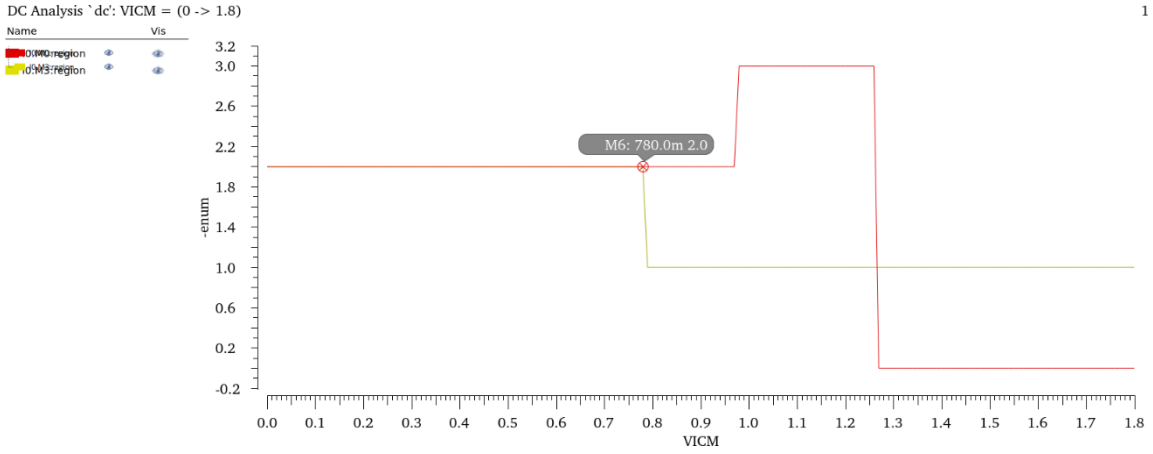

Figure 35: regions vs VICM

$$CMIR_{high} = V_{DD} - |V_{DSsat3}| - |V_{GS0,1}|$$
$$CMIR_{low} = -|V_{GS0,1}| + |V_{DSsat0,1}| + V_{GS4,5}$$

Spec	*simulation*	*analytic*
$CMIR_{low}$	$-$	$-143\ mV$
$CMIR_{high}$	$780\ mV$	$693\ mV$

7. CM large signal ccs (GBW vs VICM)

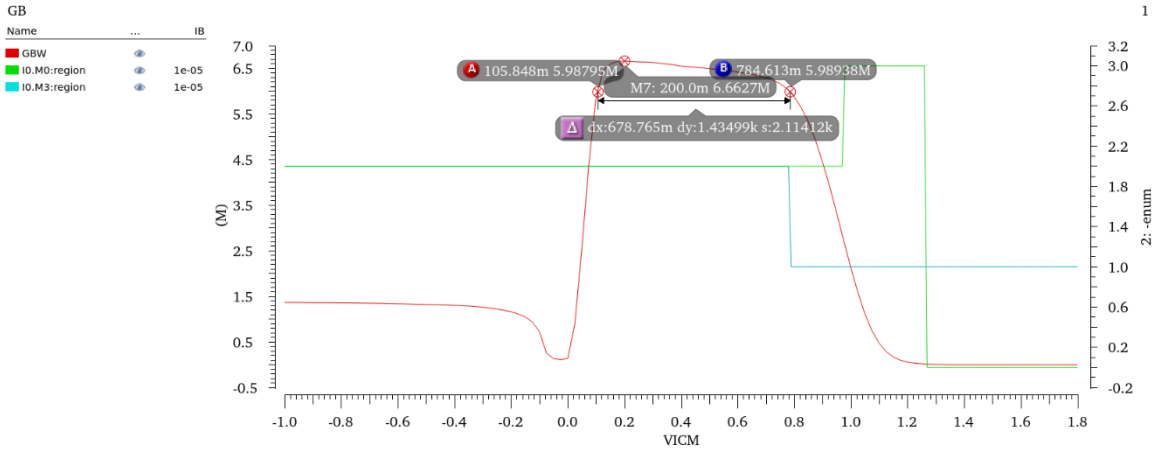

Figure 36: GBW vs VICM

$$CMIR_{high} = V_{DD} - |V_{DSsat3}| - |V_{GS0,1}|$$
$$CMIR_{low} = -|V_{GS0,1}| + |V_{DSsat0,1}| + V_{GS4,5}$$

Spec	*simulation*	*analytic*
$CMIR_{low}$	$105.9\ mV$	$-143\ mV$
$CMIR_{high}$	$784\ mV$	$693\ mV$

Table 5: CMIR

The noticeable variance in the $CMIR$ is due to:

- The body effect obstacles the $CMIR_{high}$ but it also advances $CMIR_{low}$ as the VGS increases and it appears in both specs in negative.

Part 5: Design specs

Spec	*Required*	*Achieved*
Supply Voltage	$1.8\ V$	$1.8\ V$
Static gain error	$\leq 0.05\ \%$	$6 * 10^{-3}\%$
CMRR @DC	$\geq 74\ dB$	$83.6\ dB$
Phase Margin	$\geq 70°$	$70.33°$
OTA current consumption	$\leq 60\ \mu A$	$58.8\ \mu A$
CMIR - high	$\geq 1\ V$	$725\ mV$
CMIR - low	$\leq 0.2\ V$	$-365\ mV$
Output swing	$0.2\ V - 1.6\ V$	$121\ mV - 1.657\ V$
Load	$5\ pF$	$5\ pF$
Buffer closed loop rise time (10% to 90%)	$\leq 70\ ns$	$36.18\ ns$
Slew rate	$5\ V/\mu s$	$5.08\ V/\mu s$

Table 13: Design specs