

Chapter No:7

Latches and Flip Flop

TOPICS

1. Latches
2. Flip-Flops
3. Flip-Flop Operating Characteristics
4. Flip-Flop Applications

Flip-Flops

. The fundamentals of sequential logic , Bistable, Monostable, and Astable logic devices called multivibrators . A multivibrator circuit oscillates between a "HIGH" state and a "LOW" state producing a continuous output.

Astable - A free-running multivibrator that has **NO** stable states but switches continuously between two states this action produces a train of square wave pulses at a fixed frequency.

Monostable - A one-shot multivibrator that has only **ONE** stable state and is triggered externally with it returning back to its first stable state.

Bistable - A flip-flop that has **TWO** stable states that produces a single pulse either positive or negative in value.

Two categories of bistable devices are the latch and the flip-flop. The flip-flop is a basic building block for counters, registers, and other sequential control logic and is used in certain types of memories

LATCHES

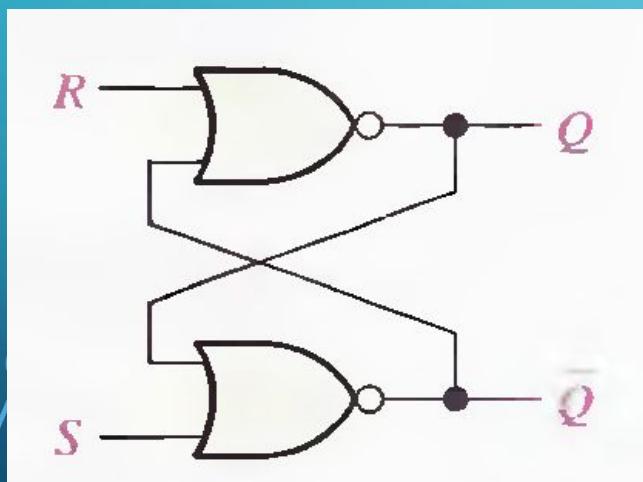
The **latch** is a type of temporary storage device that has two stable states (bistable) and is normally placed in a category separate from that of flip-flops. Latches are similar to flip-flops because they are bistable devices that can reside in either of two states using a feedback arrangement, in which the outputs are connected back to the opposite inputs. The main difference between latches and flip-flops is in the method used for changing their state.

FLIP-FLOPS

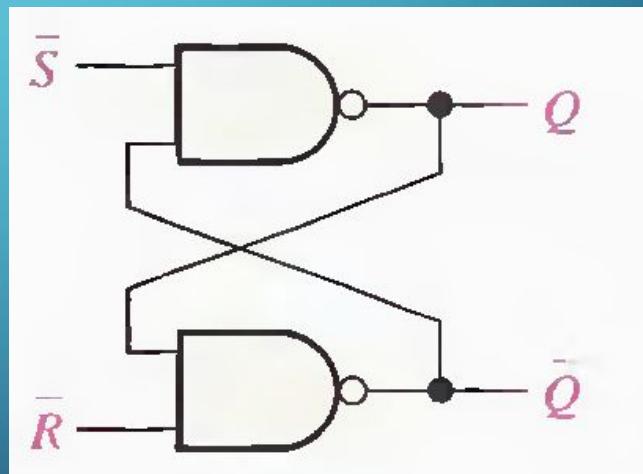
Flip-flops are synchronous bistable devices, also known as *bistable multivibrators*. In this case, the term *synchronous* means that the output changes state only at a specified point on the triggering input called the **clock** (CLK), which is designated as a control input, *C*; that is, changes in the output occur in synchronization with the clock.

The S-R (SET-RESET) Latch

A latch is a type of bistable logic device or multivibrator. An active-HIGH input S-R (SET- RESET) latch is formed with two cross-coupled NOR gates, an active-LOW input S-R latch is formed with two cross-coupled NAND gates, .That the output of each gate is connected to an input of the opposite gate .This produces the regenerative feedback that is characteristic of all latches and flip-flops.

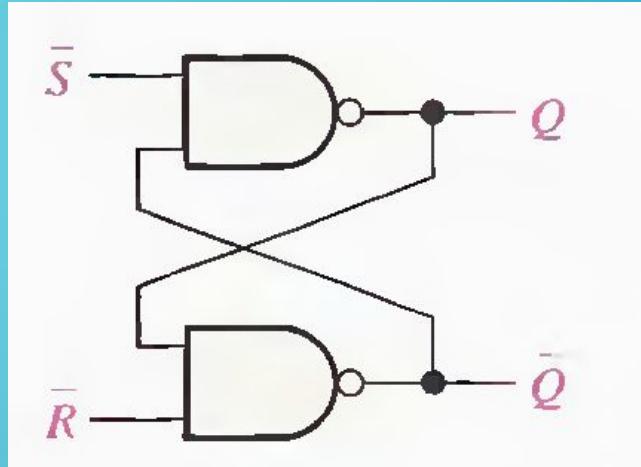
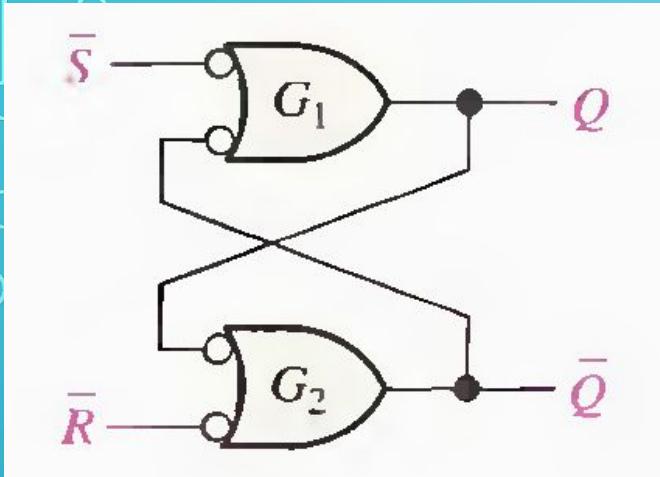


Active-HIGH input S-R latch



Active-LOW input S-R latch

Negative-OR equivalent of the NAND gate S-R latch



When Q is HIGH, \bar{Q} is LOW, and when Q is LOW, \bar{Q} is HIGH.

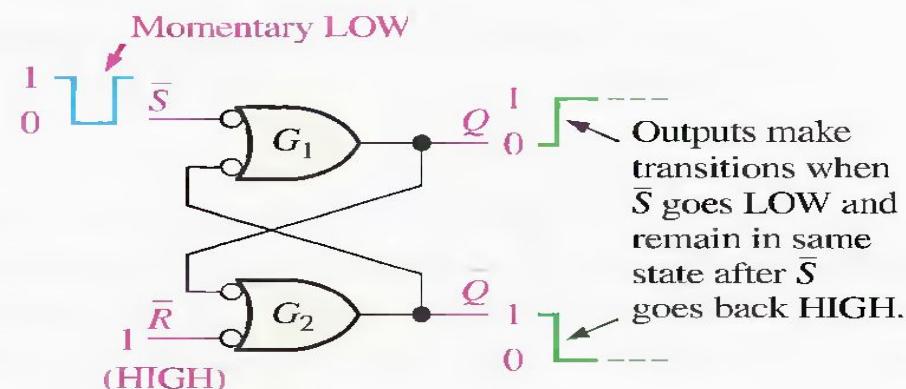
Let's start by assuming that both inputs and the Q output are HIGH. Since the Q output is connected back to an input of gate G₂, and the R' input is HIGH, the output of G₂ must be LOW. This LOW output is coupled back to an input of gate G₁ to ensure that its output is HIGH. When the Q output is HIGH, the latch is in the SET state. It will remain in this state indefinitely until LOW is temporarily applied to the R' input.

With a LOW on the R' input and a HIGH on S', the output of gate G₂ is forced HIGH. This HIGH on the Q' output is coupled back to an input of G₁, and since the S' input is HIGH, the output of G₁ goes LOW. This LOW on the Q output is then coupled back to an input of G₂, ensuring that the Q' output remains HIGH even when the LOW on the R' input is removed.

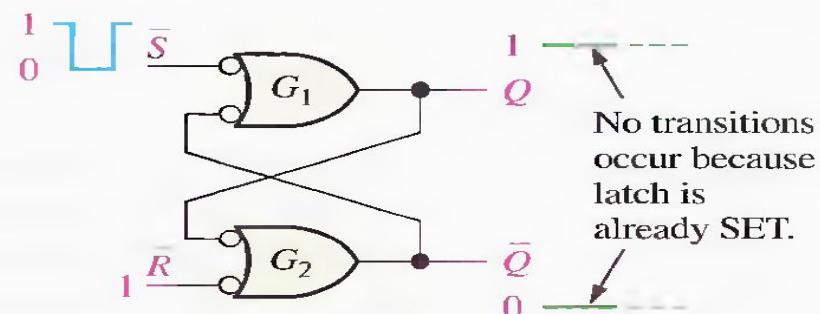
When the Q output is LOW, the latch is in the RESET state. Now the latch remains indefinitely in the RESET state until a LOW is applied to the S' input.

A latch can reside in either of its two states, SET or RESET.

SET means that the Q output is HIGH.

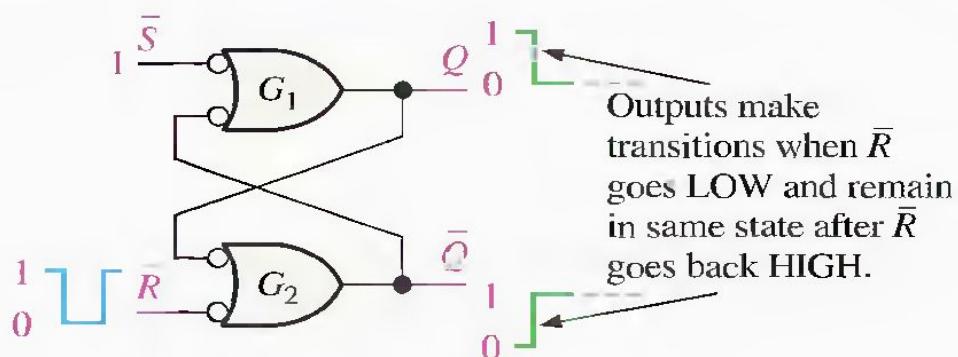


Latch starts out RESET ($Q = 0$).

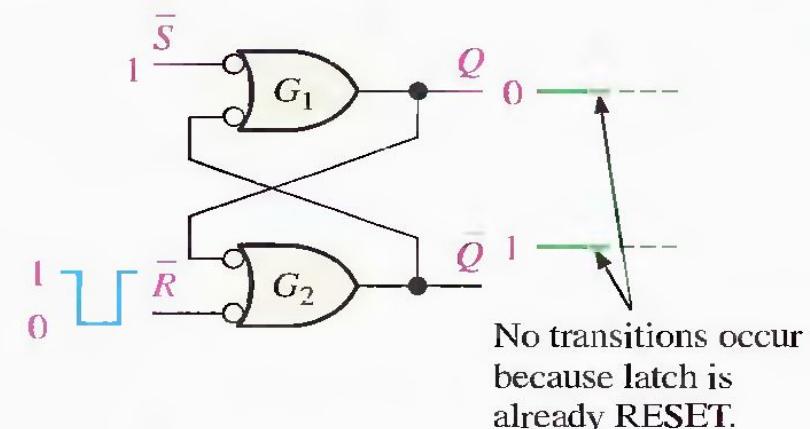


Latch starts out SET ($Q = 1$).

RESET means that the Q output is LOW.

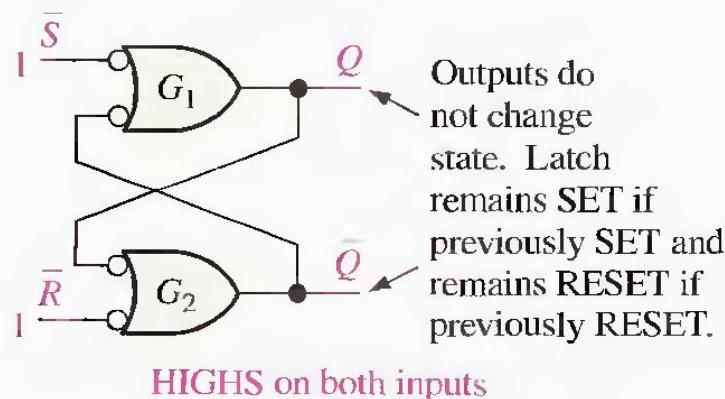


Latch starts out SET ($Q = 1$).

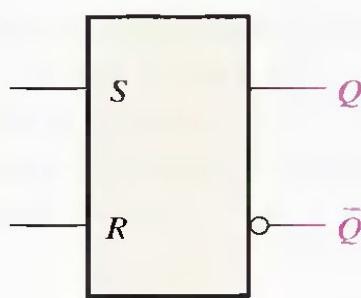
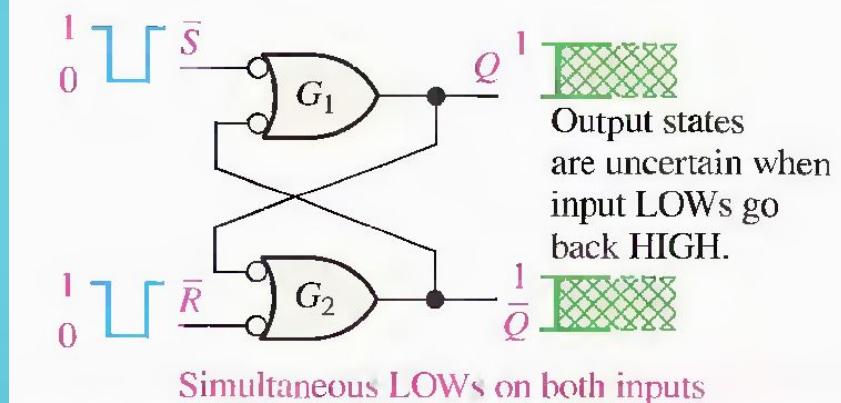


Latch starts out RESET ($Q = 0$).

No-change condition



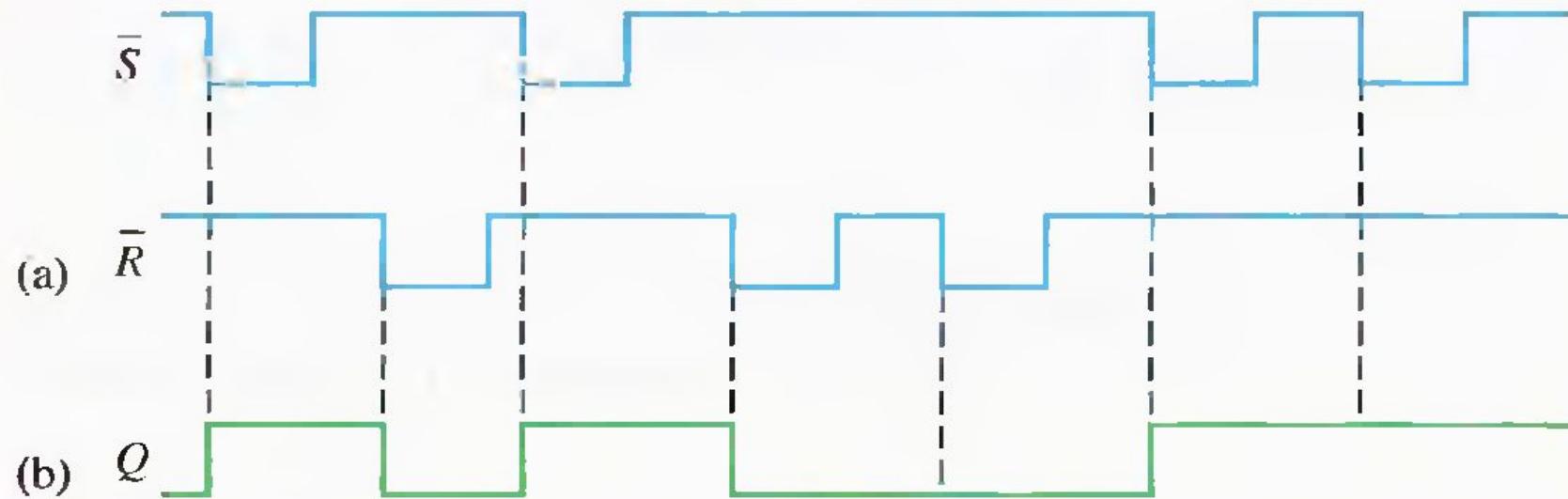
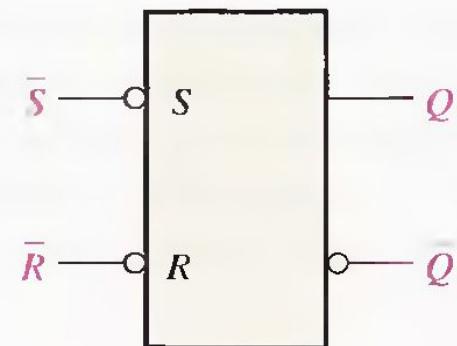
Invalid condition



(a) Active-HIGH input S-R latch

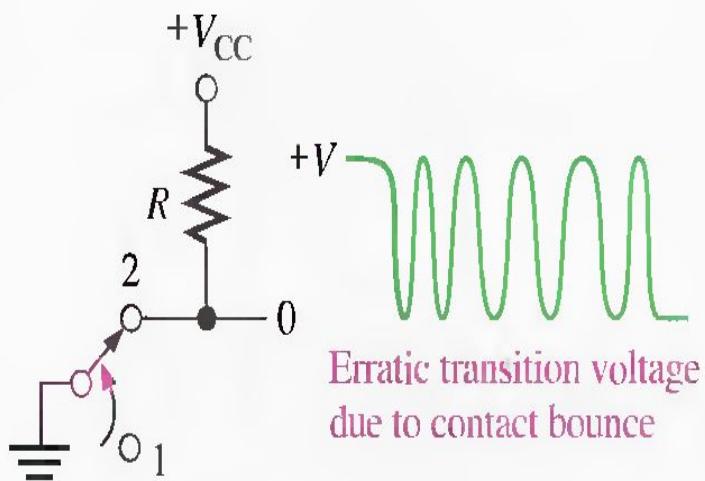
INPUTS		OUTPUTS		COMMENTS
\bar{S}	\bar{R}	Q	\bar{Q}	
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

If the \bar{S} and \bar{R} waveforms in Figure are applied to the inputs of the latch in Figure determine the waveform that will be observed on the Q output.
Assume that Q is initially LOW.

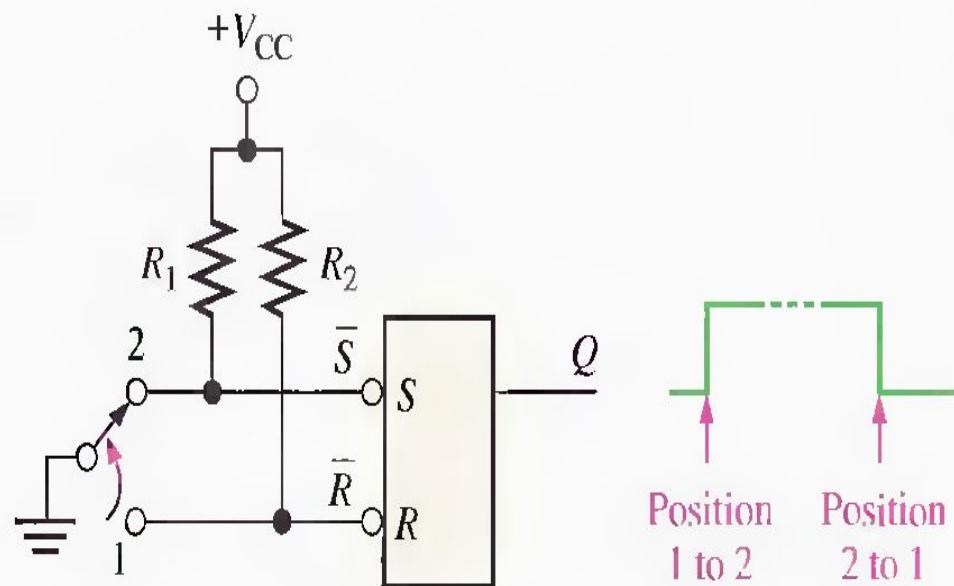


An Application

The Latch as a Contact-Bounce Eliminator



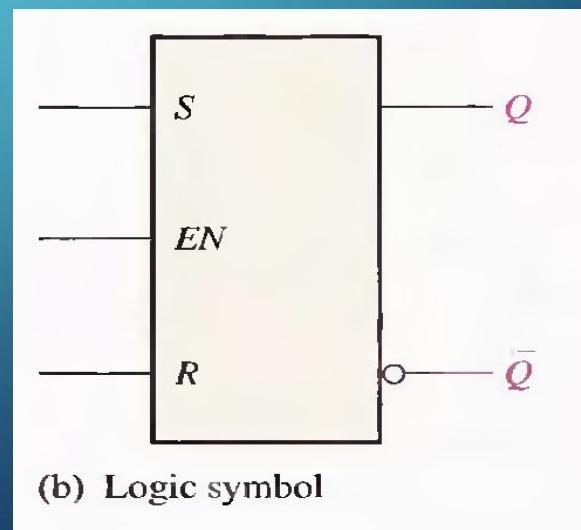
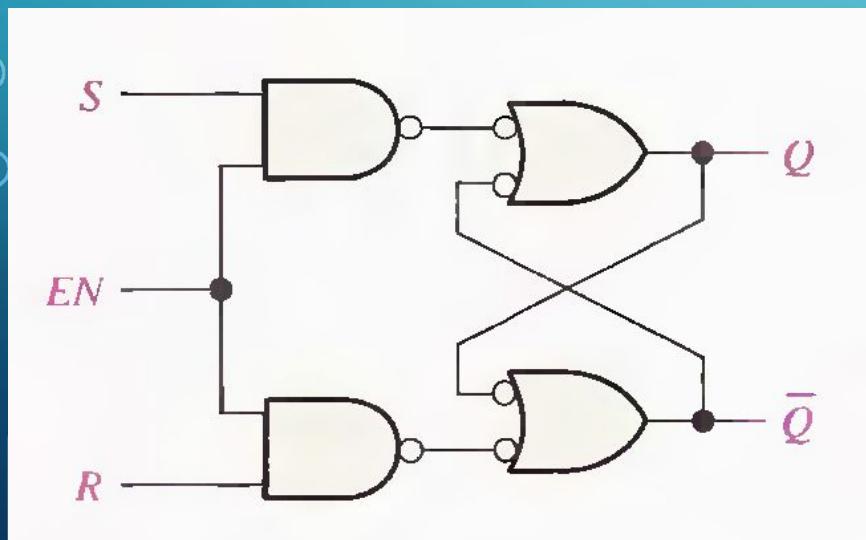
(a) Switch contact bounce



(b) Contact-bounce eliminator circuit

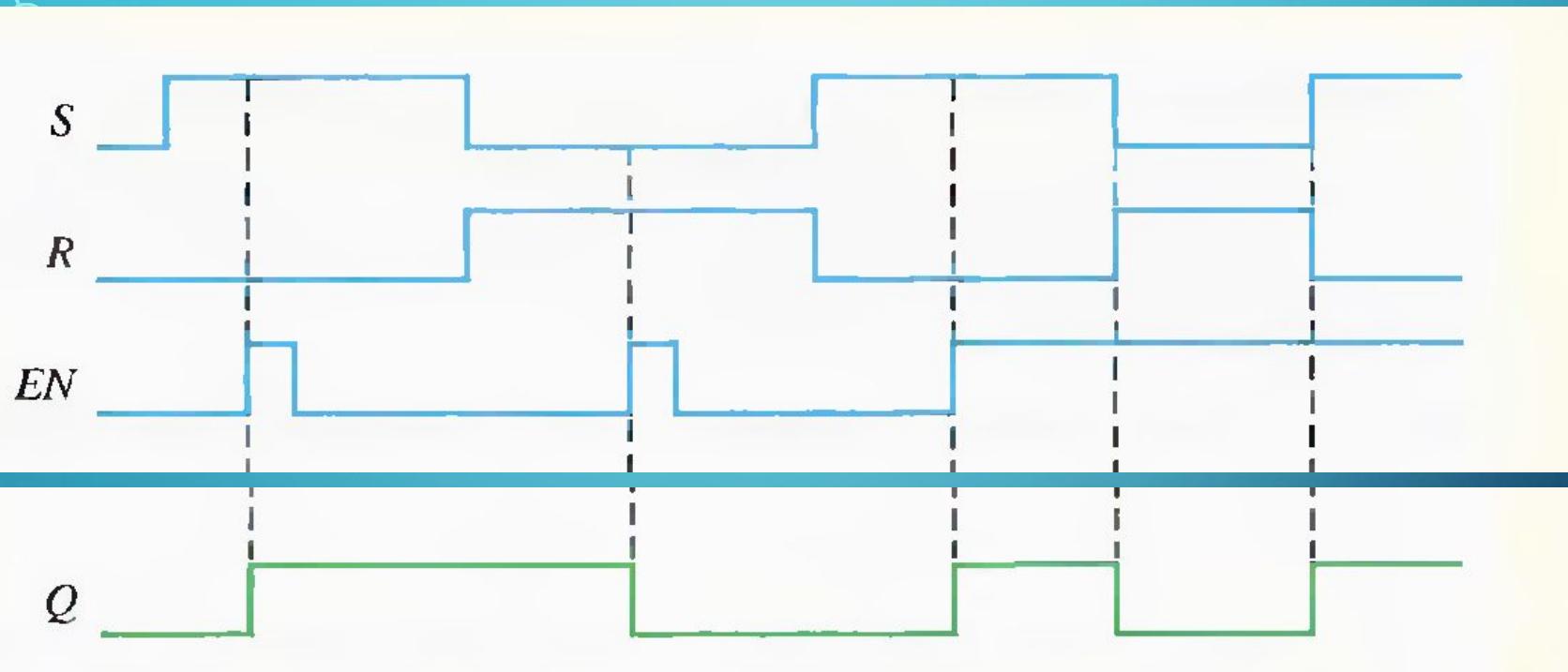
The Gated S-R Latch

A gated latch requires an enable input, EN (G is also used to designate an enable input). The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input. The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs. In this circuit, the invalid state occurs when both S and R are simultaneously HIGH.



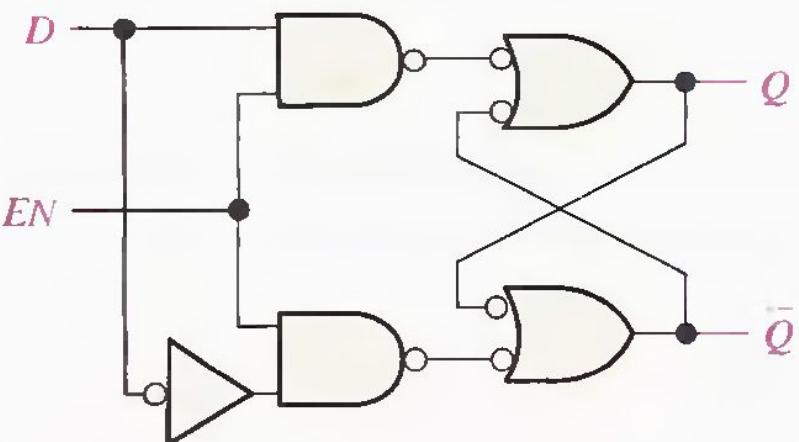
a gated S-R latch that is initially RESET.

Determine the Q output waveform

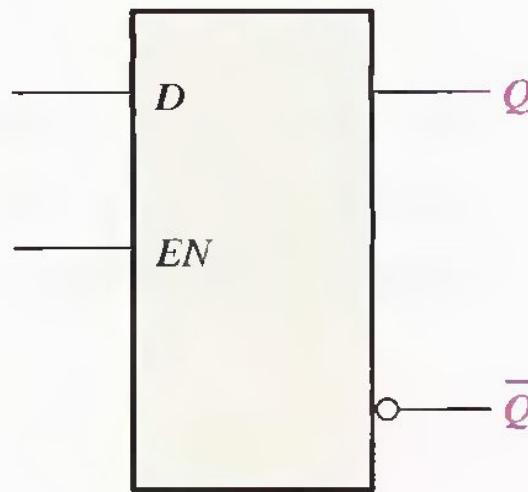


The Gated D Latch

Gated D latch is differs from the S-R latch because it has only one input in addition to EN. This input is called the D (data) input. When the D input is HIGH and the EN input is HIGH, the latch will set. When the D input is LOW and EN is HIGH, the latch will reset. Stated another way, the output Q follows the input D when EN is HIGH.

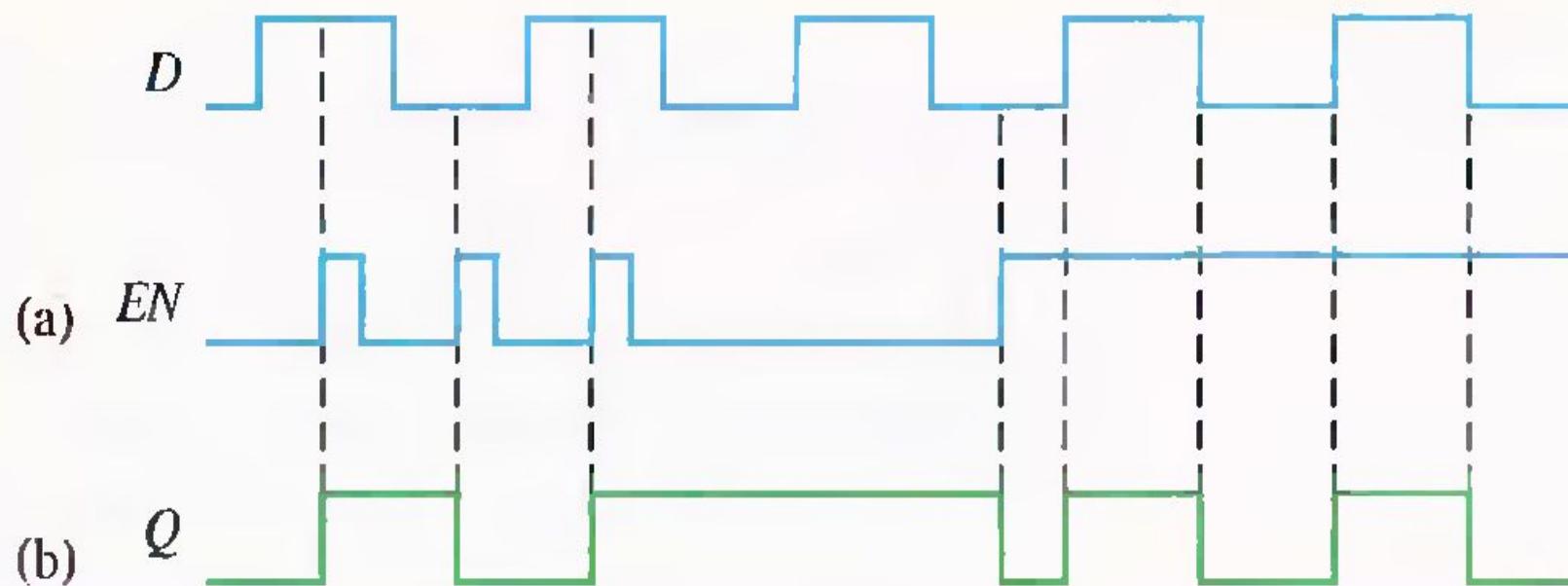


(a) Logic diagram



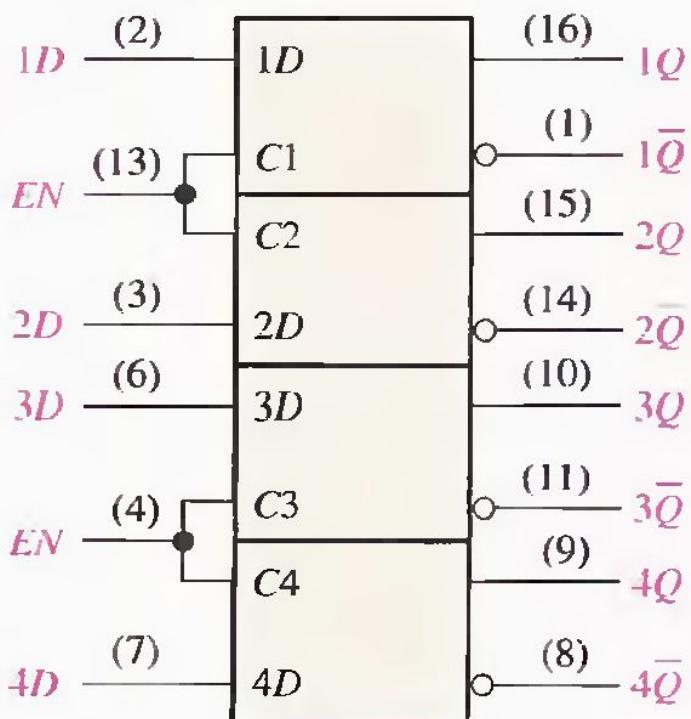
(b) Logic symbol

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.



THE 74LS75 D LATCH

The 74LS75 quad gated D latches.



(a) Logic symbol

Inputs		Outputs		Comments
D	EN	Q	\bar{Q}	
0	1	0	1	RESET
1	1	1	0	SET
X	0	Q_0	\bar{Q}_0	No change

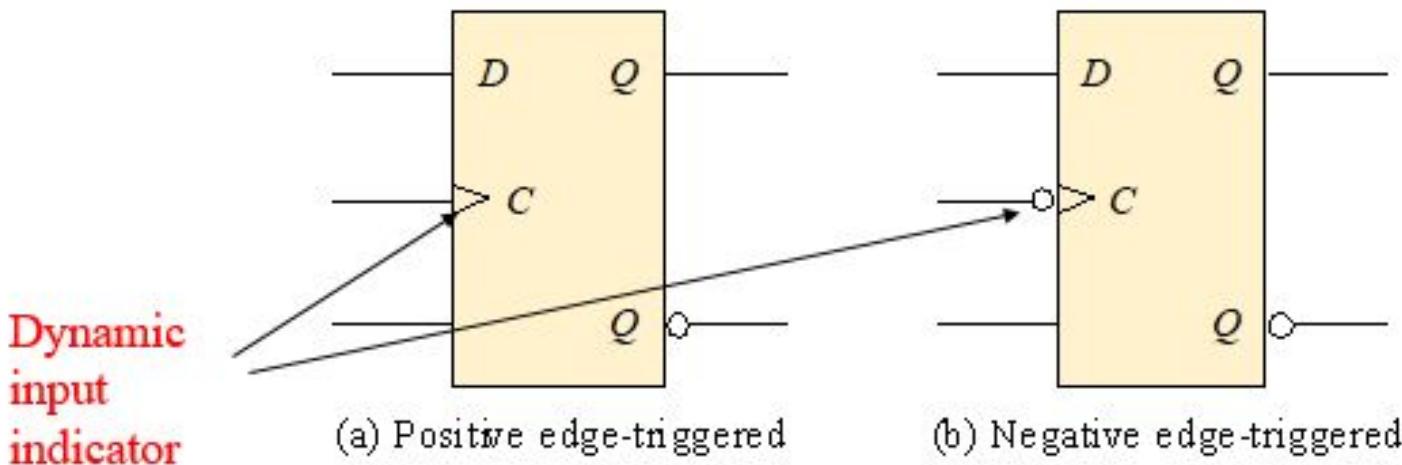
Note: Q_0 is the prior output level before the indicated input conditions were established.

(b) Truth table (each latch)

Flip-flops

A flip-flop differs from a latch in the manner it changes states. A flip-flop is a clocked device, in which only the clock edge determines when a new bit is entered.

The active edge can be positive or negative.



Flip-flops

The truth table for a positive-edge triggered D flip-flop shows an up arrow to remind you that it is sensitive to its D input only on the rising edge of the clock; otherwise it is latched. The truth table for a negative-edge triggered D flip-flop is identical except for the direction of the arrow.

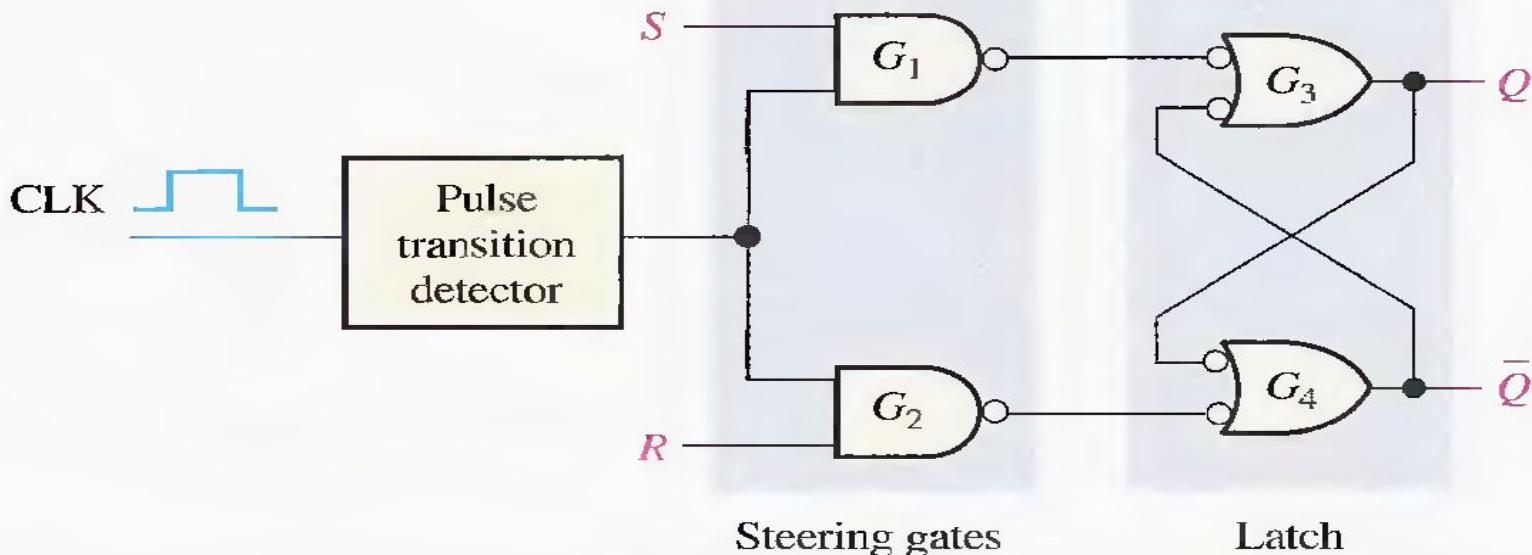
Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET
0	↑	0	1	RESET

(a) Positive-edge triggered

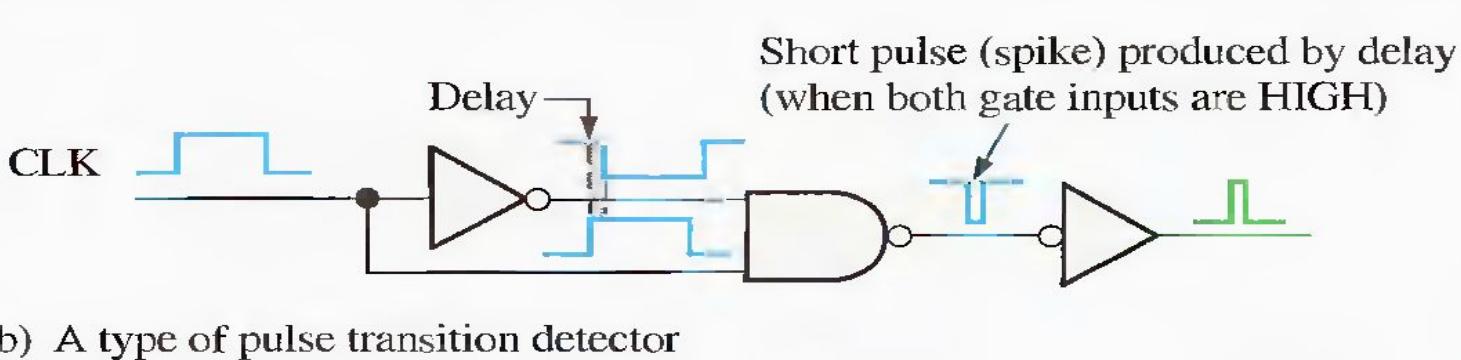
Inputs		Outputs		Comments
D	CLK	Q	\bar{Q}	
1	↓	1	0	SET
0	↓	0	1	RESET

(b) Negative-edge triggered

A Method of Edge-Triggering

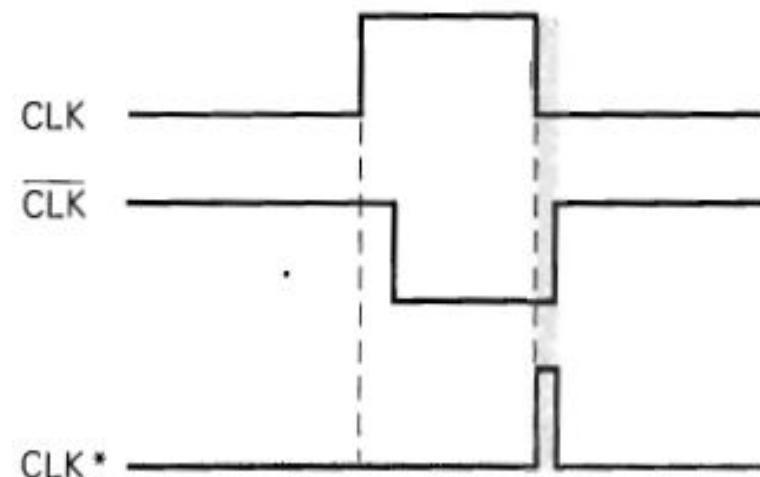
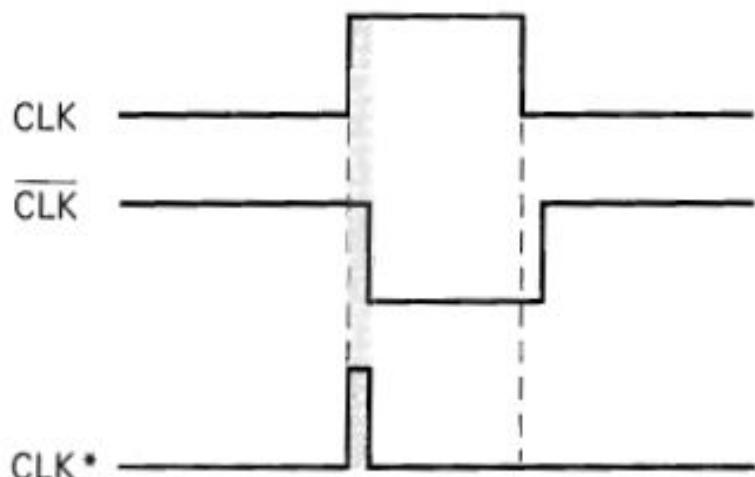
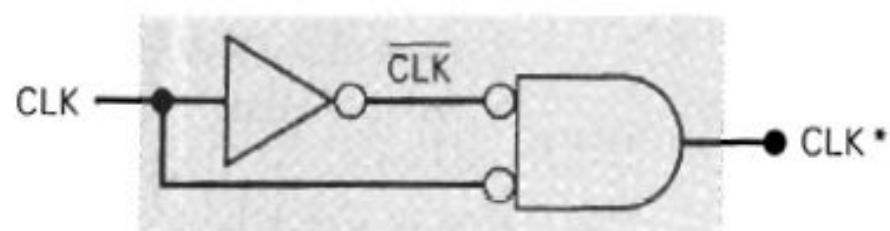
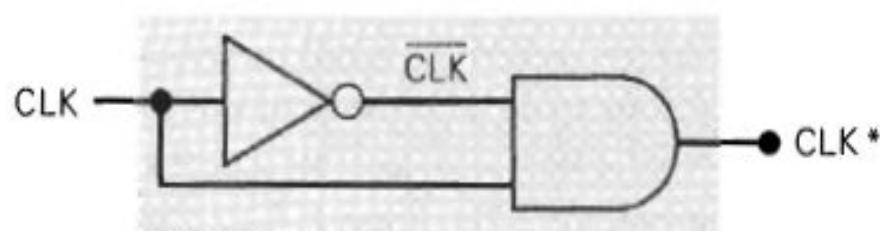
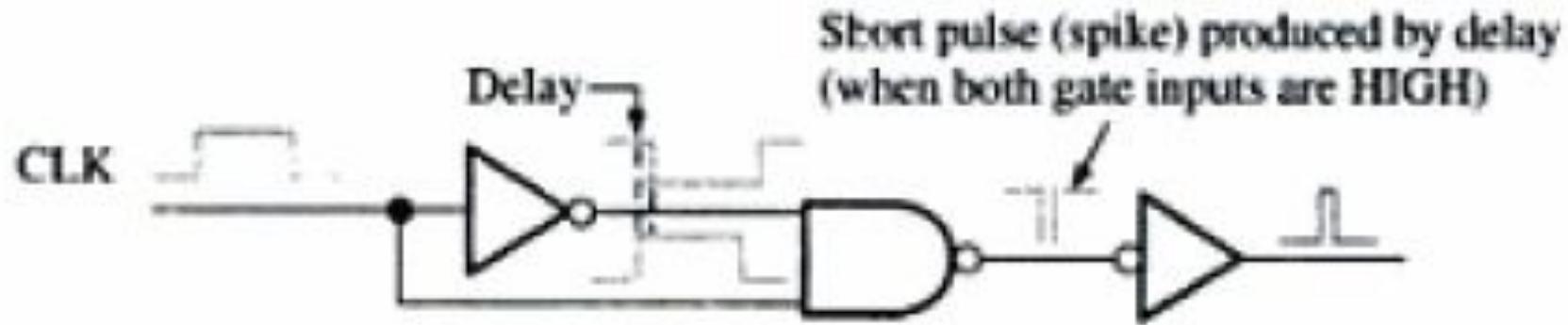


(a) A simplified logic diagram for a positive edge-triggered S-R flip-flop

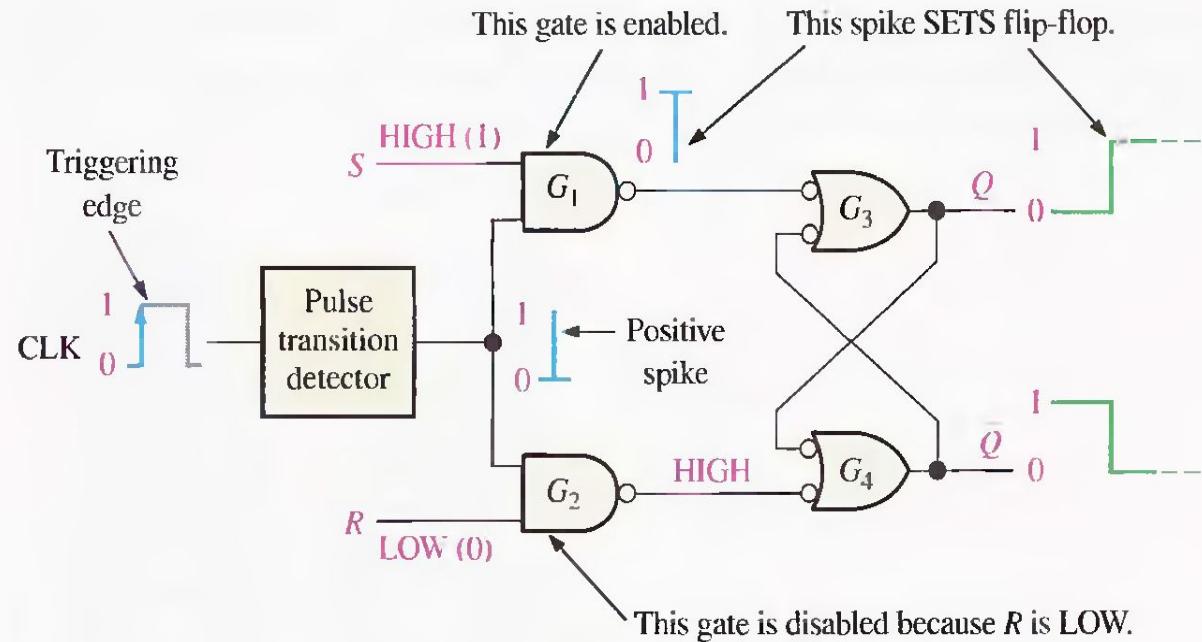


(b) A type of pulse transition detector

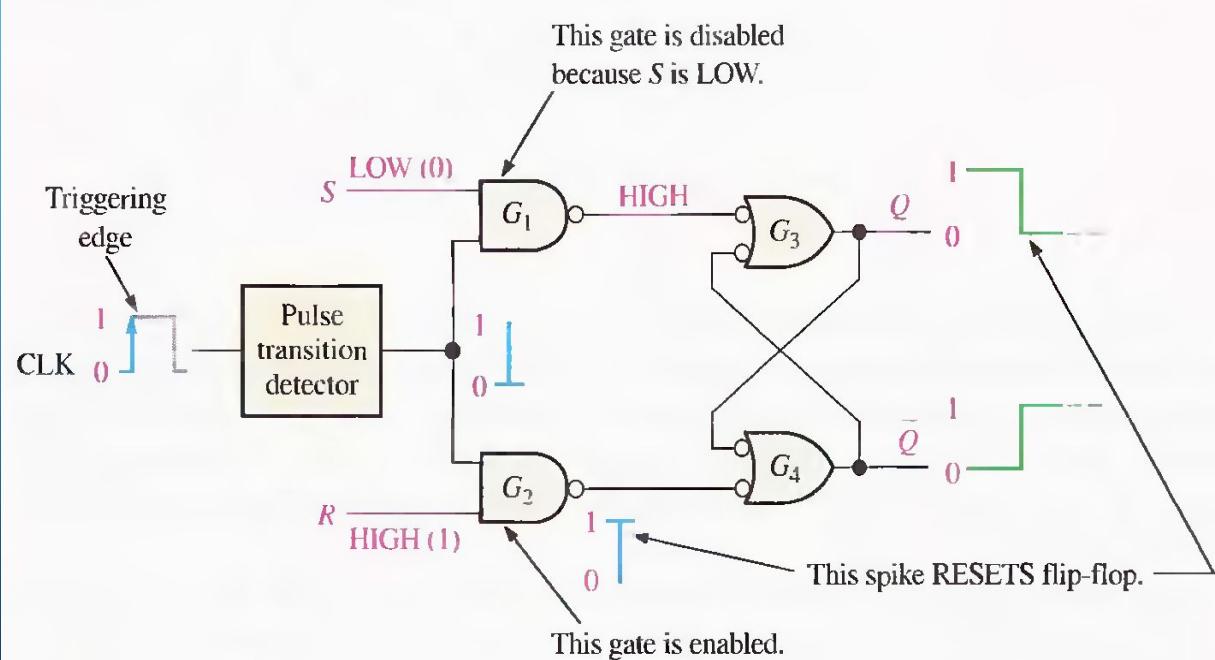
A type of Pulse Transition detector



Flip-flop making a transition from the RESET state to the SET state on the positive-going edge of the clock pulse.

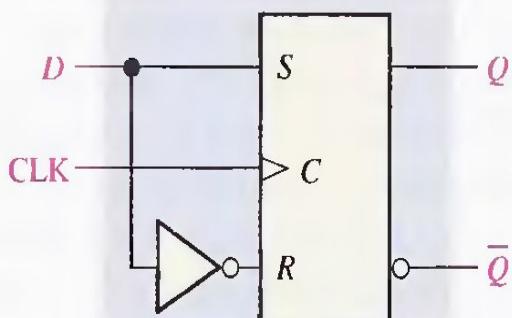


Flip-flop making a transition from the SET state to the RESET state on the positive-going edge of the clock pulse.



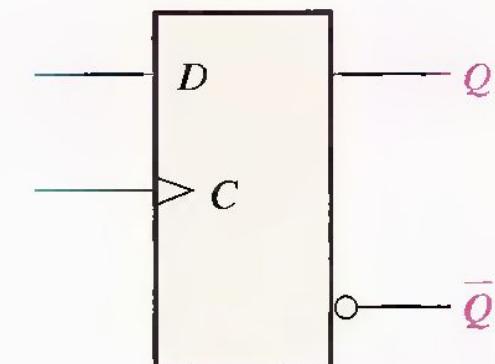
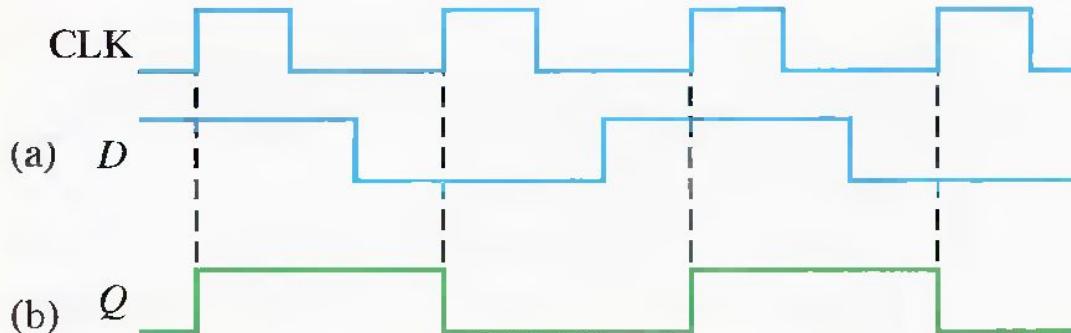
The Edge-Triggered D Flip-Flop

The **D flip-flop** is useful when a single data bit (1 or 0) is to be stored.



INPUTS		OUTPUTS		COMMENTS
D	CLK	Q	\bar{Q}	
1	↑	1	0	SET (stores a 1)
0	↑	0	1	RESET (stores a 0)

↑ = clock transition LOW to HIGH

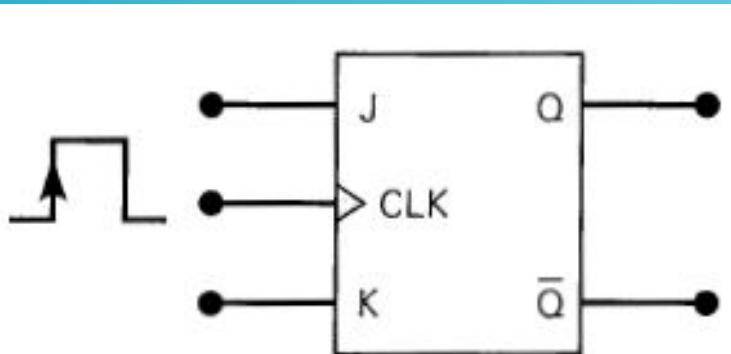


The Edge-Triggered J-K Flip-Flop

The J and K inputs control the state of the FF in the same ways as the S and C input do for the clocked S-C Flip Flop except one major difference:

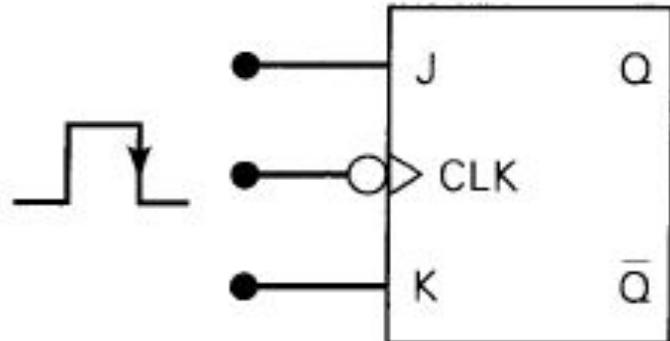
The J=K=1 condition does not result in an ambiguous output.

For this condition J=K=1, the FF will always go to its opposite state upon the positive transition of the clock signal. This is called the



J	K	CLK	Q
0	0	↑	Q_0 (no change)
1	0	↑	1
0	1	↑	0
1	1	↑	\bar{Q}_0 (toggles)

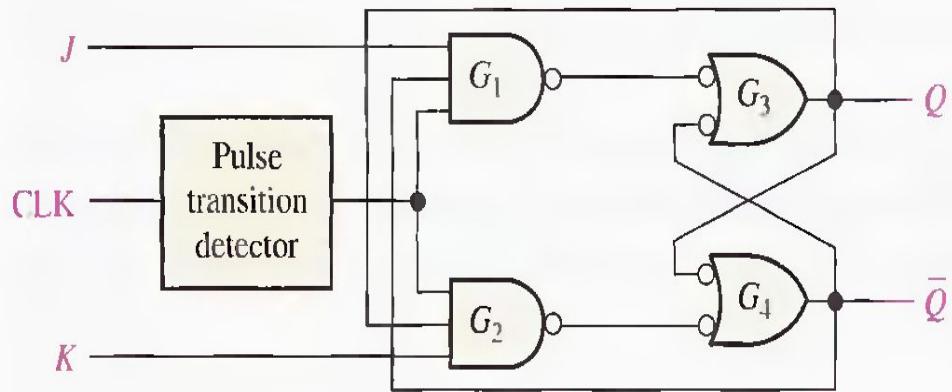
J-K flip-flop that triggers only on negative-going transitions.



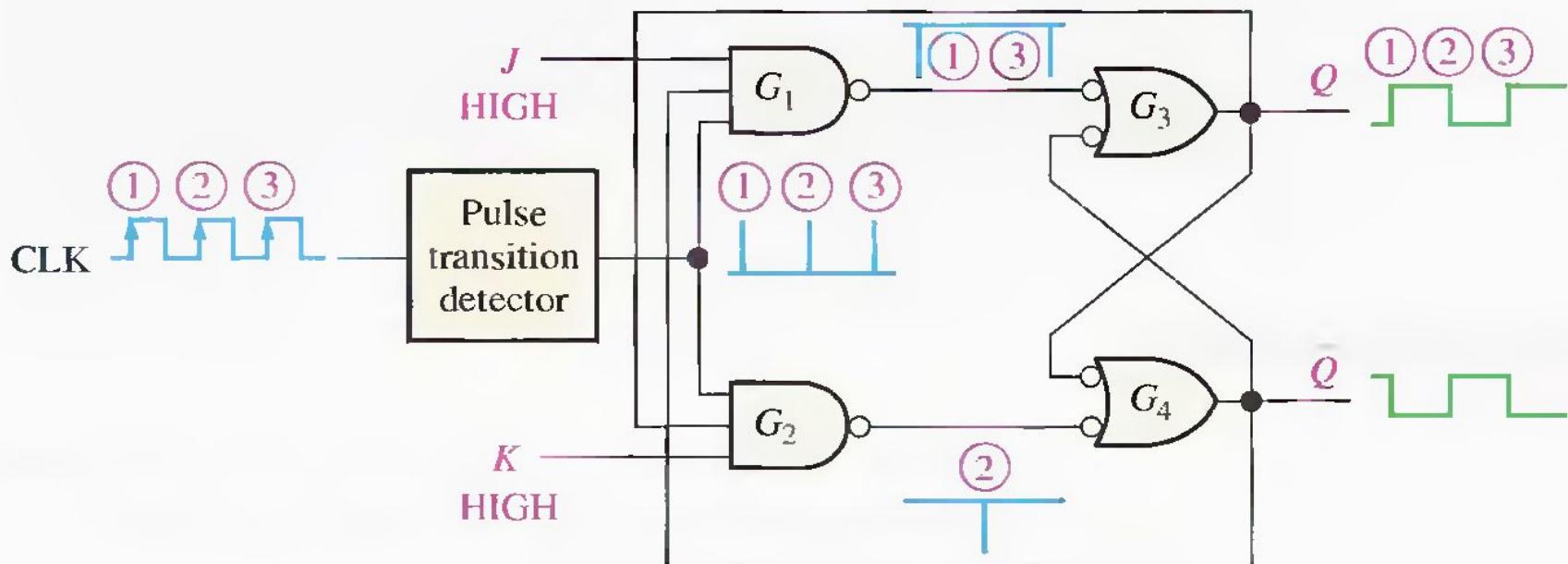
J	K	CLK	Q
0	0	↓	Q_0 (no change)
1	0	↓	1
0	1	↓	0
1	1	↓	\bar{Q}_0 (toggles)

The Edge-Triggered J-K Flip-Flop

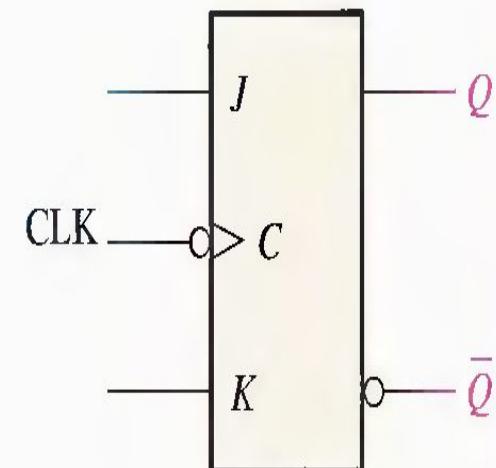
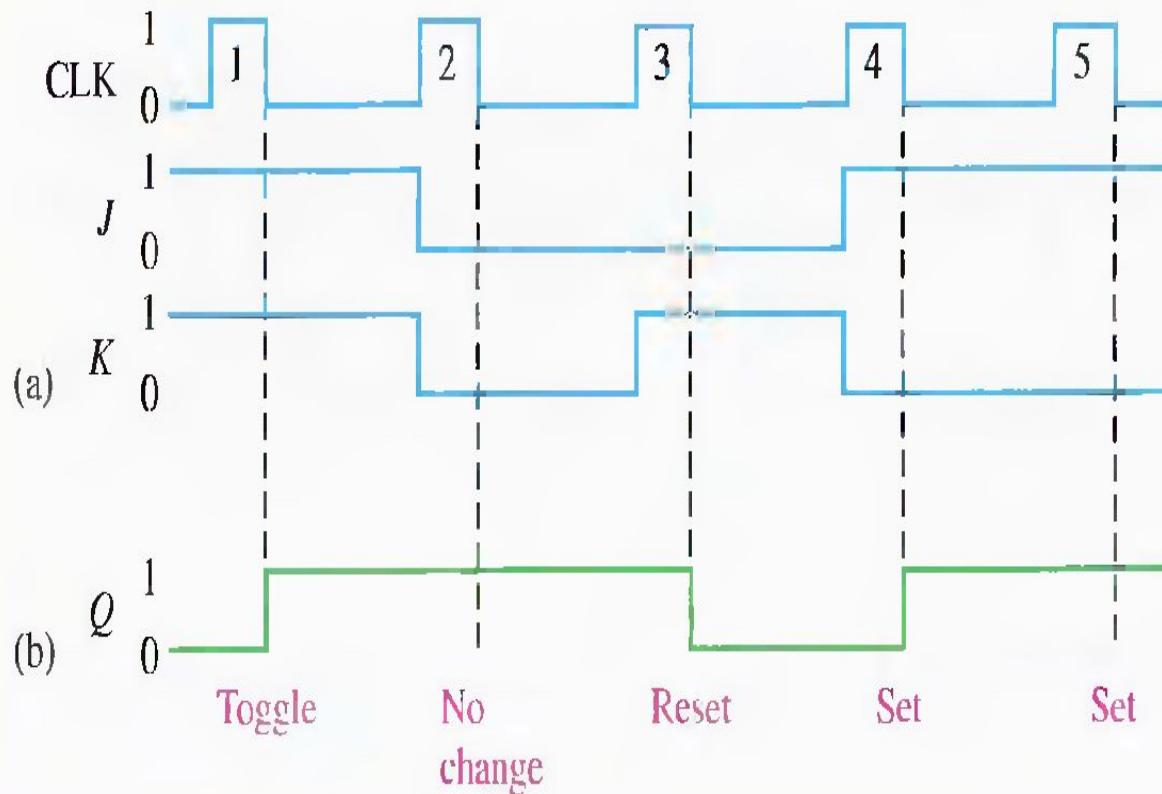
A simplified logic diagram for a positive edge-triggered J-K flip-flop.



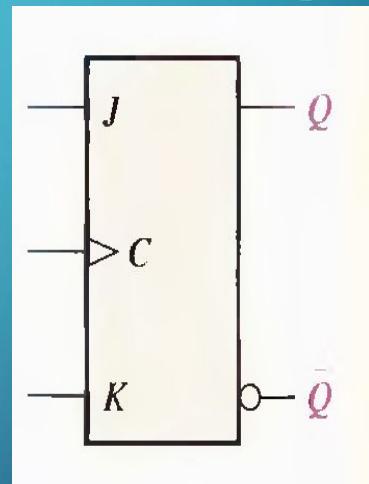
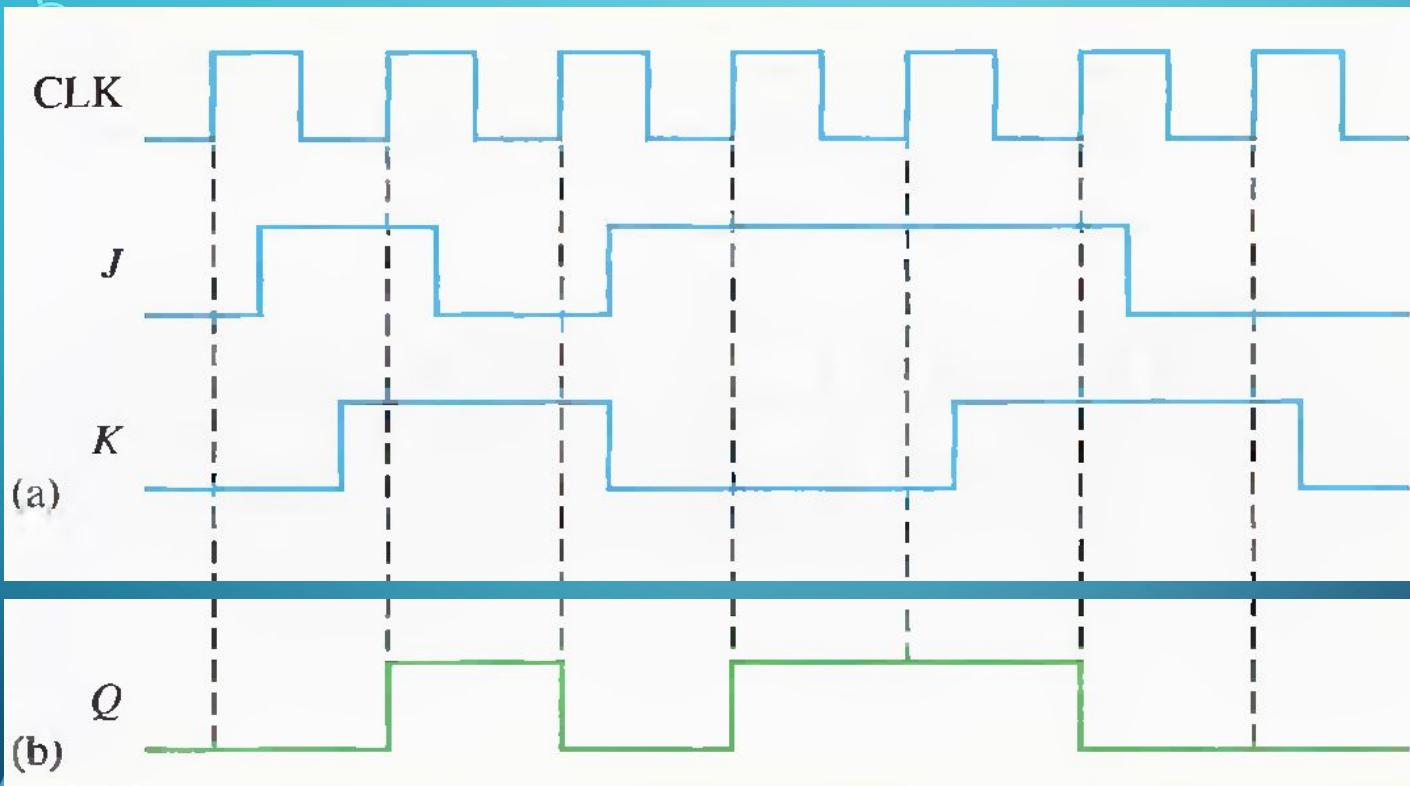
Transitions illustrating the toggle operation when $J = 1$ and $K = 1$.



The waveforms in Figure are applied to the J , K , and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.



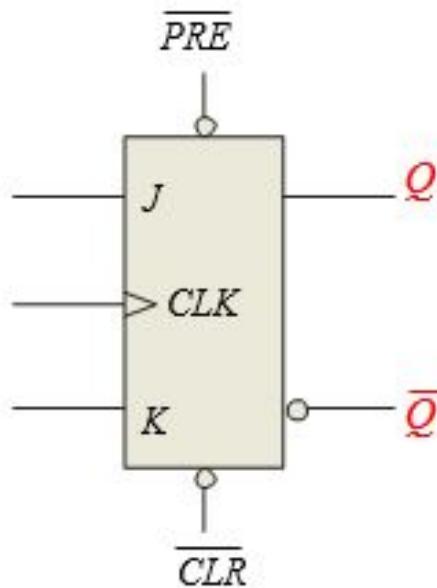
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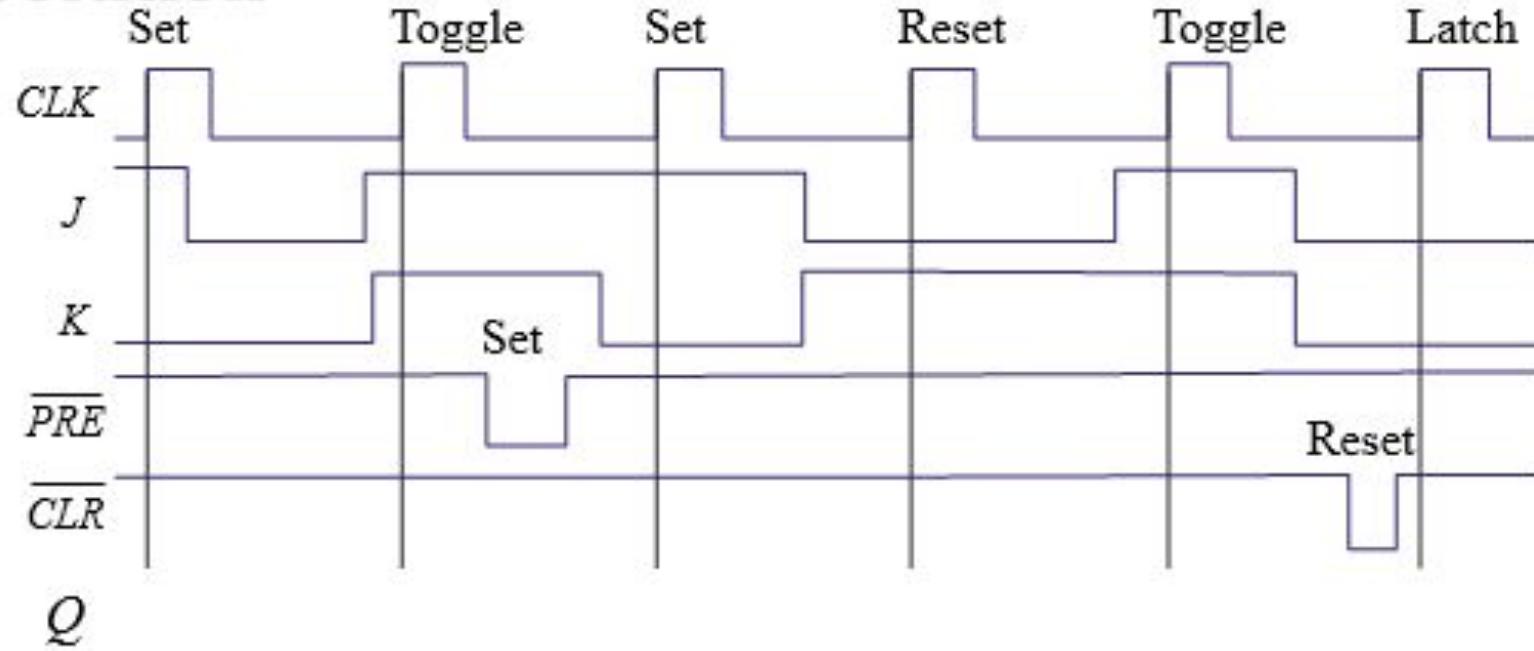


Flip-flops

Synchronous inputs are transferred in the triggering edge of the clock (for example the D or $J-K$ inputs). Most flip-flops have other inputs that are *asynchronous*, meaning they affect the output independent of the clock.

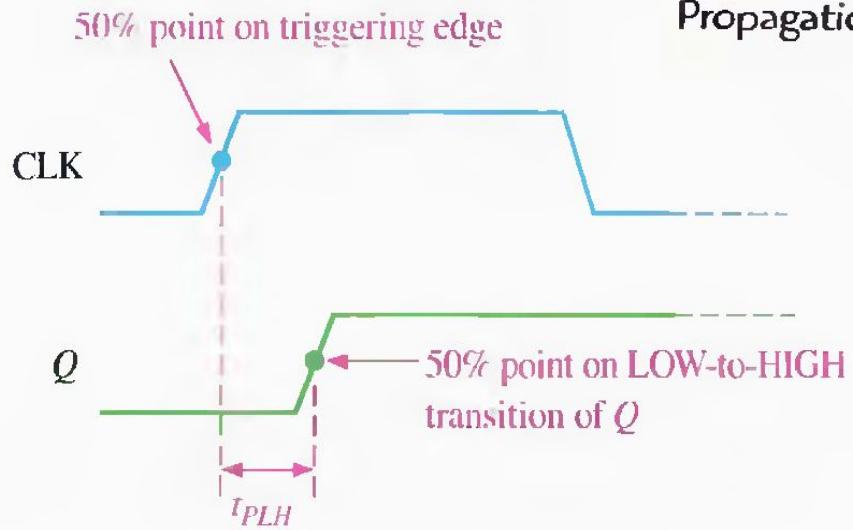
Two such inputs are normally labeled preset (PRE) and clear (CLR). These inputs are usually active LOW. A J-K flip flop with active LOW preset and CLR is shown.



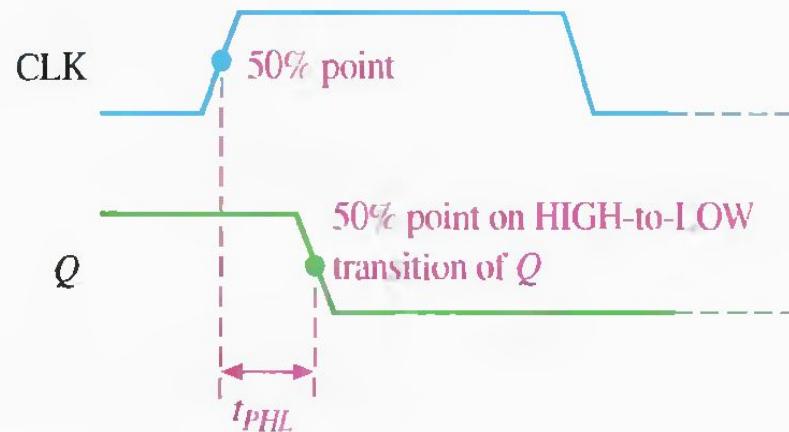


FLIP-FLOP OPERATING CHARACTERISTICS

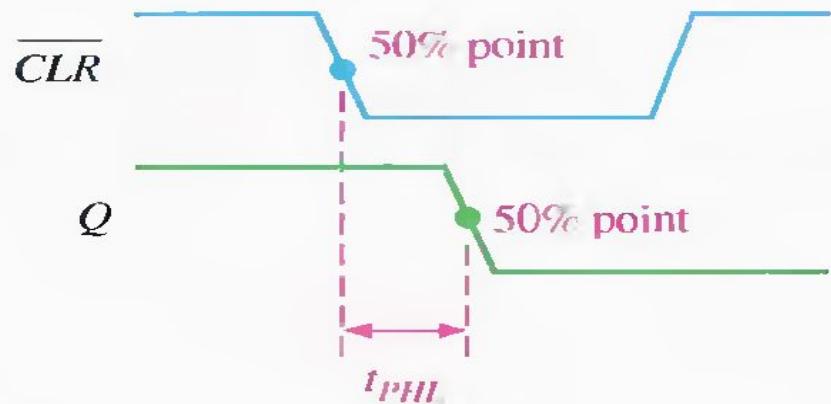
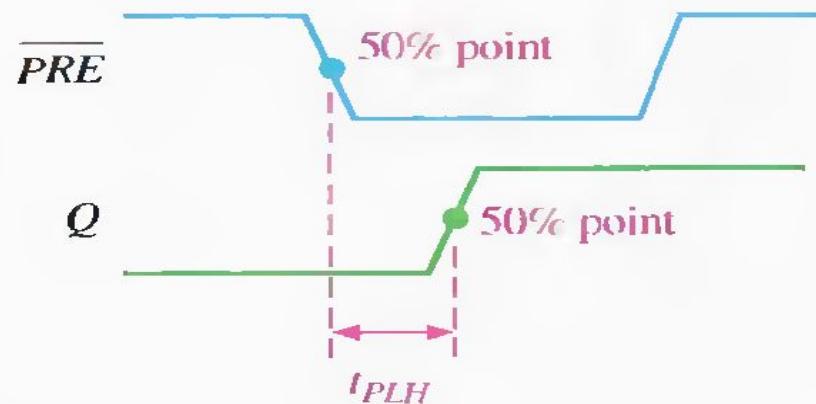
Propagation Delay Times



Propagation delays, clock to output.

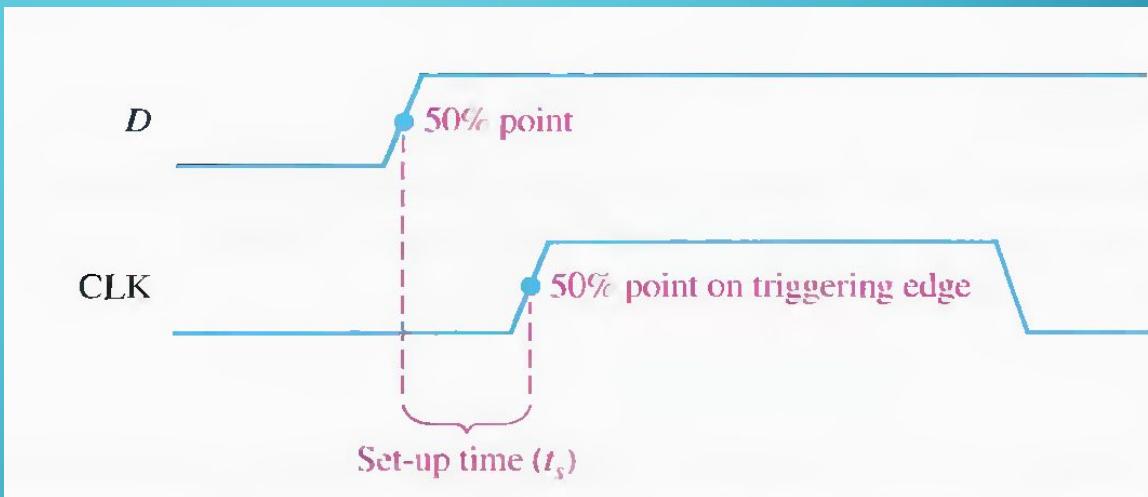


Propagation delays, preset input to output and clear input to output.



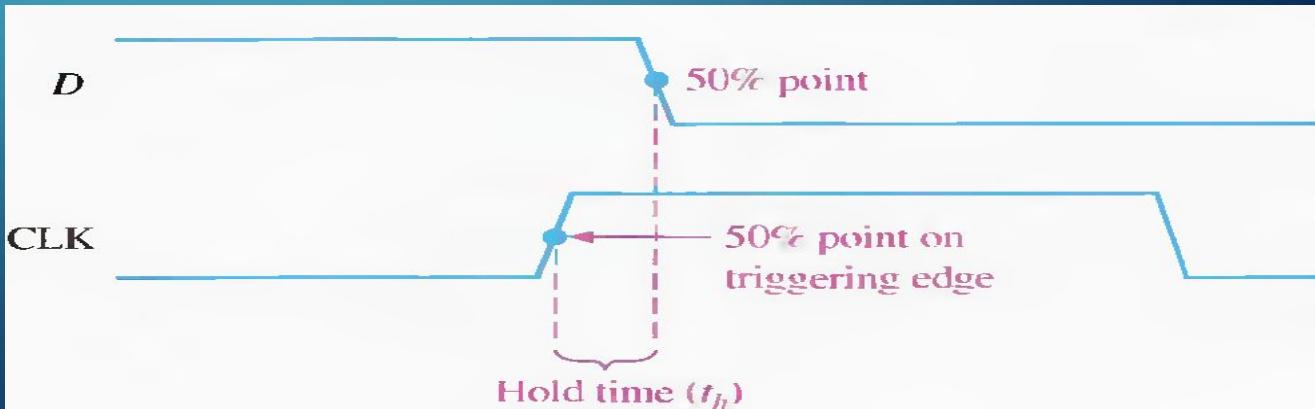
Set-up Time

The set-up time (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Hold Time

The hold time (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Maximum Clock Frequency

The maximum clock frequency (f_{\max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5 \text{ V} \times 5 \text{ mA} = 25 \text{ mW}$$

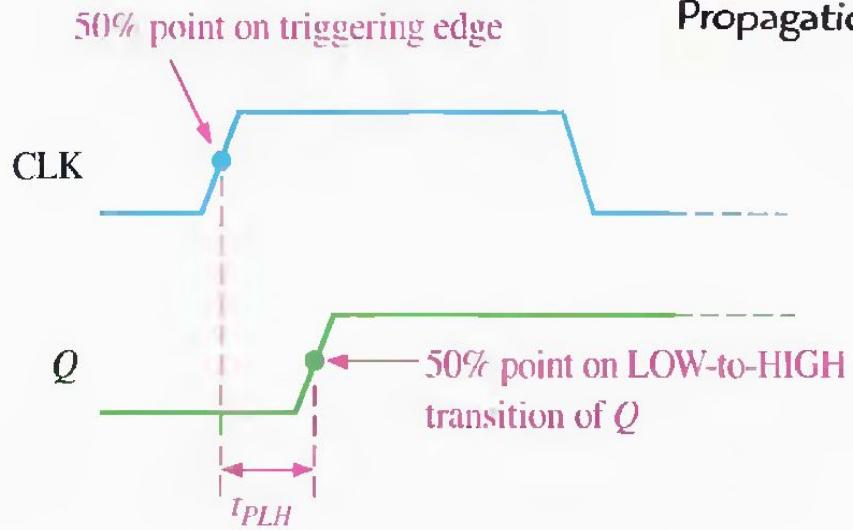
Comparison of Specific Flip-Flops

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

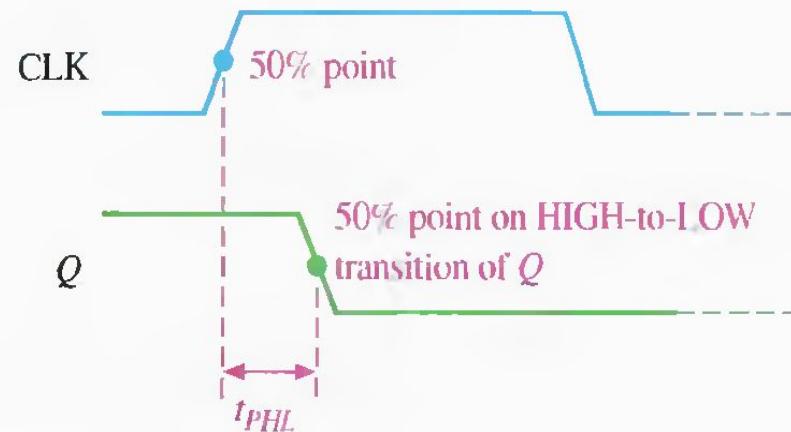
PARAMETER	CMOS		TTL	
	74HC74A	74AHC74	74LS74A	74F74
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
t_{PHL} (\overline{CLR} to Q)	18 ns	4.8 ns	40 ns	9.0 ns
t_{PLH} (\overline{PRE} to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_w (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_w (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_w(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

FLIP-FLOP OPERATING CHARACTERISTICS

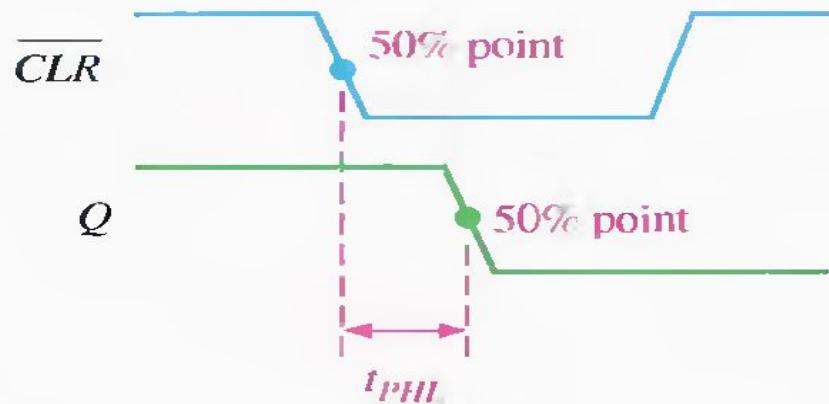
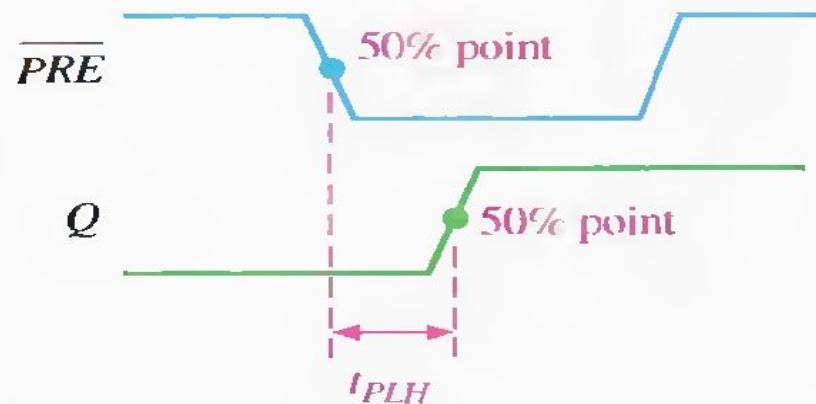
Propagation Delay Times



Propagation delays, clock to output.

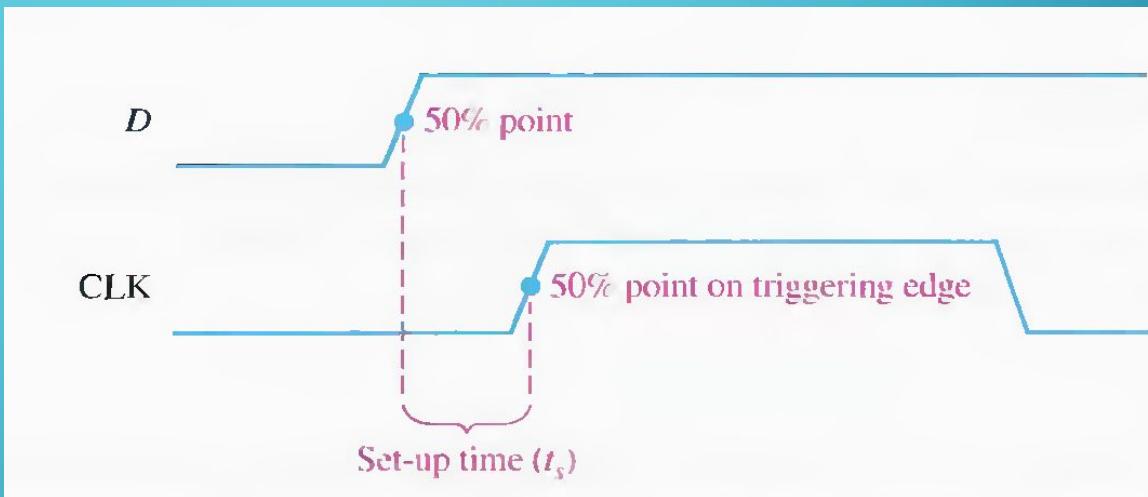


Propagation delays, preset input to output and clear input to output.



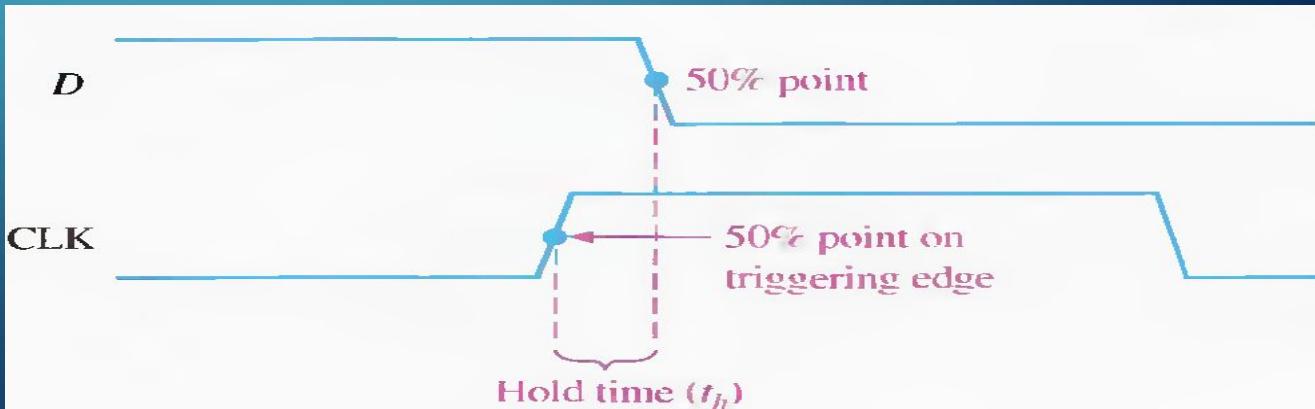
Set-up Time

The set-up time (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or S and R, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Hold Time

The hold time (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. for a D flip-flop.



Maximum Clock Frequency

The maximum clock frequency (f_{\max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

Power Dissipation

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} \times I_{CC} = 5 \text{ V} \times 5 \text{ mA} = 25 \text{ mW}$$

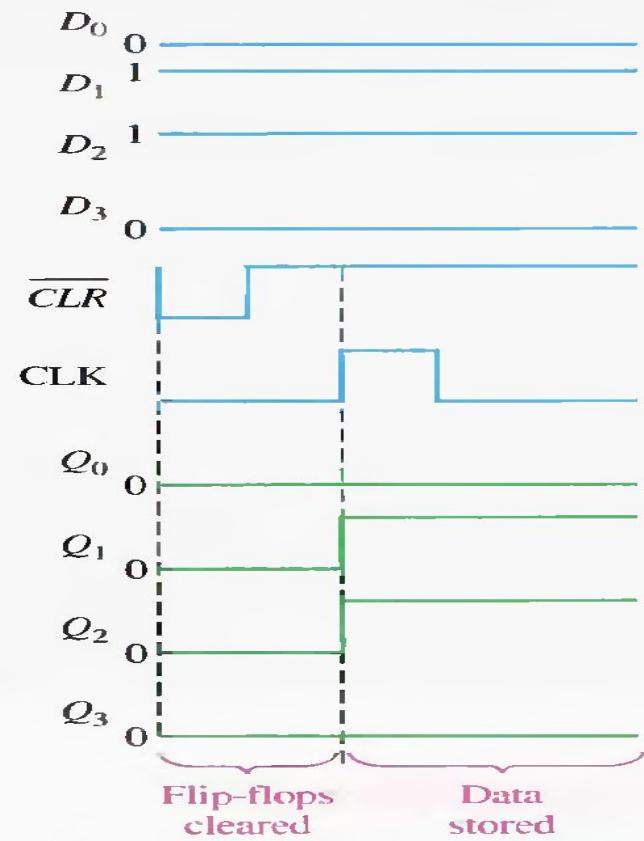
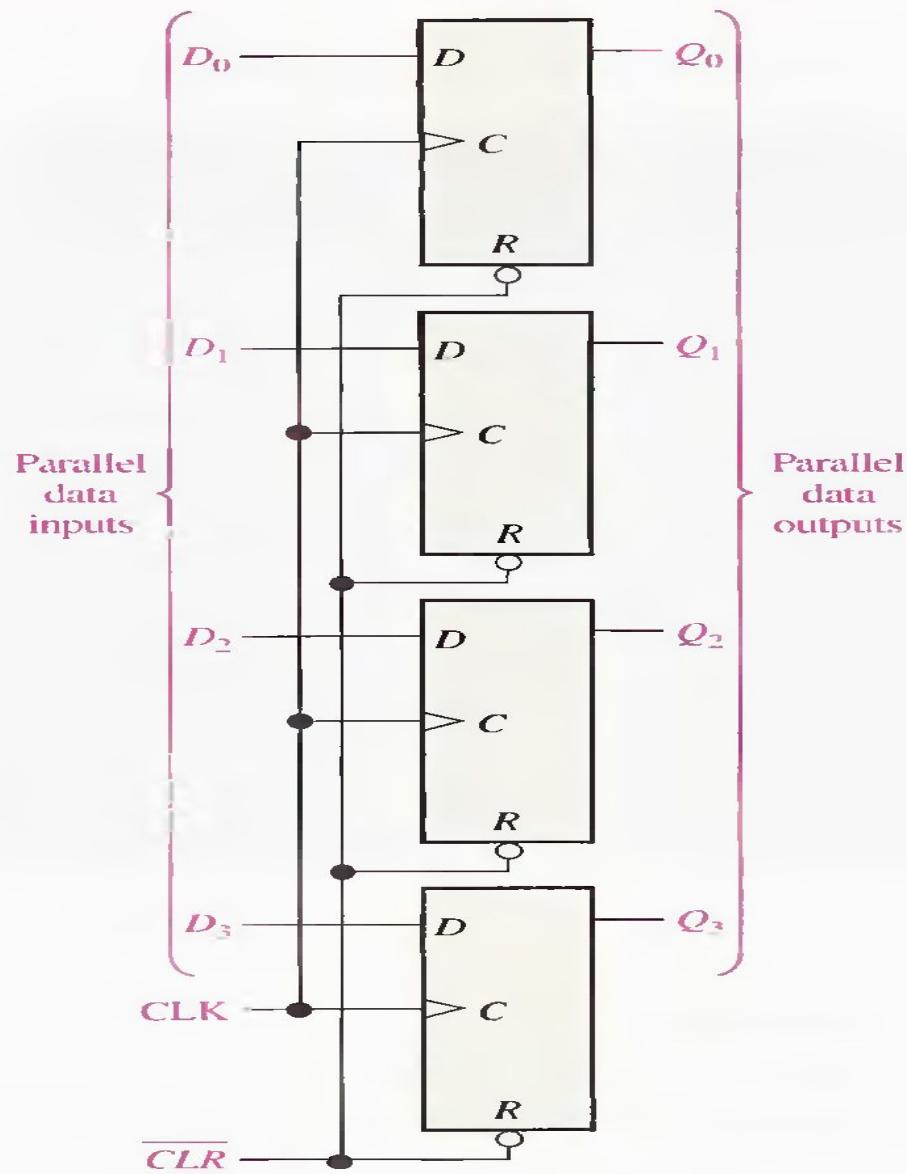
Comparison of Specific Flip-Flops

Comparison of operating parameters for four IC families of flip-flops of the same type at 25°C.

PARAMETER	CMOS		TTL	
	74HC74A	74AHC74	74LS74A	74F74
t_{PHL} (CLK to Q)	17 ns	4.6 ns	40 ns	6.8 ns
t_{PLH} (CLK to Q)	17 ns	4.6 ns	25 ns	8.0 ns
t_{PHL} (\overline{CLR} to Q)	18 ns	4.8 ns	40 ns	9.0 ns
t_{PLH} (\overline{PRE} to Q)	18 ns	4.8 ns	25 ns	6.1 ns
t_s (set-up time)	14 ns	5.0 ns	20 ns	2.0 ns
t_h (hold time)	3.0 ns	0.5 ns	5 ns	1.0 ns
t_w (CLK HIGH)	10 ns	5.0 ns	25 ns	4.0 ns
t_w (CLK LOW)	10 ns	5.0 ns	25 ns	5.0 ns
$t_w(\overline{CLR}/\overline{PRE})$	10 ns	5.0 ns	25 ns	4.0 ns
f_{max}	35 MHz	170 MHz	25 MHz	100 MHz
Power, quiescent	0.012 mW	1.1 mW		
Power, 50% duty cycle			44 mW	88 mW

FLIP-FLOP APPLICATIONS

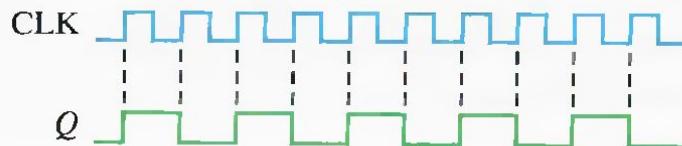
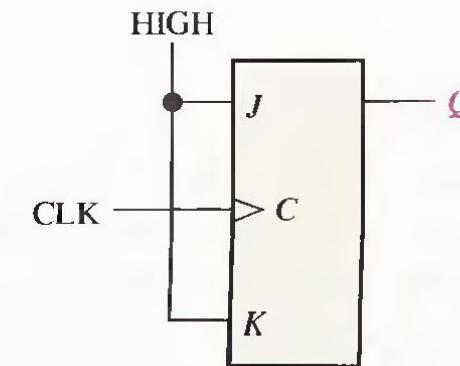
Parallel Data Storage



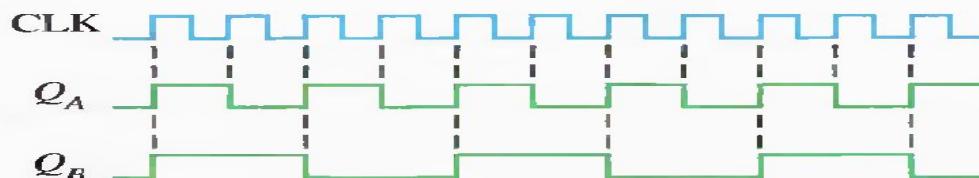
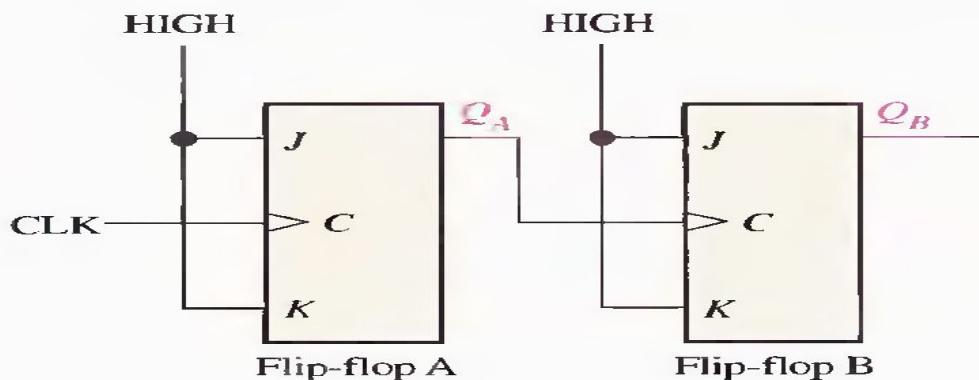
(b)

Frequency Division

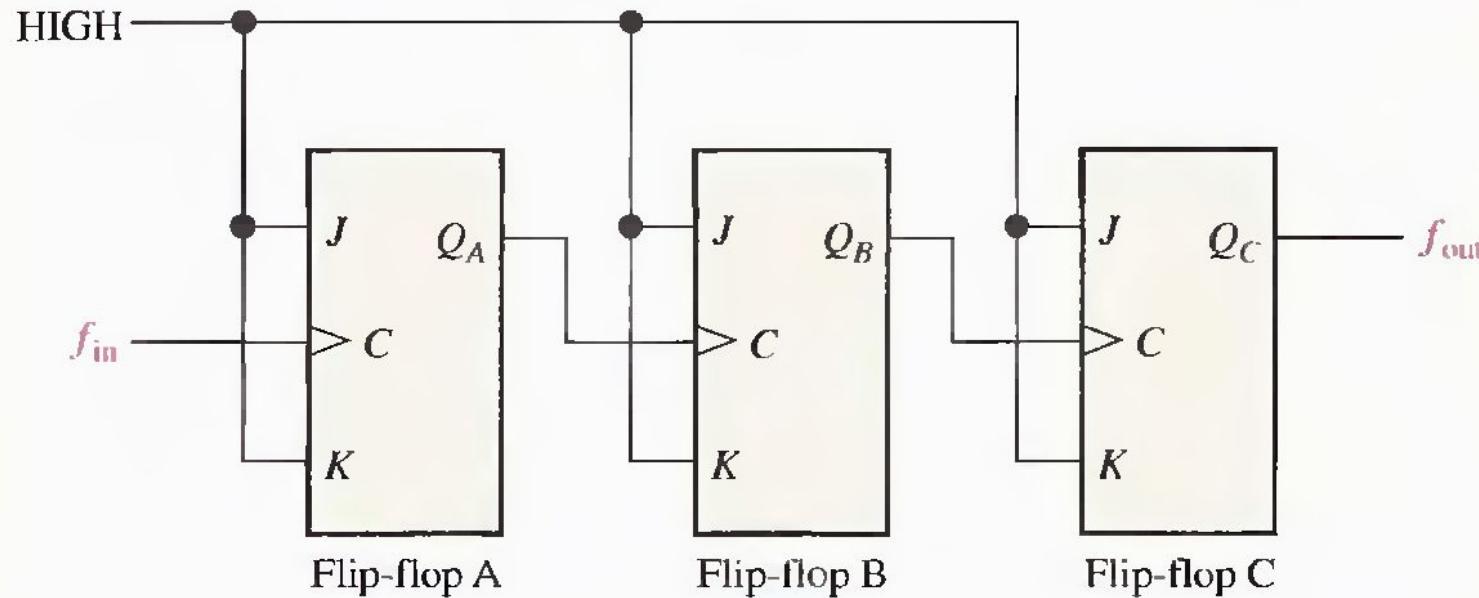
The J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.



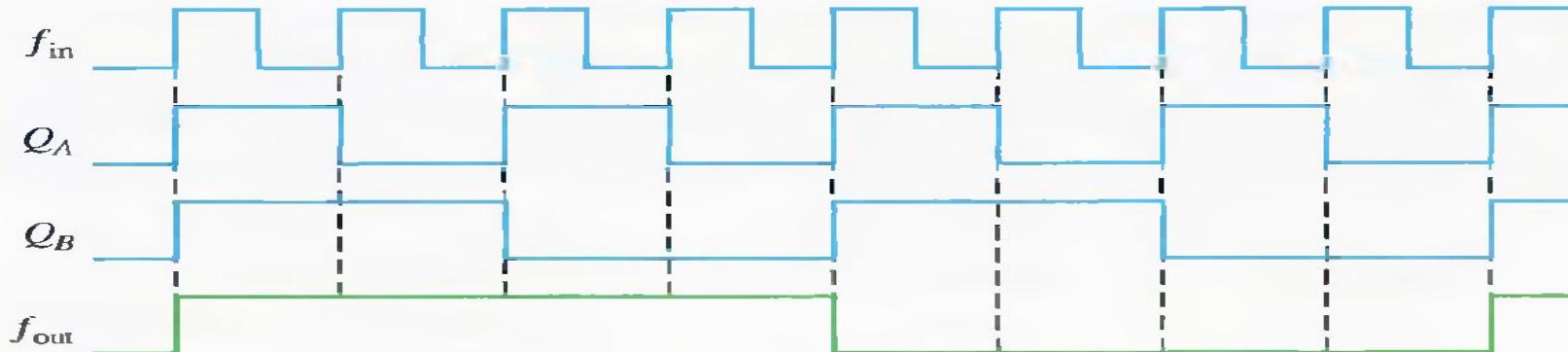
Example of two J-K flip-flops used to divide the clock frequency by 4. Q_A is one-half and Q_B is one-fourth the frequency of CLK.



Develop the f_{out} waveform for the circuit in Figure when an 8 kHz square wave input is applied to the clock input of flip-flop A.

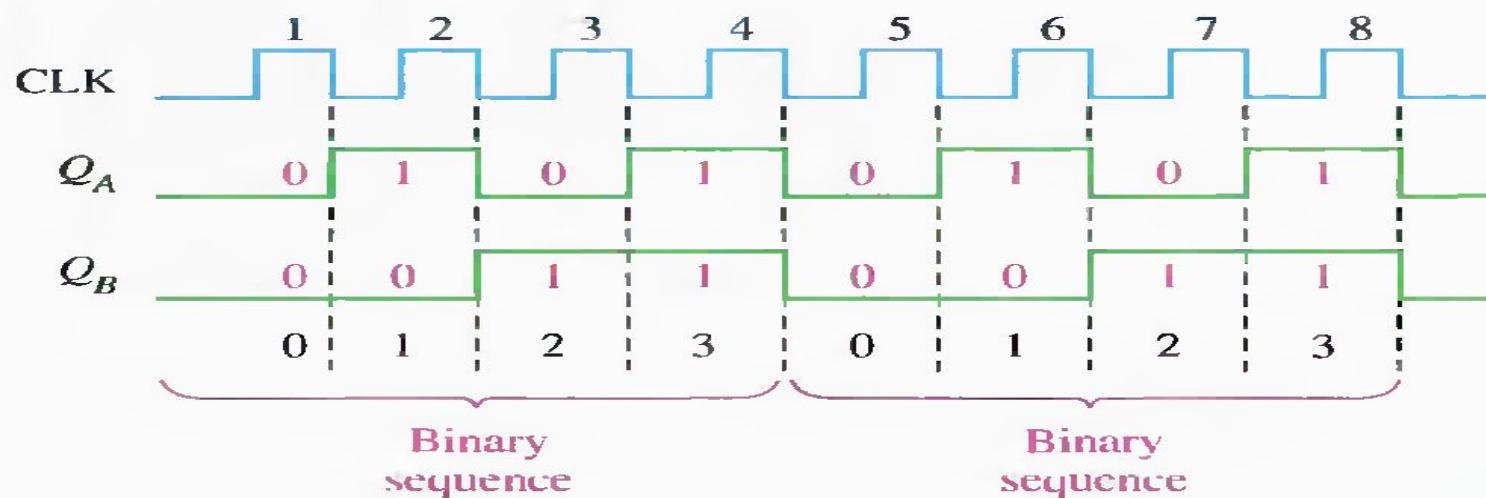
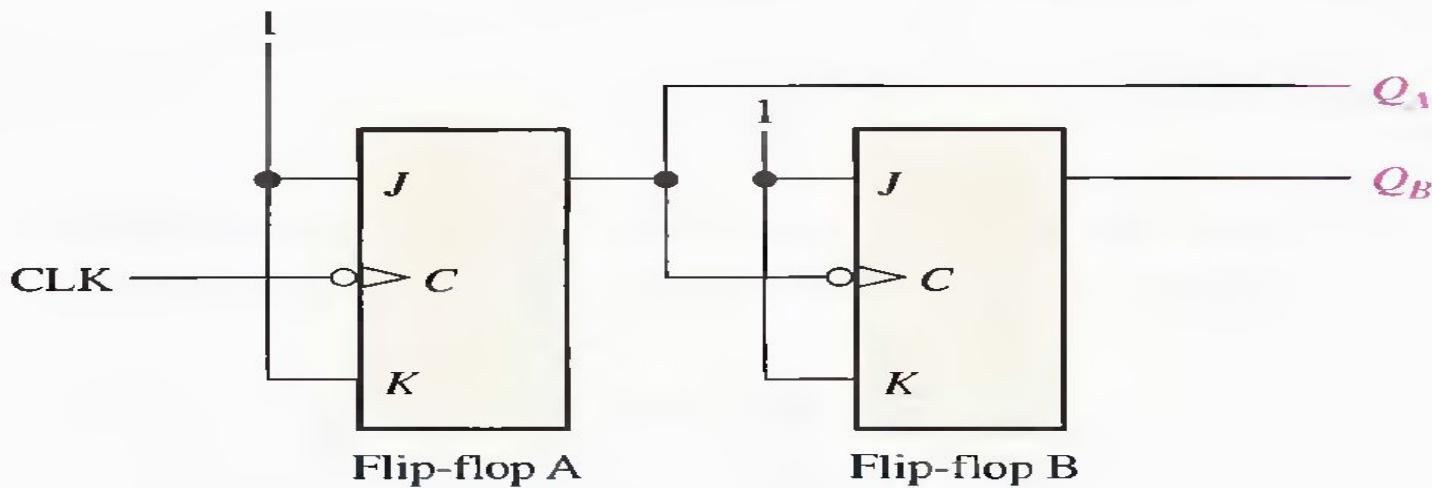


The three flip-flops are connected to divide the input frequency by eight ($2^3 = 8$)

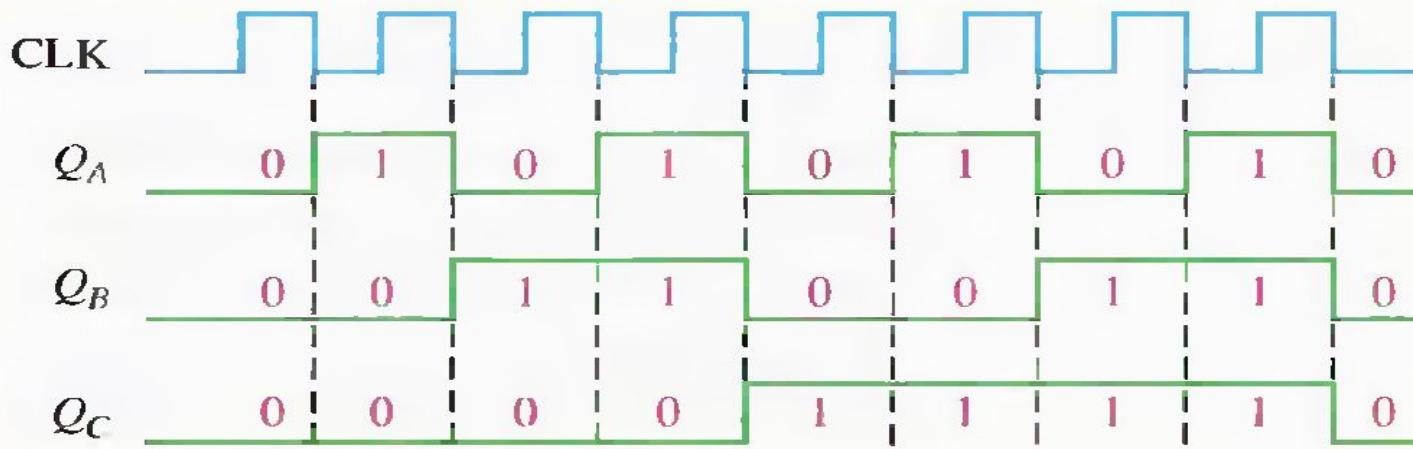
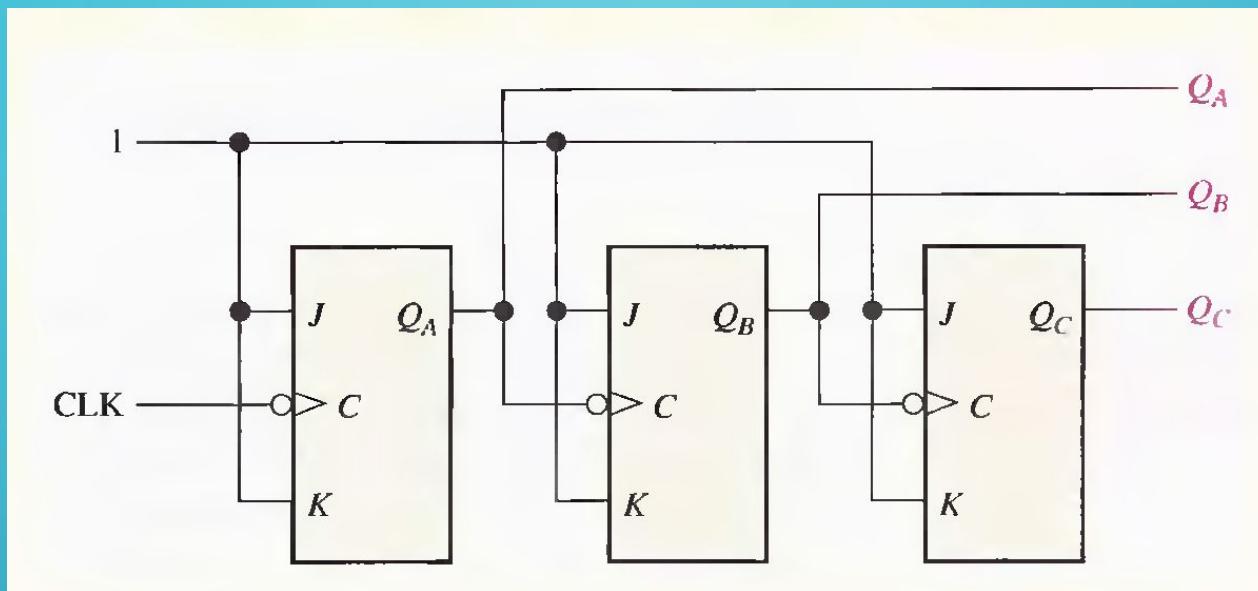


Counting

Flip-flops used to generate a binary count sequence. Two repetitions (00, 01, 10, 11) are shown.



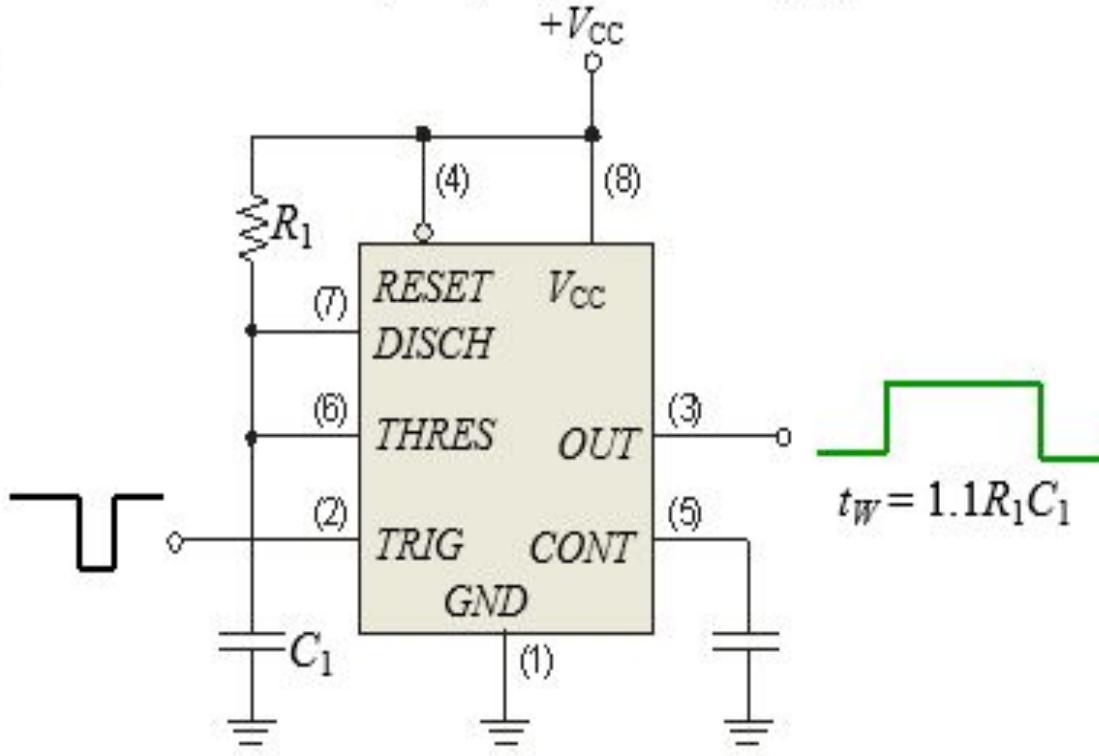
Determine the output waveforms in relation to the clock for Q_A , Q_B , and Q_C



The 555 timer

The 555 timer can be configured in various ways, including as a one-shot. A basic one shot is shown. The pulse width is determined by R_1C_1 and is approximately $t_W = 1.1R_1C_1$.

The trigger is a negative-going pulse.

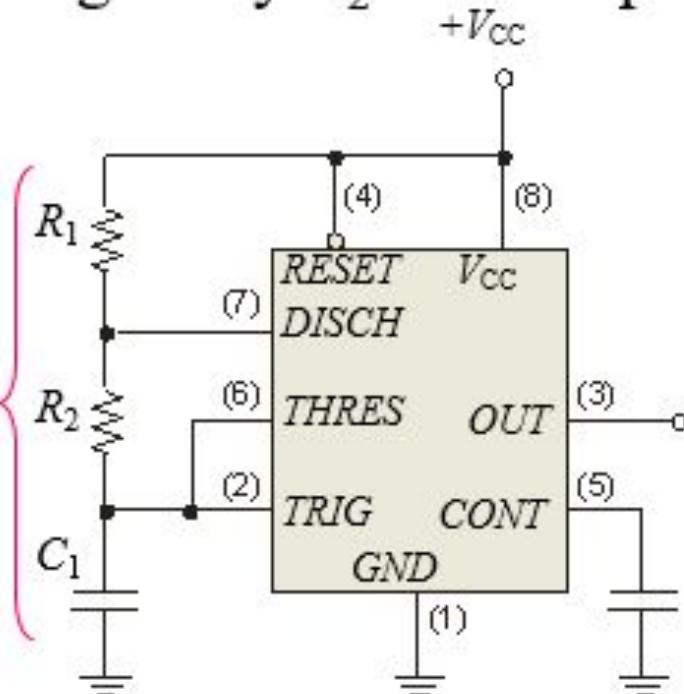


The 555 timer

The 555 can be configured as a basic astable multivibrator with the circuit shown. In this circuit C_1 charges through R_1 and R_2 and discharges through only R_2 . The output frequency is given by:

$$f = \frac{1.44}{(R_1 + 2R_2)C_1}$$

The frequency and duty cycle
are set by these components.



Counting in Binary

As you know, the binary count sequence follows a familiar pattern of 0's and 1's as described in Section 2-2 of the text.

The next bit changes on every fourth number.

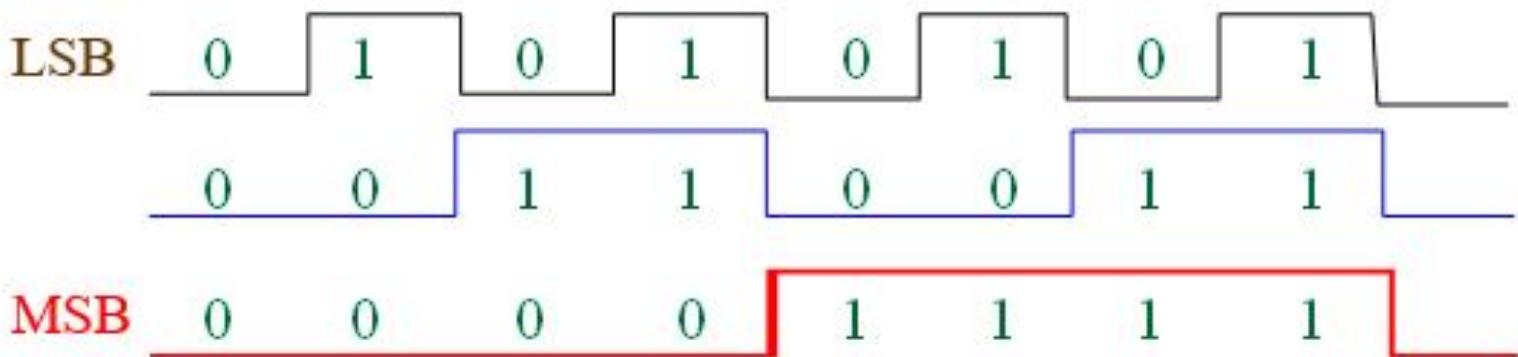
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

LSB changes on every number.

The next bit changes on every other number.

Counting in Binary

A counter can form the same pattern of 0's and 1's with logic levels. The first stage in the counter represents the least significant bit – notice that these waveforms follow the same pattern as counting in binary.

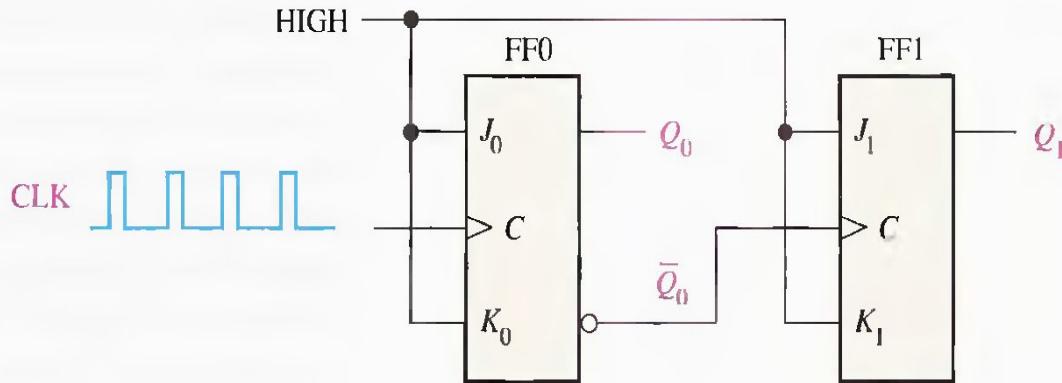


ASYNCHRONOUS COUNTER OPERATION

The term **asynchronous** refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An **asynchronous counter** is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

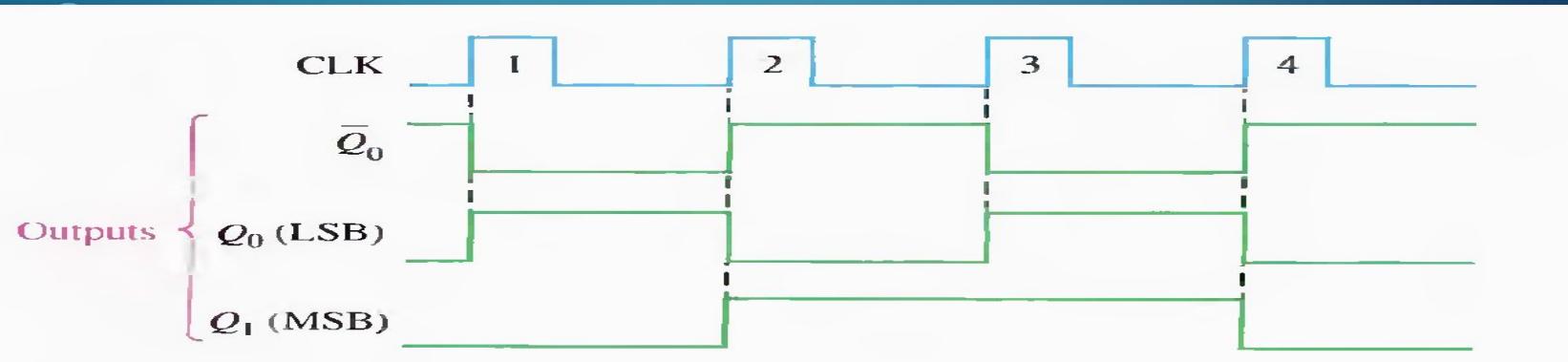
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A 2-Bit Asynchronous Binary Counter

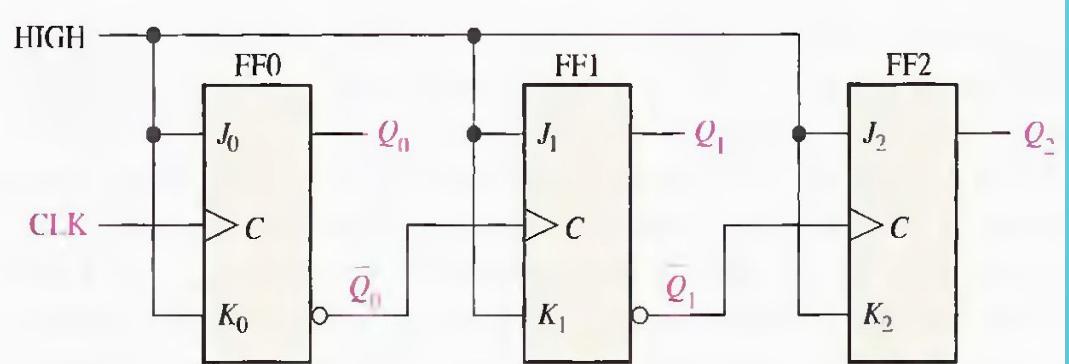


Asynchronous counters are also known as ripple counters.

CLOCK PULSE	Q_1	Q_0
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0



A 3-Bit Asynchronous Binary Counter



CLOCK PULSE	Q_2	Q_1	Q_0
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0

