Assignment 5 [Due Date: 28 May]

Solve and submit the following questions as your assignment 5. Rest of the questions are for your practice.

[Assignment questions: 6,9,10,14,17,20,21,23,25]

1. If the waveforms in Figure 7–70 are applied to an active-HIGH S-R latch, draw the resulting Q output waveform in relation to the inputs. Assume that Q starts LOW.

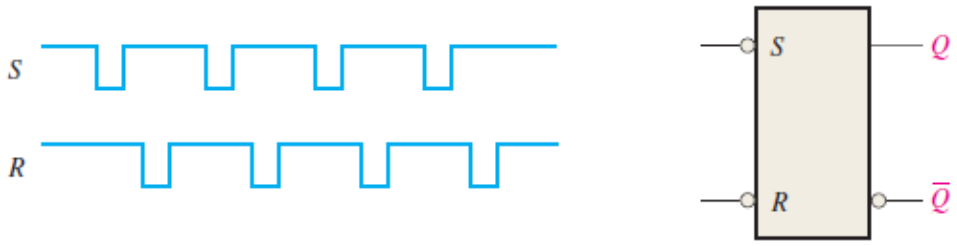


FIGURE 7–70

2. Solve Problem 1 for the input waveforms in Figure 7–71 applied to an active-LOW $\overline{S} - \overline{R}$ latch.

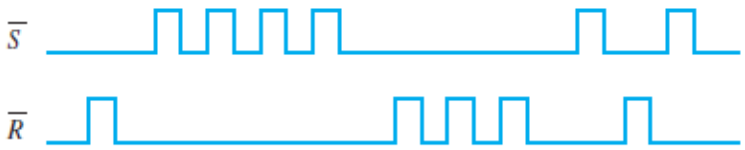


FIGURE 7–71

3. Solve Problem 1 for the input waveform in Figure 7–72.

FIGURE 7–72

4. For a gated S-R latch, determine the Q and $\overline{Q}$ outputs for the inputs in Figure 7–73. Show them in proper relation to the enable input. Assume that Q starts LOW.

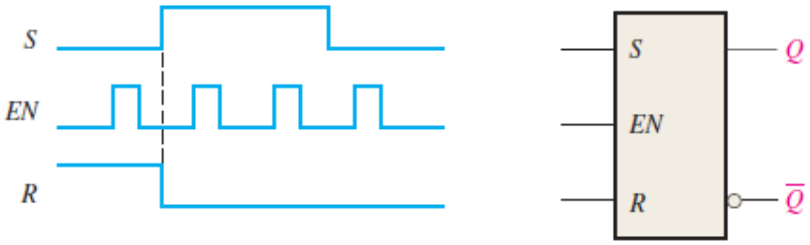


FIGURE 7–73

5. Determine the output of a gated D latch for the inputs in Figure 7–74.

FIGURE 7–74

6. Determine the output of a gated D latch for the inputs in Figure 7–75.

FIGURE 7–75

9. The *Q* output of an edge-triggered D flip-flop is shown in relation to the clock signal in Figure 7–78. Determine the input waveform on the D input that is required to produce this output if the flip-flop is a positive edge-triggered type.

FIGURE 7–78

10. Draw the *Q* output relative to the clock for a D flip-flop with the inputs as shown in Figure 7–79. Assume positive edge-triggering and *Q* initially LOW.

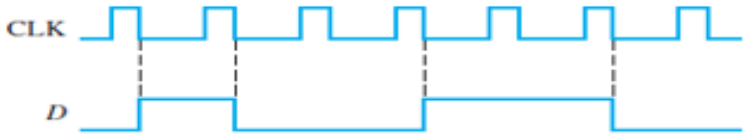


FIGURE 7–79

11. Solve Problem 10 for the inputs in Figure 7–80.

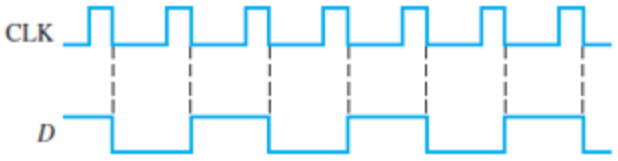


FIGURE 7–80

12. For a positive edge-triggered D flip-flop with the input as shown in Figure 7–81, determine the *Q* output relative to the clock. Assume that *Q* starts LOW.

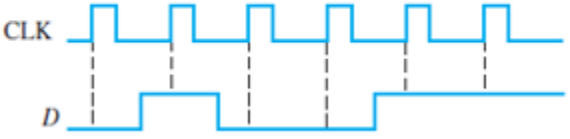


FIGURE 7–81

13. Solve Problem 12 for the input in Figure 7–82.

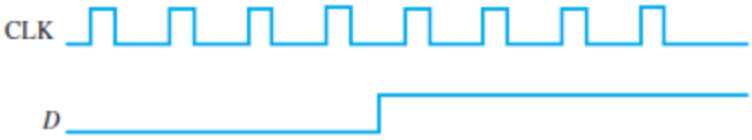


FIGURE 7–82

14. Determine the Q waveform relative to the clock if the signals shown in Figure 7–83 are applied to the inputs of the J-K flip-flop. Assume that Q is initially LOW.

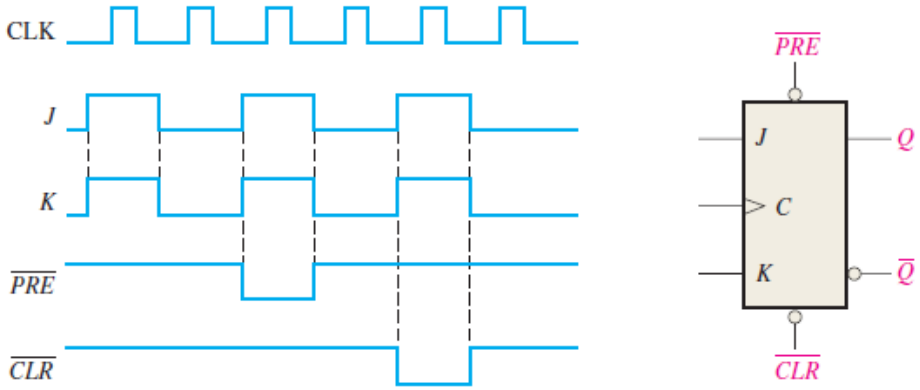


FIGURE 7–83

15. For a negative edge-triggered J-K flip-flop with the inputs in Figure 7–84, develop the Q output waveform relative to the clock. Assume that Q is initially LOW.

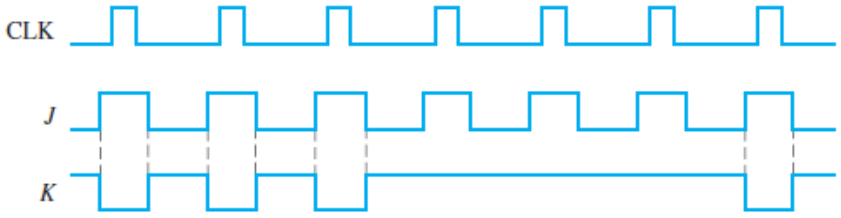
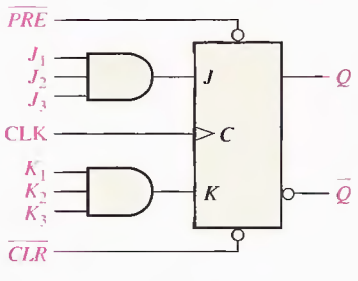


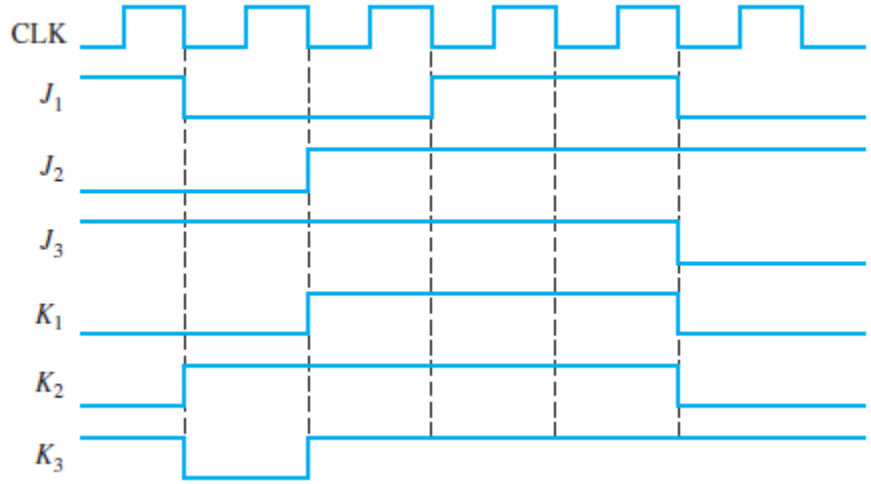
FIGURE 7–84

16. The following serial data are applied to the flip-flop through the AND gates as indicated in Figure. Determine the resulting serial data that appear on the Q output. There is one clock pulse for each bit time. Assume that Q is initially 0 and that PRE and CLR are HIGH. Rightmost bits are applied first.

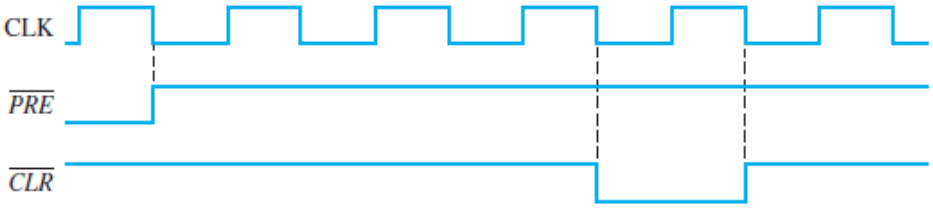
J_1: 1 0 1 0 0 1 1
J_2: 0 1 1 1 0 1 0
J_3: 1 1 1 1 0 0 0
K_1: 0 0 0 1 1 1 0
K_2: 1 1 0 1 1 0 0
K_3: 1 0 1 0 1 0 1



17. For the circuit in Figure -1, complete the timing diagram in Figure 2 by showing the Q output (which is initially LOW). Assume PRE and CLR remain HIGH.



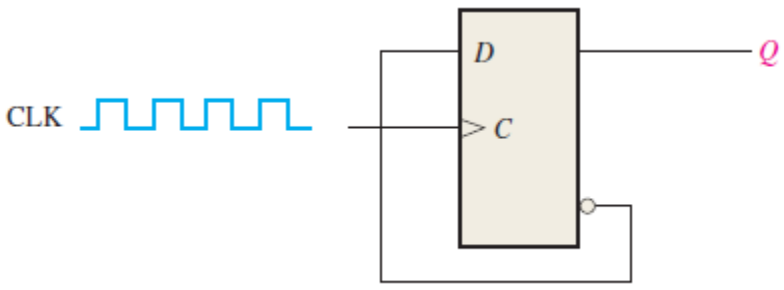
18. Solve Problem 2 with the same J and K inputs but with the PRE and CLR inputs as shown in Figure 3 in relation to the clock.



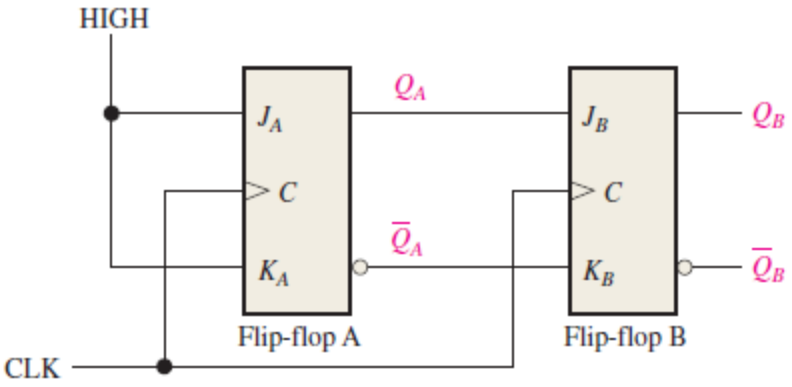
19. Show how to connect a 4-bit asynchronous counter for each of the following moduli. Also for 30kHz clock determine the frequency at the output of each counter.

(a) 9 **(b)** 11 **(c)** 13 **(d)** 14 **(e)** 15

20. A D flip-flop is connected as shown in Figure 7–90. Determine the Q output in relation to the clock. What specific function does this device perform?

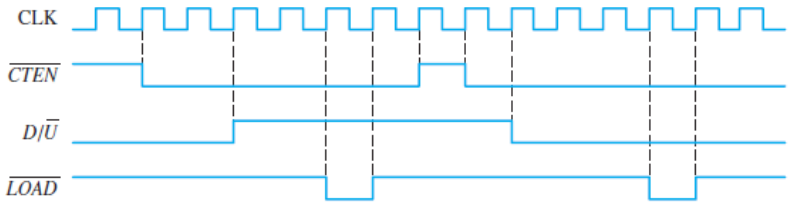


21. For the circuit in Figure, develop a timing diagram for eight clock pulses, showing the QA and QB outputs in relation to the clock.



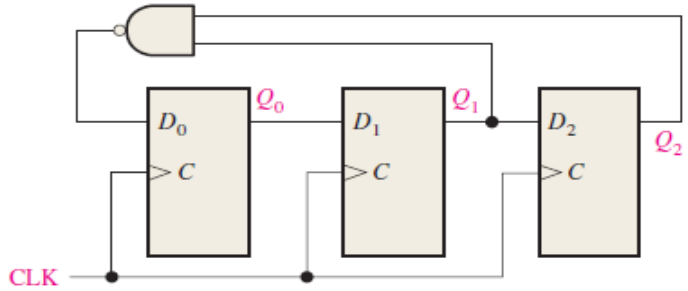
22. Show a complete timing diagram for a 3-bit up/down counter that goes through the following sequence. Indicate when the counter is in the UP mode and when it is in the DOWN mode. Assume positive edge-triggering. 0, 1, 2, 3, 2, 1, 2, 3, 4, 5, 6, 5, 4, 3, 2, 1, 0

23. **Develop t**he Q output waveforms for a 74HC190 up/down counter with the input waveforms shown in Figure. A binary 0 is on the data inputs. Start with a count of 0000.



a.

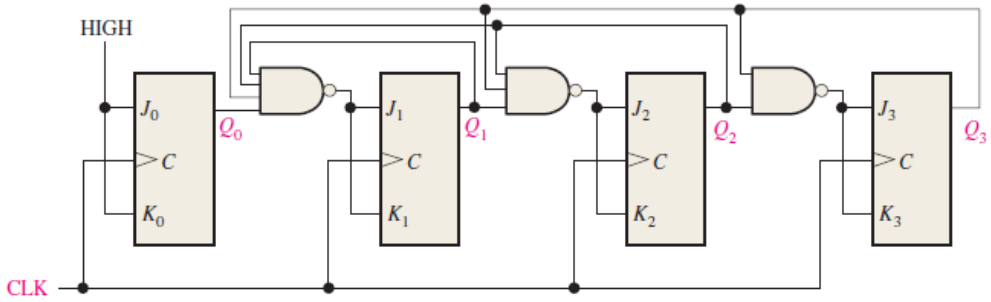
24. Determine the sequence of the counter in Figure.



i.

ii.

25. Determine the sequence of the counter in Figure 9–74. Begin with the counter cleared.



iii.

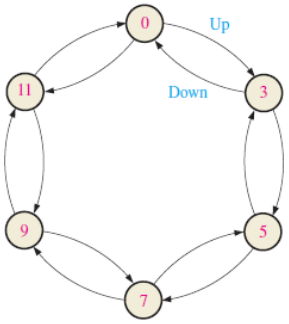
26. Design a counter to produce the following sequence. Use J-K flip-flops. 00, 10, 01, 11, 00, ….

27. Design a counter to produce the following binary sequence. Use J-K flip-flops. 1, 4, 3, 5, 7, 6, 2, 1, ….

b.

28. Design a counter to produce the following binary sequence. Use J-K flip-flops. 0, 9, 1, 8, 2, 7, 3, 6, 4, 5, 0, …

29. Design a binary counter with the sequence shown in the state diagram of Figure. (using D flip flop)



i.

30. Design a counter by using D -flip flop only with the irregular binary count sequence shown in the state diagram of Fig. Include Next-state table, transition table, Karnaugh maps and final circuit.