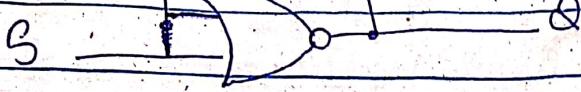


Set-reset

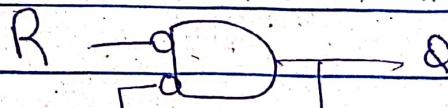
A Latch is a type of bistable logic device.



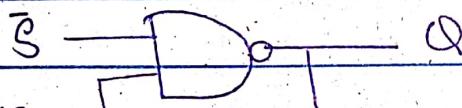
Active
High input



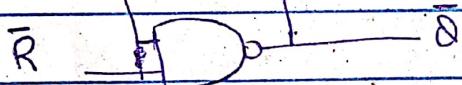
OR



OR



Active
Low input



When \bar{Q} is High Q is low and when Q is High \bar{Q} is low.

Default

S	R	Q	Q	\bar{Q}
0	0	0	1	1
		1	1	1
0	1	0	1	0
		1	1	0
1	0	0	0	1
		1	0	1
1	1	0	0	1
		1	1	0

Diagram showing the state transitions:

- Set: $\bar{S} = 1, \bar{R} = 0$ leads to $Q=1, \bar{Q}=0$. A switch labeled "Set" connects \bar{S} to the Set input of a D flip-flop.
- Reset: $\bar{S} = 0, \bar{R} = 1$ leads to $Q=0, \bar{Q}=1$. A switch labeled "reset" connects \bar{R} to the Reset input of a D flip-flop.
- Constant: $\bar{S} = 1, \bar{R} = 1$ leads to $Q=1, \bar{Q}=1$.
- Retain: $\bar{S} = 0, \bar{R} = 0$ leads to $Q=1, \bar{Q}=0$.
- Lost State: $\bar{S} = 0, \bar{R} = 0$ leads to $Q=0, \bar{Q}=1$.

When $Q=1$ State is "set"

When $Q=0$ State is "reset"

$\bar{S} 1 0 1 1 0 \quad 1 1$

$\bar{R} 1 1 0 1 0 \quad 0$

$Q \quad 1 \quad 1 \quad 0 \quad 1 \quad 1 \quad 0$

S	R	Q	\bar{Q}
0	0	1	1
0	1	1	0
1	0	0	1
1	1	1	0

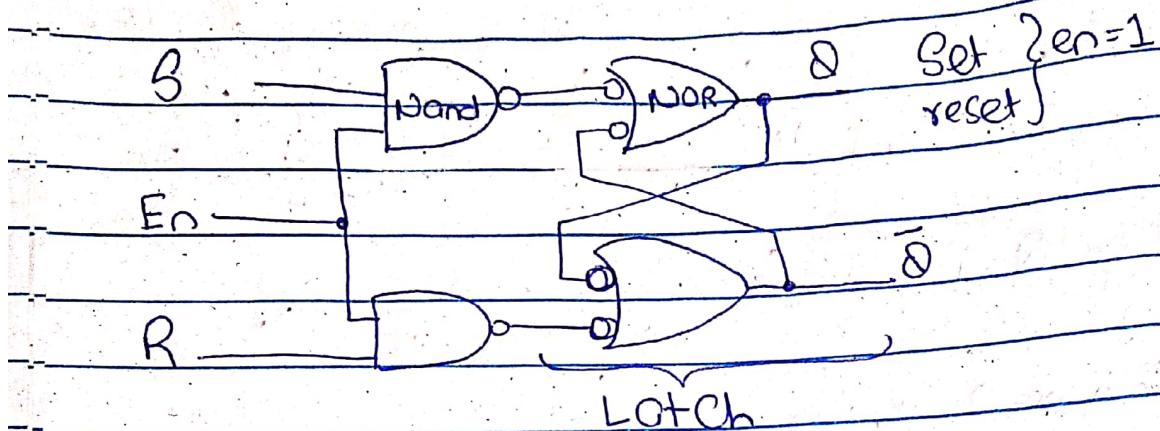
Summary of State Transitions:

- $0, 0 \rightarrow 1, 1$ (Normal)
- $0, 1 \rightarrow 1, 0$ (Reset)
- $1, 0 \rightarrow 0, 1$ (Set)
- $1, 1 \rightarrow 1, 1$ (Constant)

Types Of Latch

See "The latch as a Contact Bounce Eliminator" from lec 25.

The Gated S-R Latch:-



$E_n \rightarrow$ Activates the latch function ($e_n = 1$)

$L = 1$ activates

Since $S=0 \longrightarrow$ Constant

$$R=0 \quad \uparrow$$

$$S = 1$$

$$\bar{R} = 1$$

$$S \quad | \quad 1 \quad 0 \quad 1 \quad 0$$

$$1$$

$$R \quad | \quad 0 \quad 1 \quad 0 \quad 0$$

$$1$$

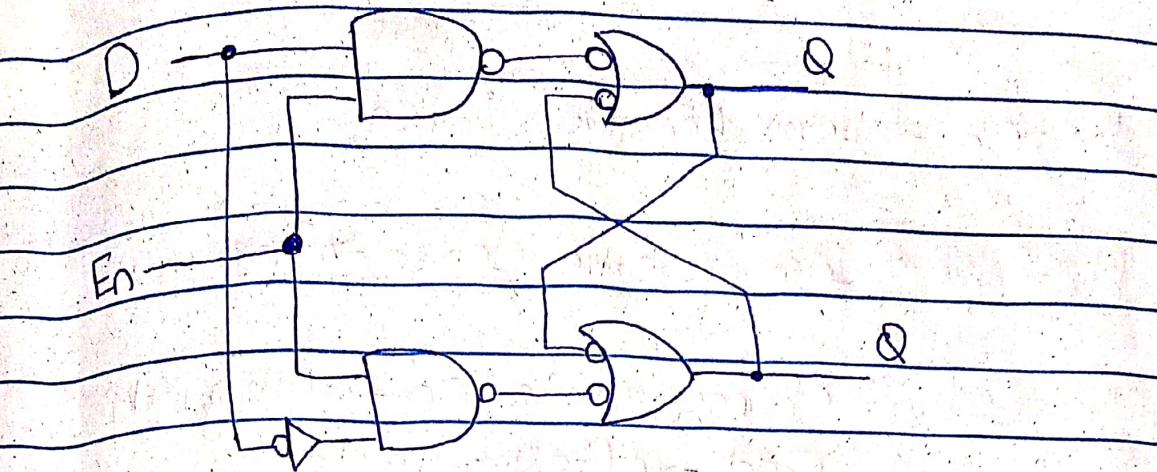
$$E_n \quad | \quad 0 \quad 1 \quad 0 \quad 0$$

$$Q$$

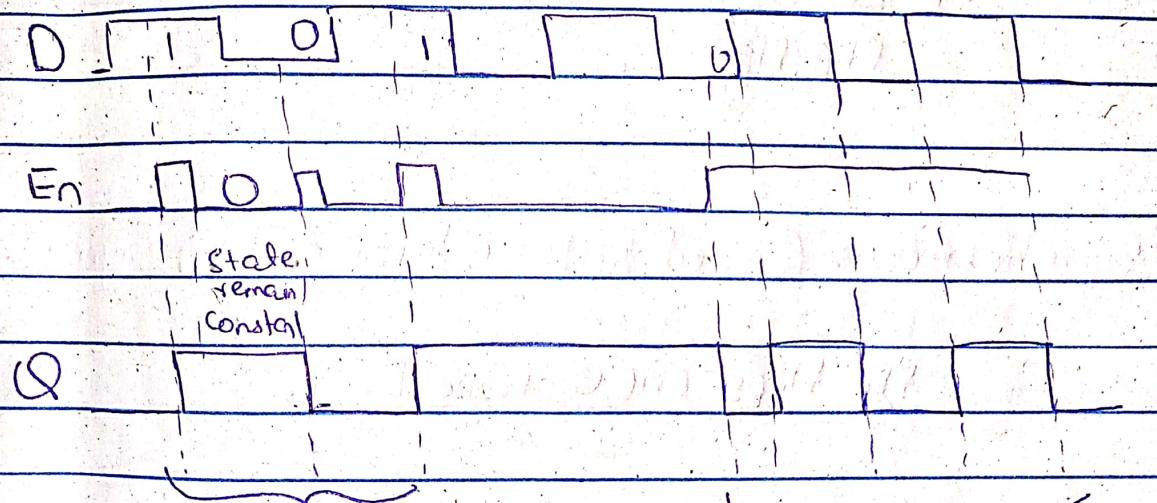
will continue its state as $e_n = 0$

Changes state at $e_n = 1$

The Gated D-Latch :-



$D \rightarrow S$ $D = 1$ Set $S = 1$
 $\bar{D} \rightarrow R$ $D = 0$ Reset $S = 0$



Switches according to $En + D$ Q Follow D

When $en \neq 0$ State changes and
when $en = 0$ State remains constant.

Flip-Flops

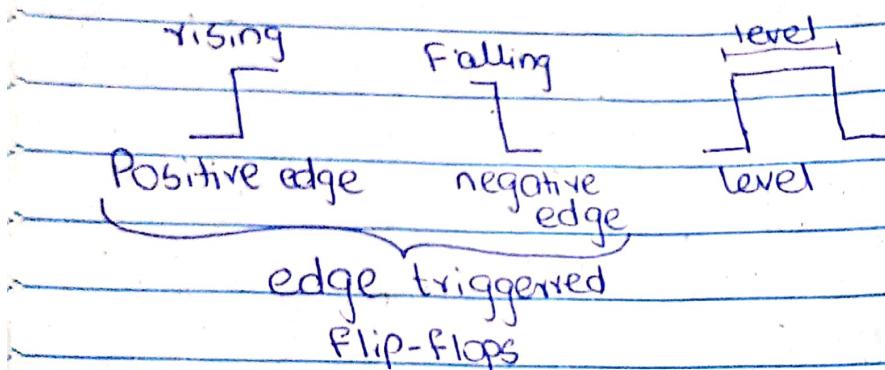
Latches is a bistable device that has two states Set and Reset.

Latch → Level Sensitive device

Flip-Flops → Edge Sensitive device → Synchronous



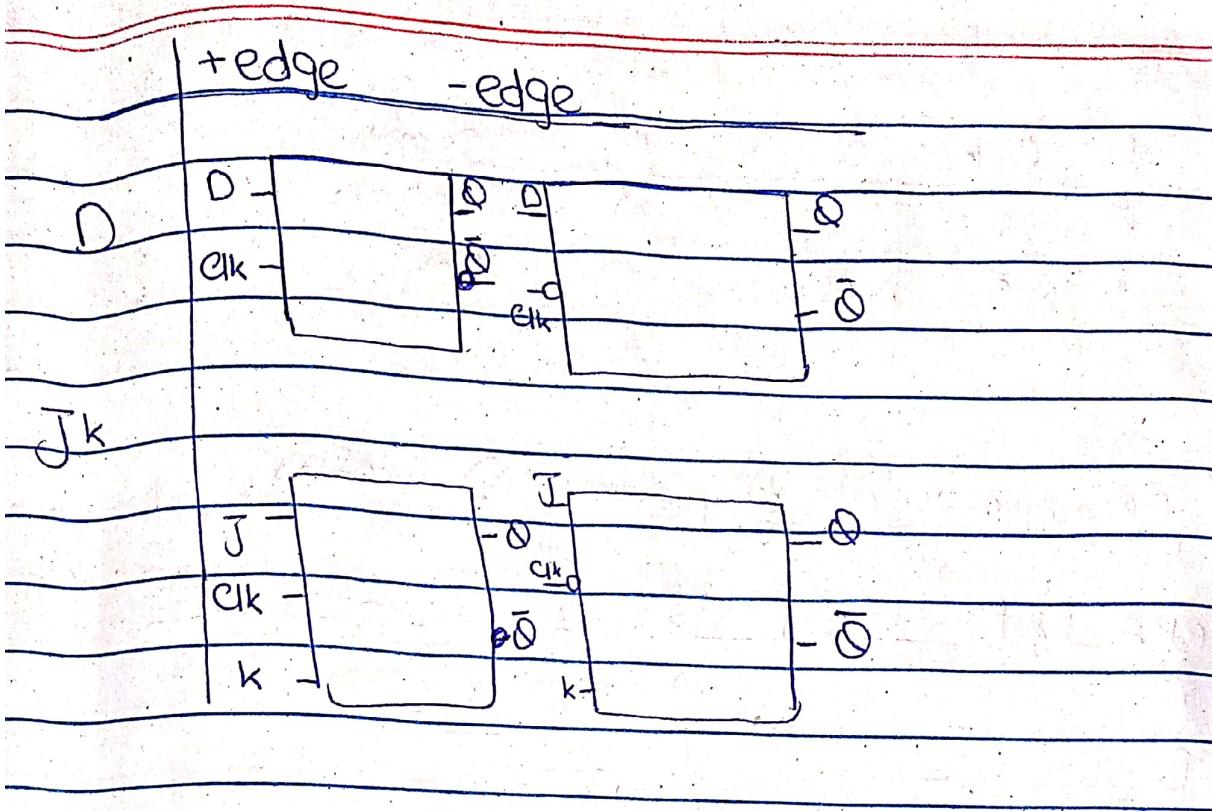
Changes State On +ve (rising) edge
And -ve (falling) edge.



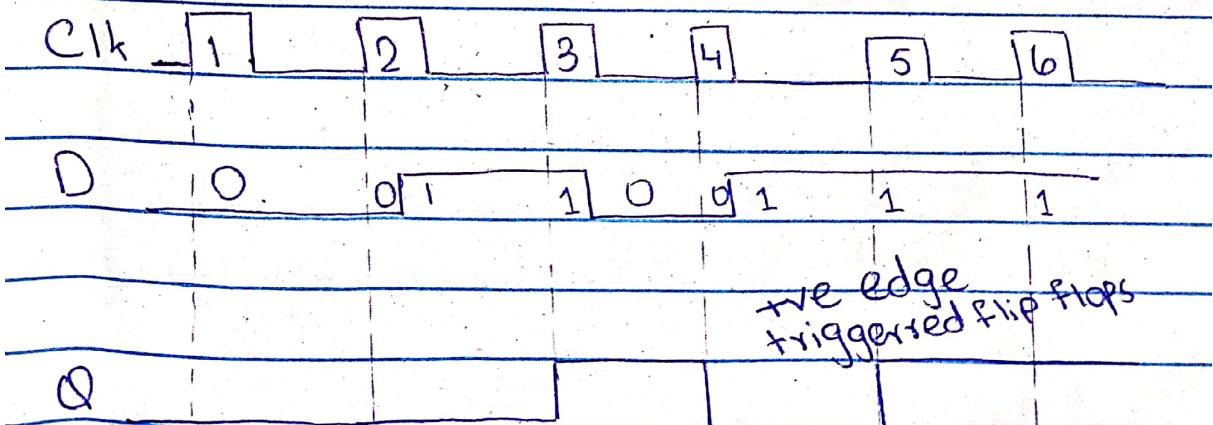
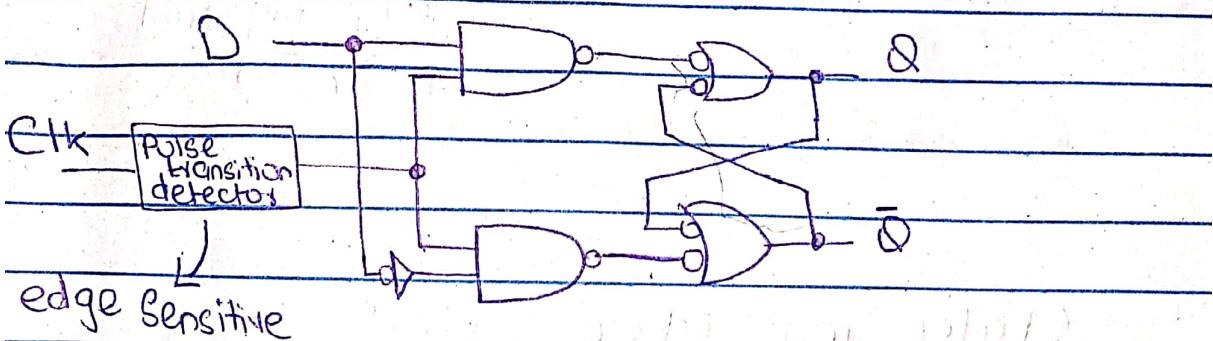
Synchronous → Synced with edge of Clock Signal

flip-flops are controlled by clocks

Clock is like enable key

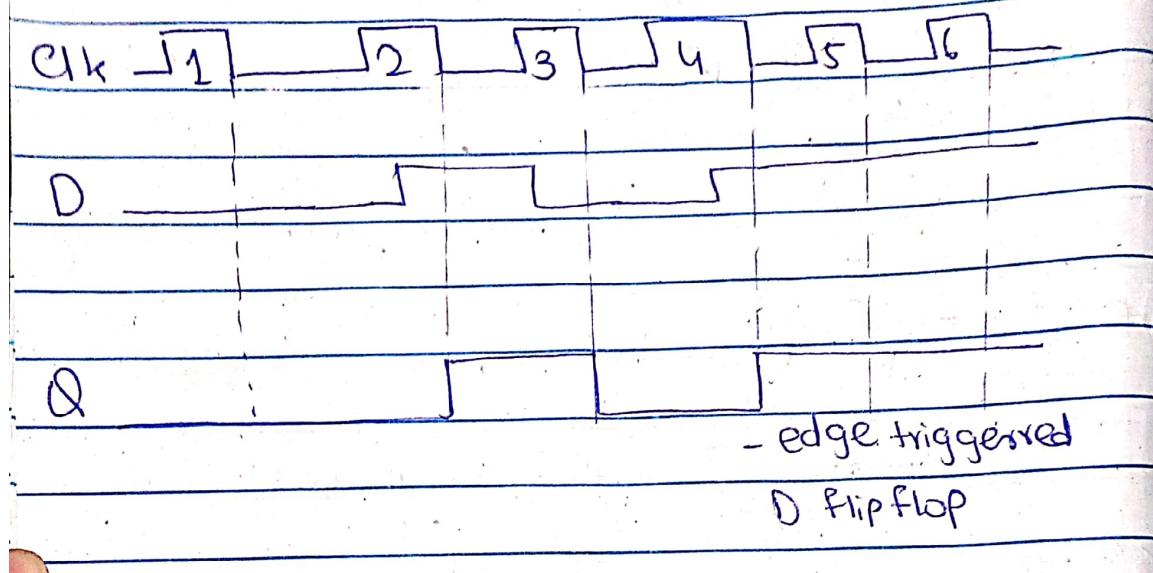


The D Flip Flop:-



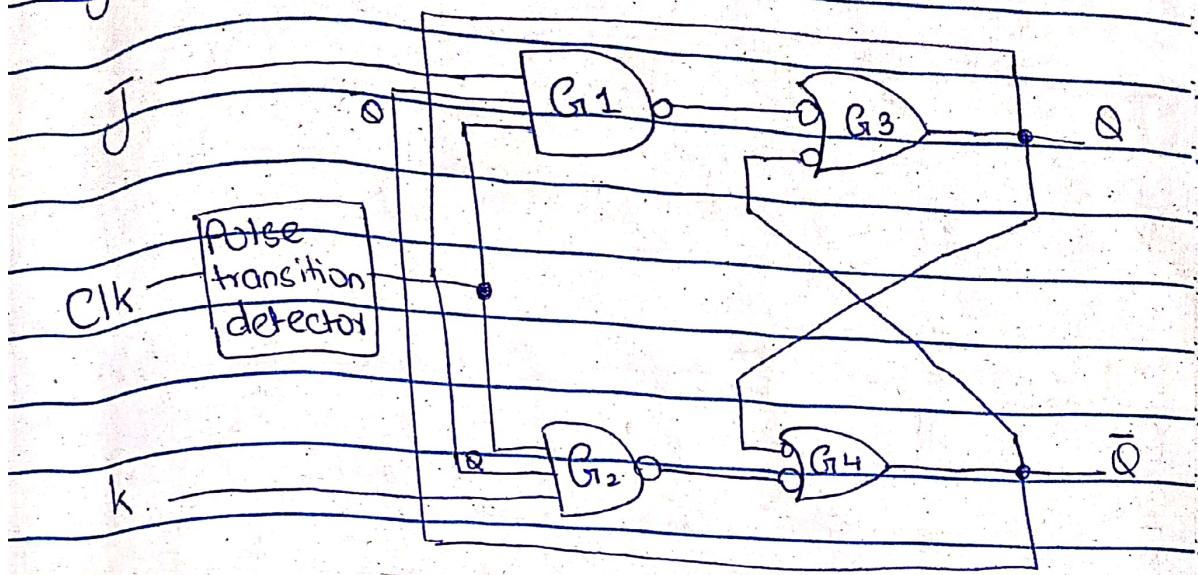
D	CLK	Q	\bar{Q}	Comment
0	↑	0	1	Reset
1	↑	1	0	Set

negative edge triggered D-Flipflop.



States will Change At
Next Clock Trigger.

J-K Flip-Flops:-

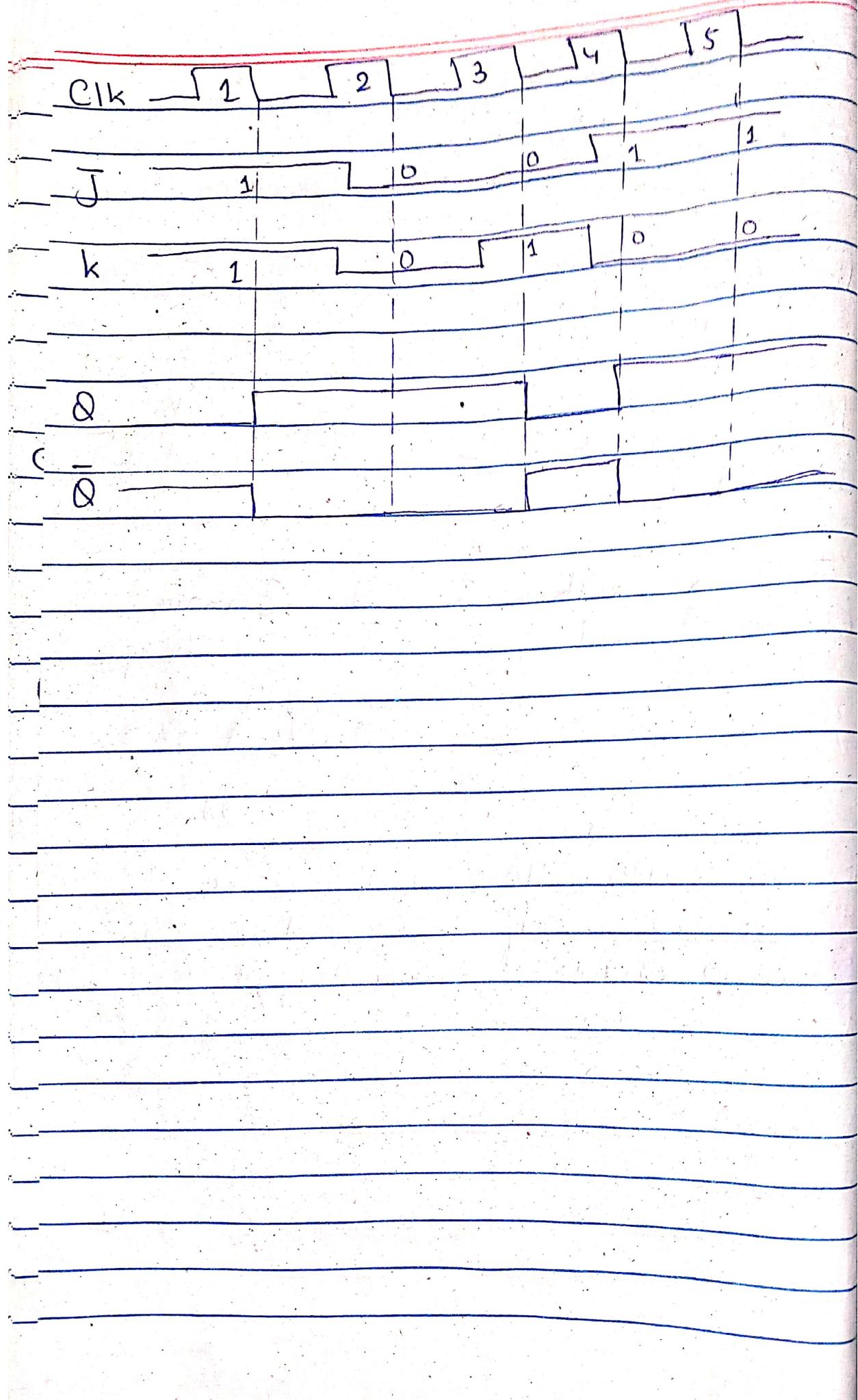


J	K	Clk	Q	\bar{Q}	Comments
0	0	↑	Q ₀	\bar{Q}_0	No change
0	1	↑	0	1	Reset
1	0	↑	1	0	Set
1	1	↑	\bar{Q}_0	Q ₀	Toggle

Toggle Switches the previous state

like previously $J=0$ and $K=1$ So

$Q=0$ and $\bar{Q}=1$, after toggle $Q=1$ and $\bar{Q}=0$.



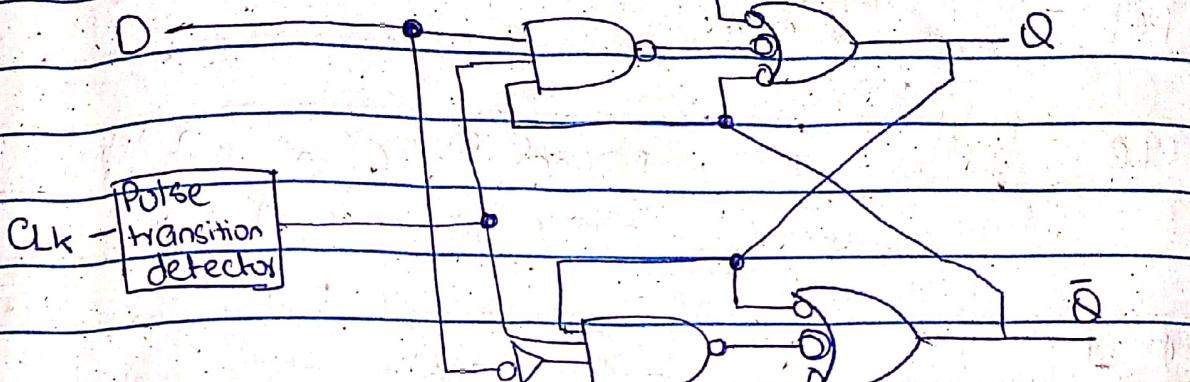
Asynchronous Inputs '8' Flip-Flop Characteristics

Preset \rightarrow Set

An active preset input makes the Q output High (Set)

CLR \rightarrow Reset

PRE (Present)

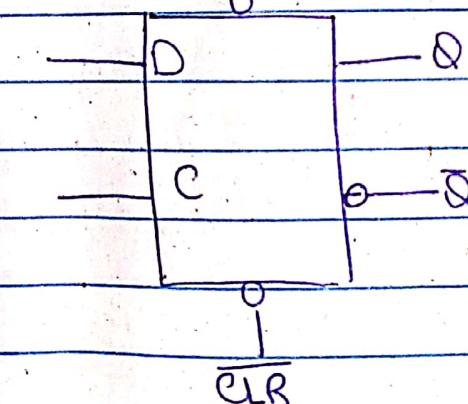


CLK - Pulse transition detector

CLR (clear)

PRE

An active clear input makes the Q output Low (reset)



It will be active at Q states

Clk | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9

D | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0

PRE | 0 Active Present |

CLR | normal D latch | 0 Active clear

+ve edge triggered

Q | 0 | 1 | 0 | 1 |

$Q=1$ as present
is active

Normal D latch

as both preset

and clear are 0

Q = 0 as active

clear

clear

Q = 0 as active

clear



Propagation Delay Times:-

A propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur. Four categories of propagation delay times are important in the operation of a flip-flop.

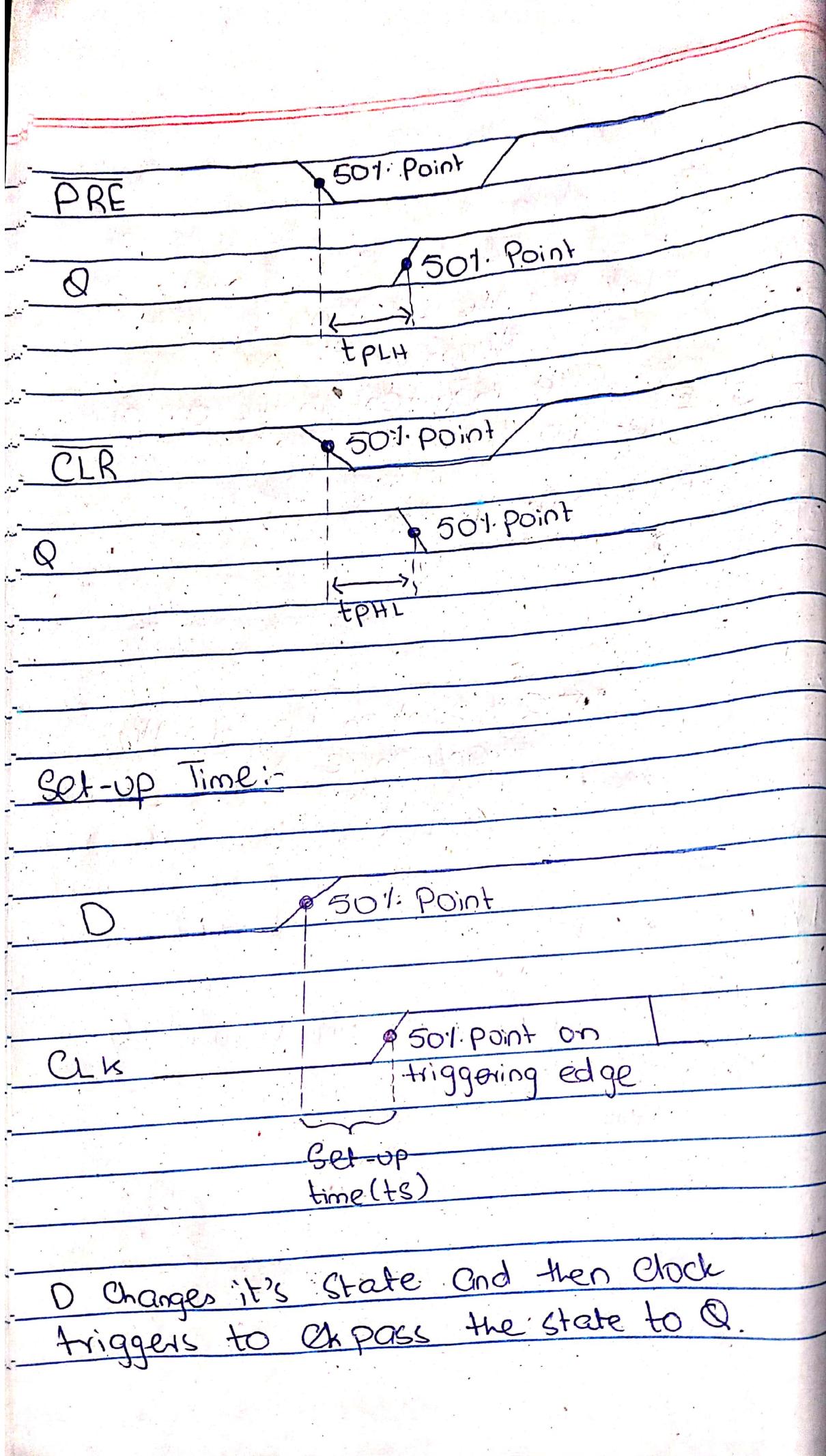
50% point on triggering edge



Q ↗ 50% point on Low-to-High
 ↔ transition of Q
 t_{PLH}

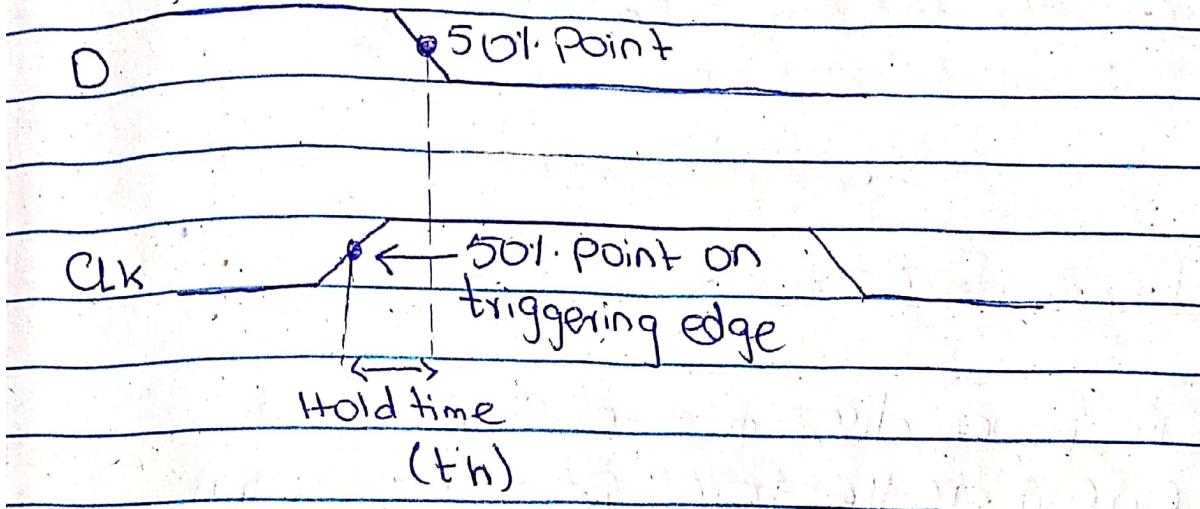
CLK ↗ 50% point

Q ↗ 50% point on High-to-Low
 ↔ transition of Q
 t_{PHL}



Hold Time:-

When clock holds some time to allow D to change its state, and then passes it to Q.



Maximum Clock Frequency:-

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop would be unable to respond reliably. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

Pulse Widths:-

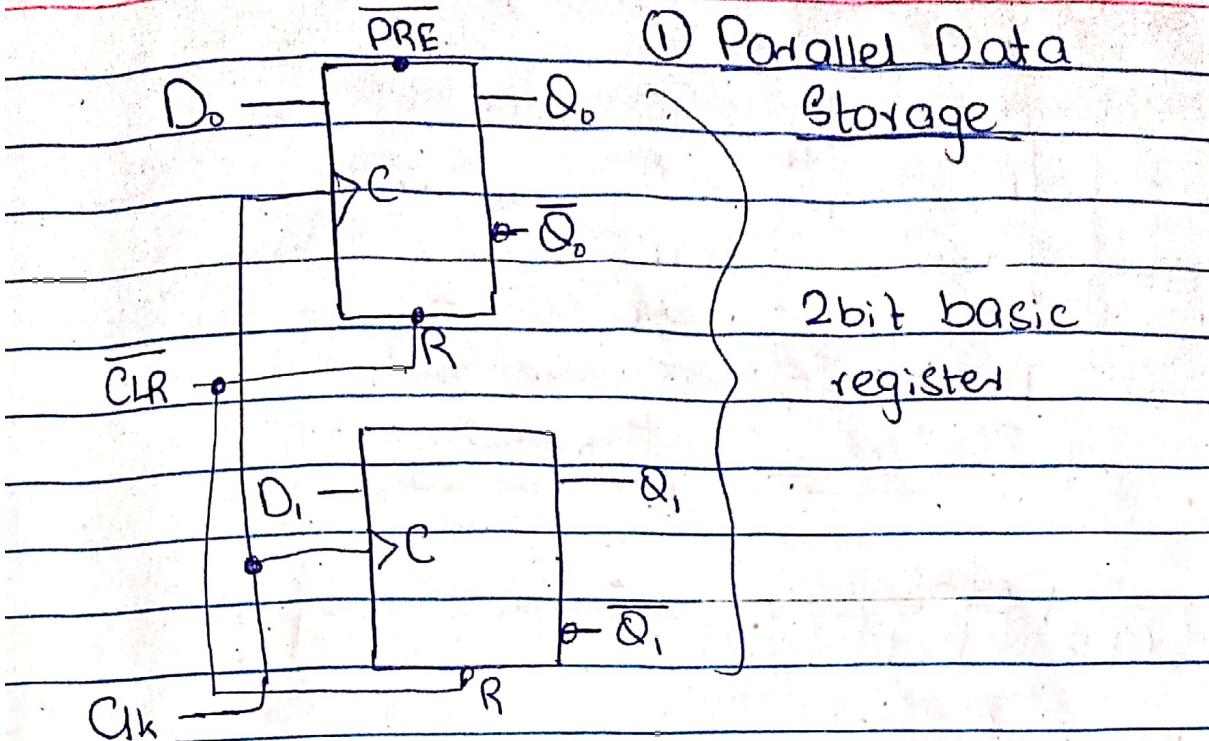
Minimum pulse widths (t_w) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum High time and its minimum Low time.

Power Dissipation:-

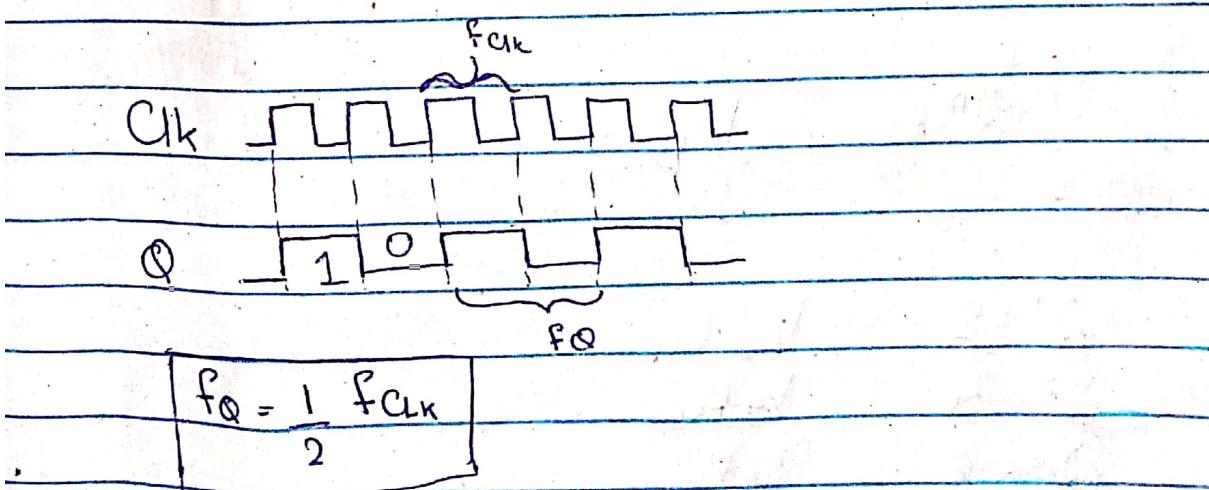
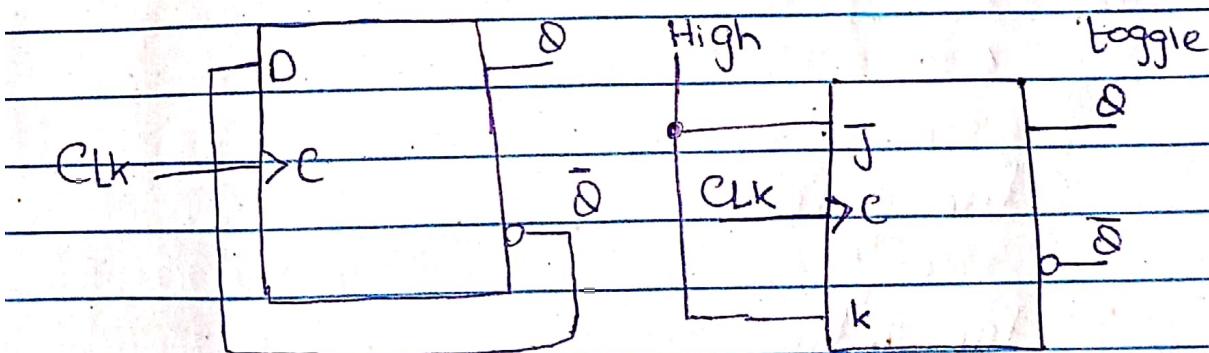
The power dissipation of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5V DC source and draws 5mA of current, the power dissipation is:

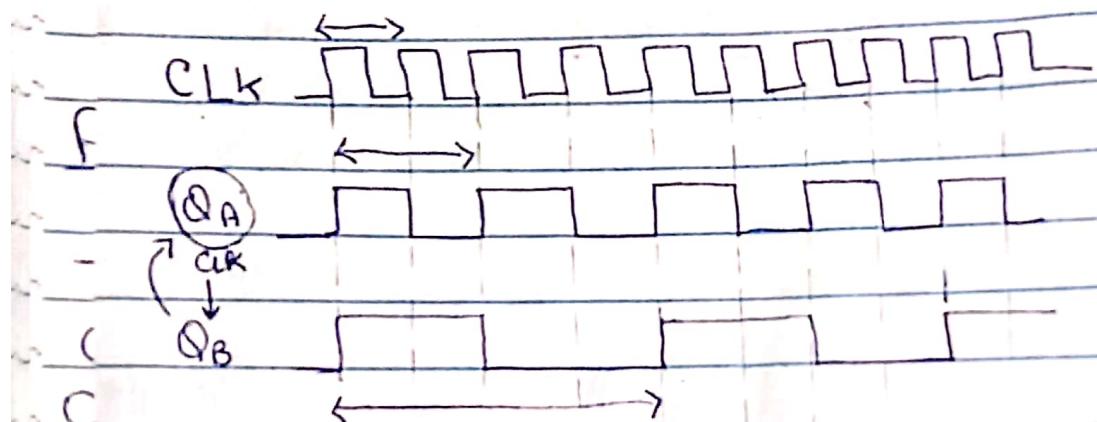
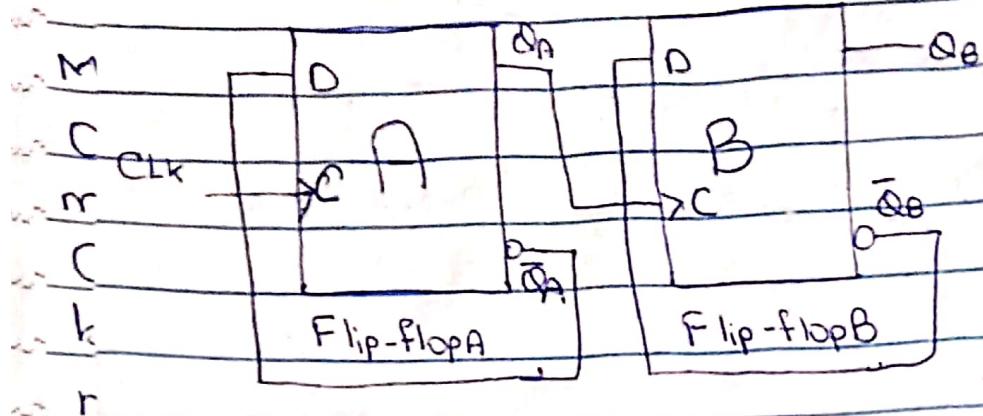
$$P = V_{CC} \times I_{CC} = 5V \times 5mA = 25mW$$

Flip-Flop Applications



② Frequency Divider





$$f_{\text{ff}_B} = \frac{1}{4} f_{\text{CLK}}$$

$$f_{\text{ff}_B} = \frac{1}{2} f_{\text{ff}_A}$$

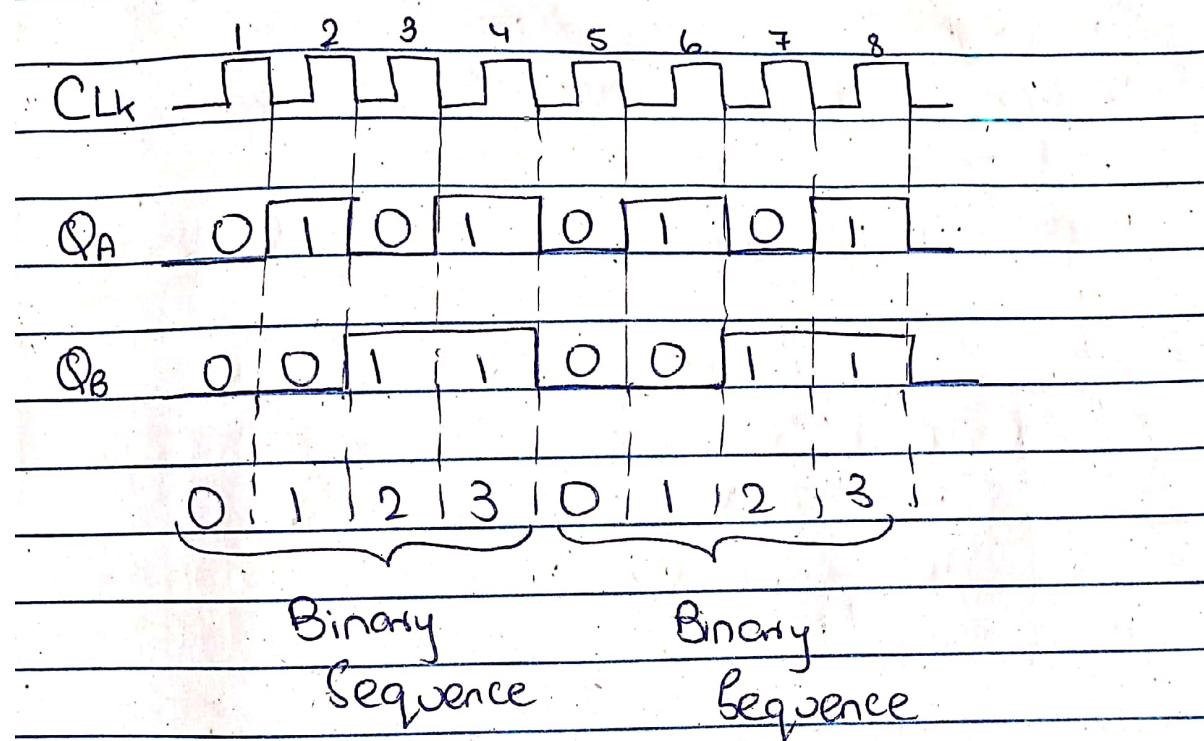
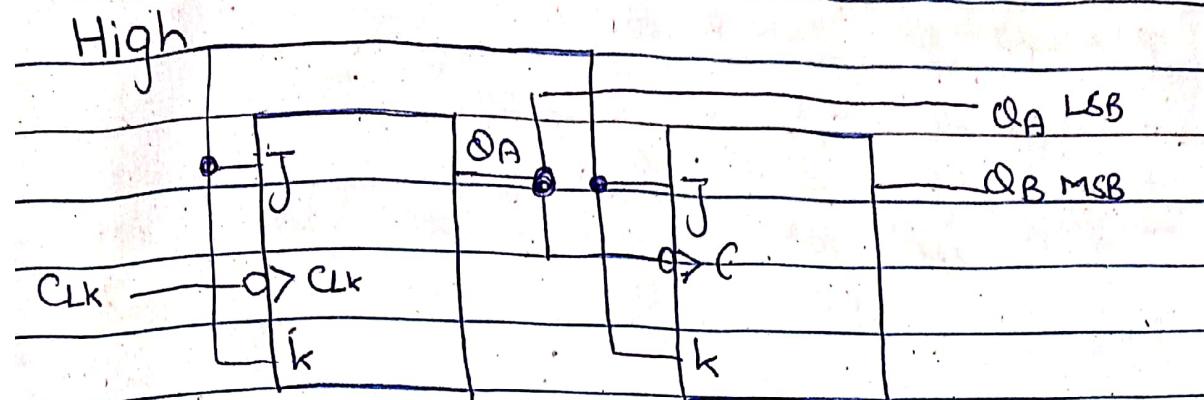
$$2^n = j \rightarrow \frac{1}{j} \text{ th}$$

$$2^1 = 2 \quad \frac{1}{2} f_{\text{CLK}}$$

$$2^2 = 4 \quad \frac{1}{4} f_{\text{CLK}}$$

$$2^3 = 8 \quad \frac{1}{8} f_{\text{CLK}}$$

③ Counter



Q_B Q_A if you just want to
0 0 - 0 (read 0, 1, 2 output)
0 1 - 1 (and not 3. So you
1 0 - 2 (have to use Asynchronous
1 1 - 3 (output and put 0 on
clear (i.e active) to
} avoid & output 3.