

# DIGITAL LOGIC DESIGN

## EE(109)

### CHAPTER -9

# Chapter No:9

# Counters

# Outlines

Asynchronous Counters

Synchronous Counters

Up/Down Synchronous Counters

Design of Synchronous Counters

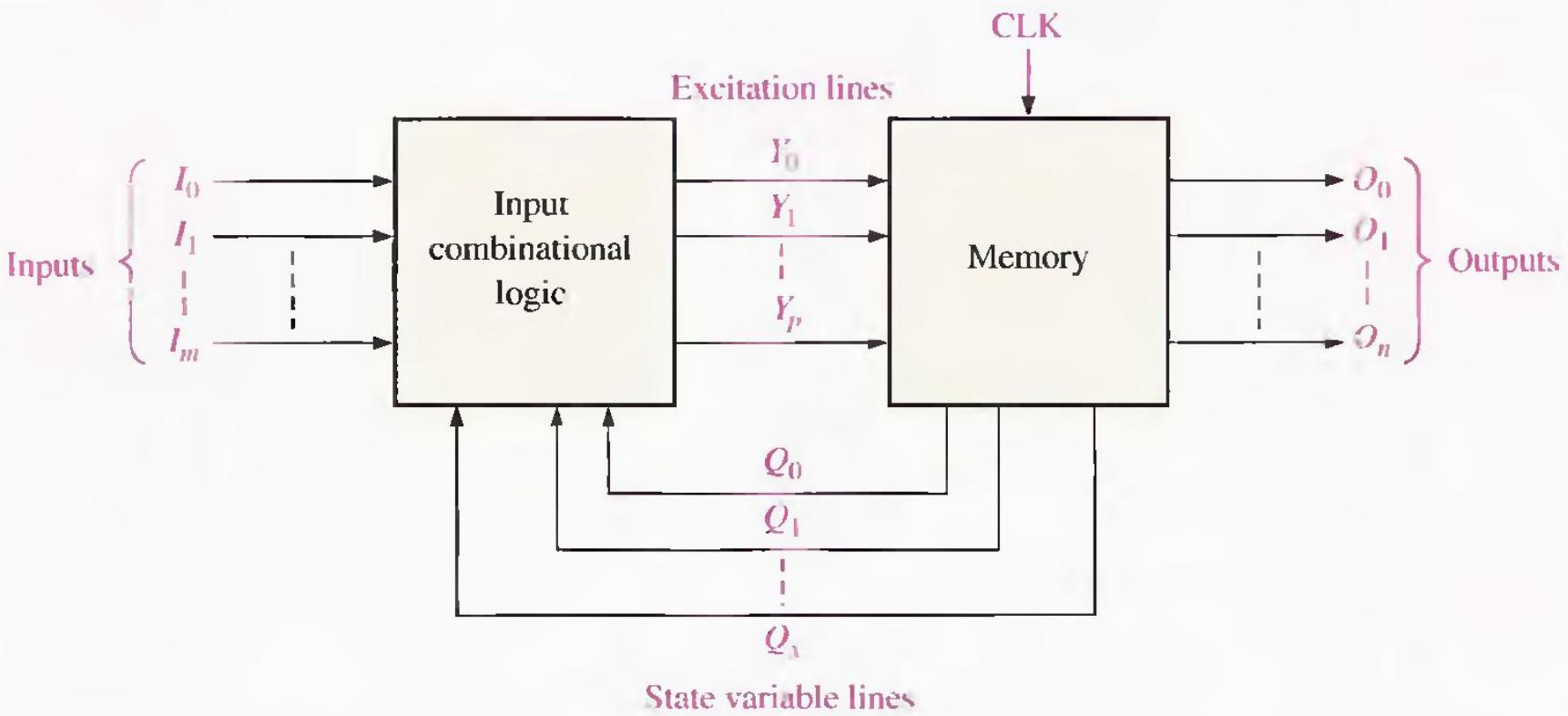
Cascaded Counters

Counter Decoding

Counter Applications

# DESIGN OF SYNCHRONOUS COUNTERS

## General Model of a Sequential Circuit

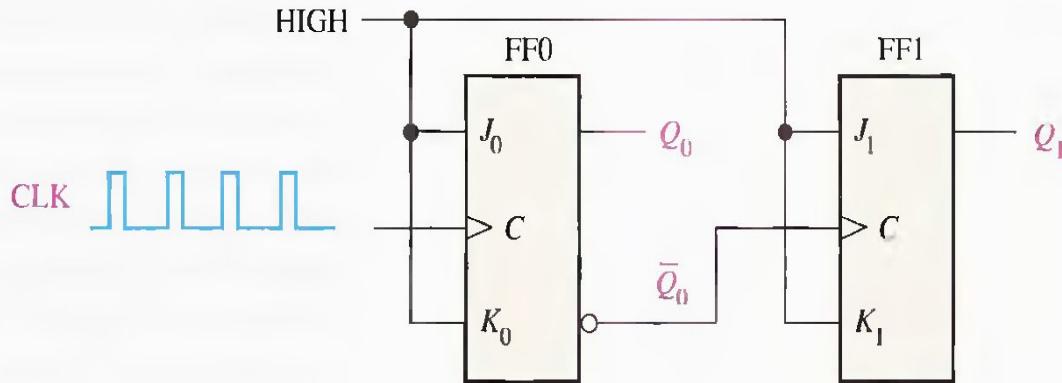


# ASYNCHRONOUS COUNTER OPERATION

The term **asynchronous** refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An **asynchronous counter** is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

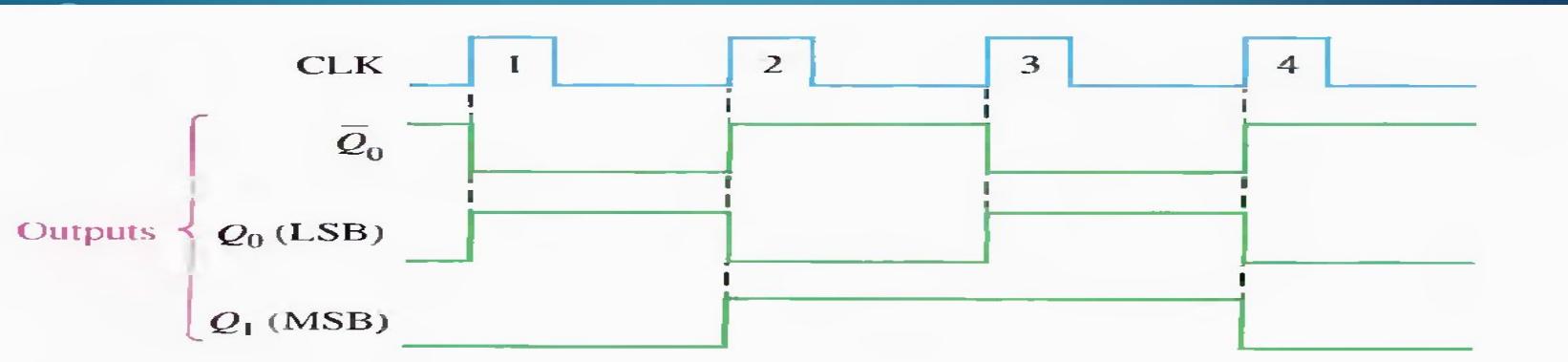
18

## A 2-Bit Asynchronous Binary Counter

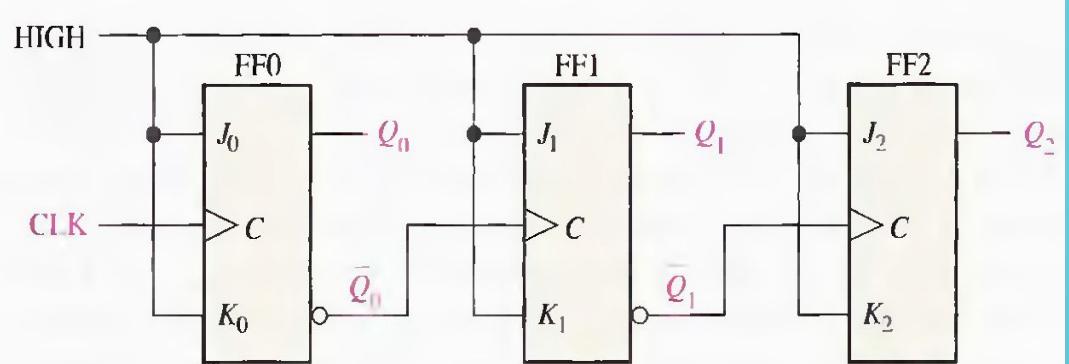


Asynchronous counters are also known as ripple counters.

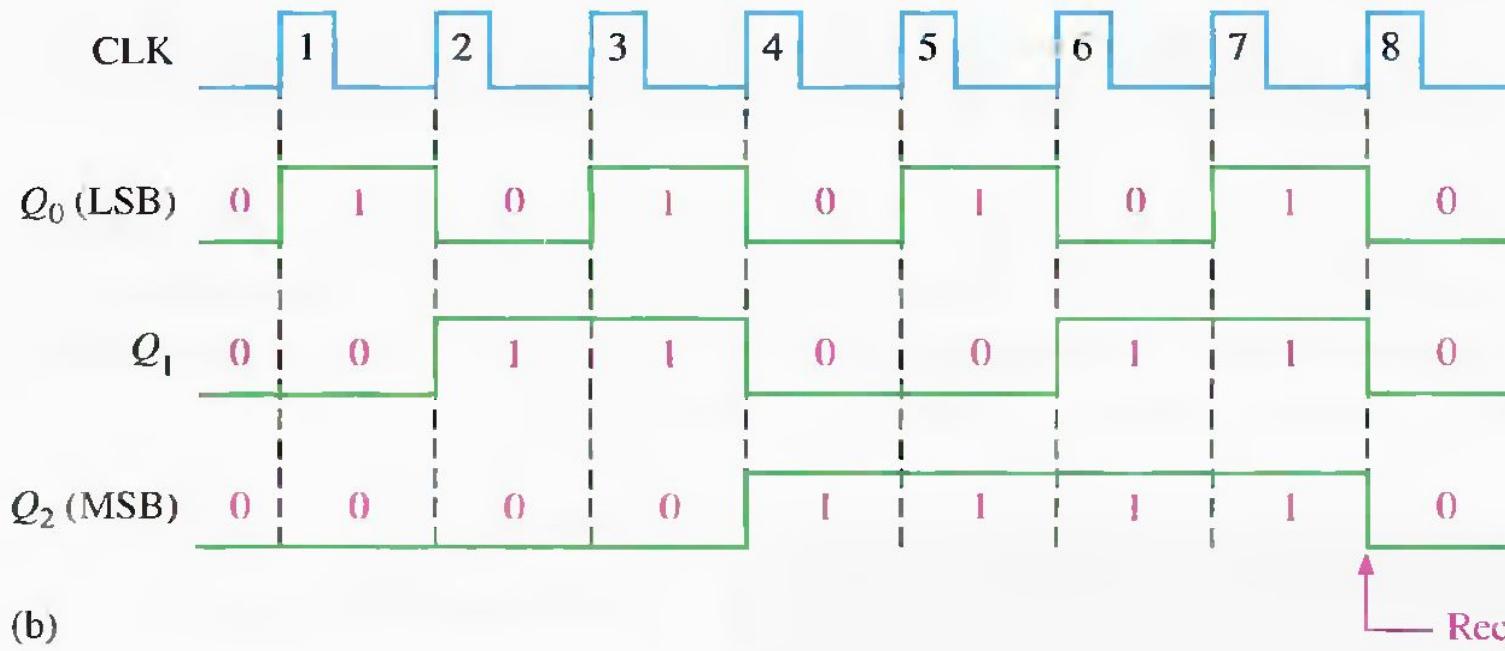
CLOCK PULSE	$Q_1$	$Q_0$
Initially	0	0
1	0	1
2	1	0
3	1	1
4 (recycles)	0	0



# A 3-Bit Asynchronous Binary Counter



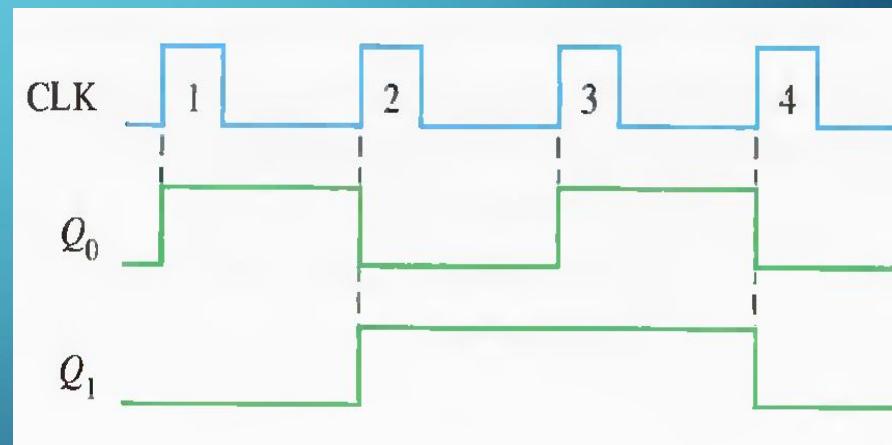
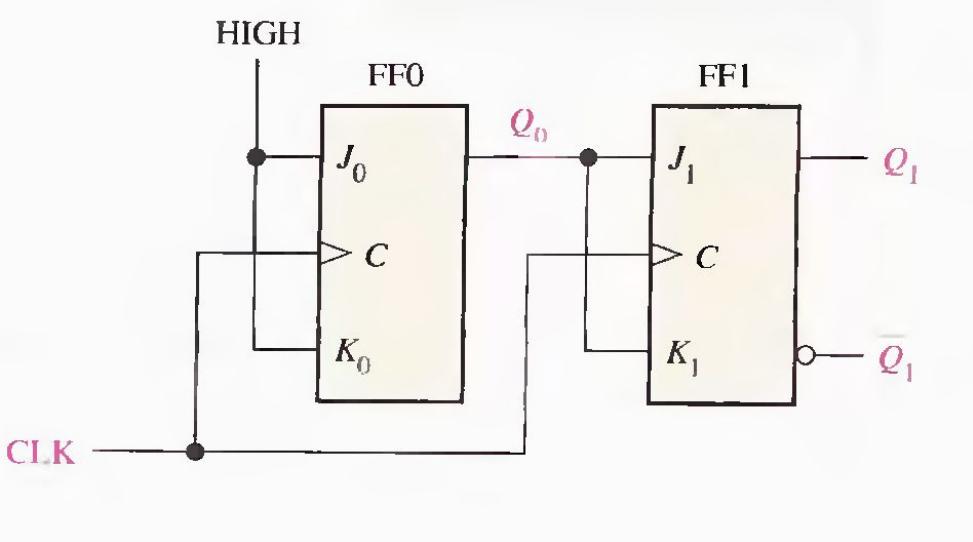
CLOCK PULSE	$Q_2$	$Q_1$	$Q_0$
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0



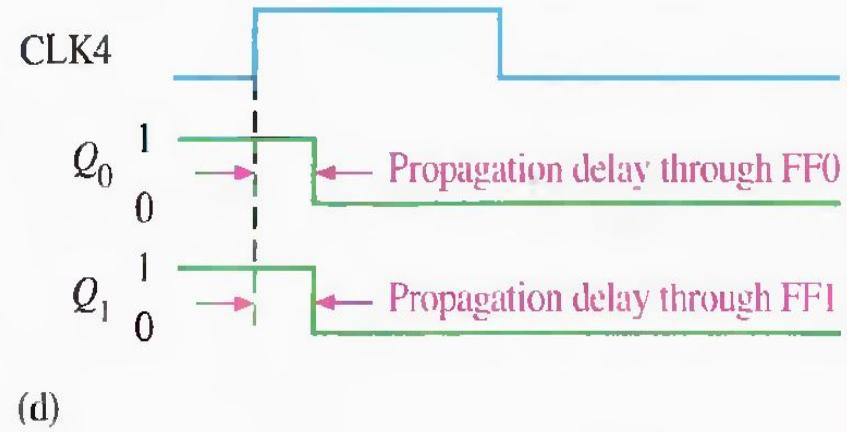
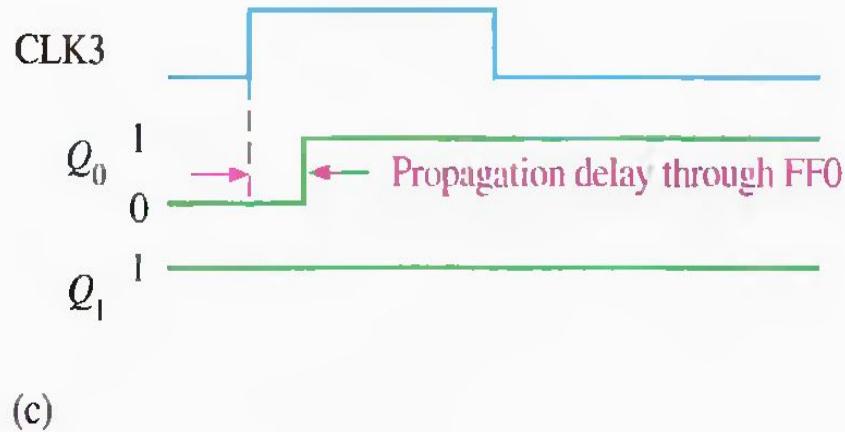
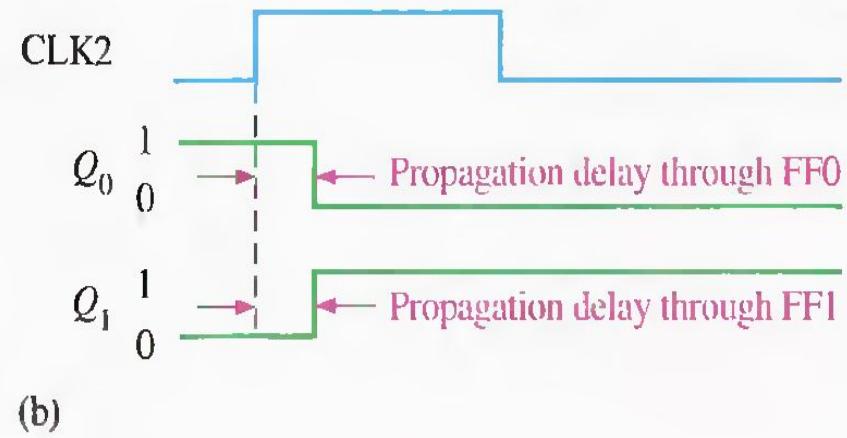
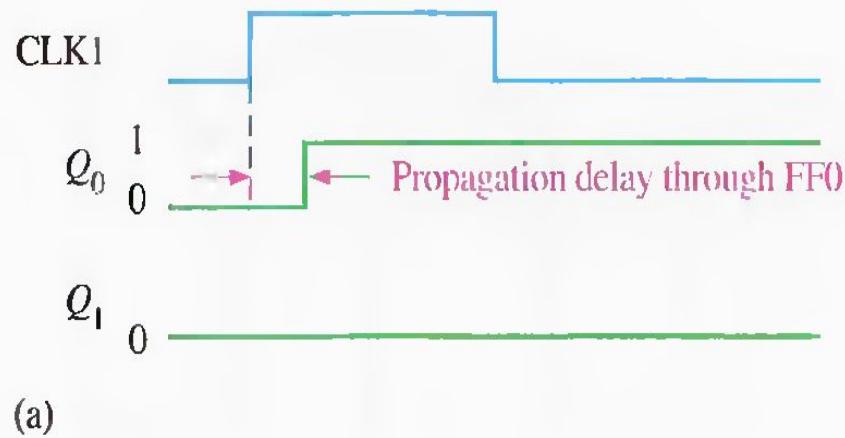
# SYNCHRONOUS COUNTER OPERATION

The term **synchronous** refers to events that have a fixed time relationship with each other. A **synchronous counter** is one in which all the flip-flops in the counter are clocked at the same time by a common clock pulse.

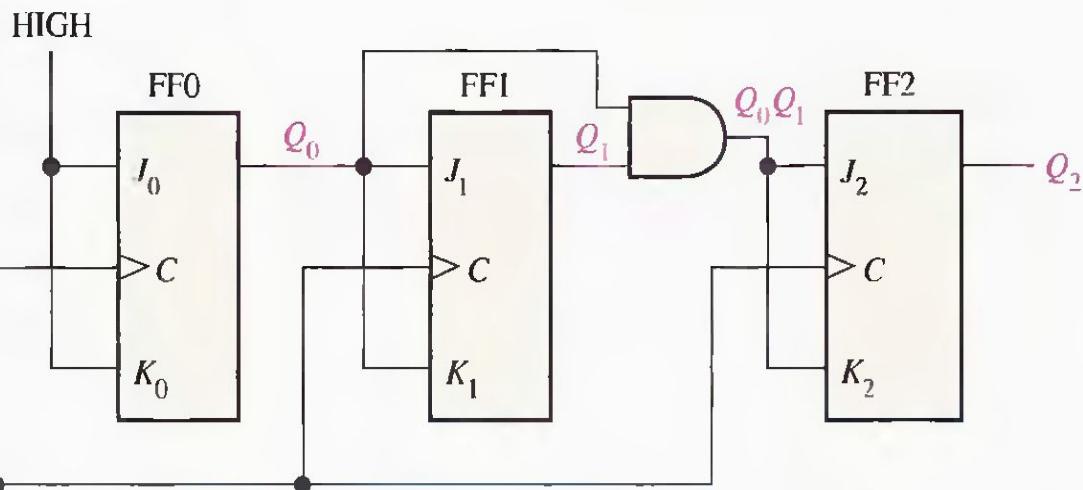
## A 2-Bit Synchronous Binary Counter



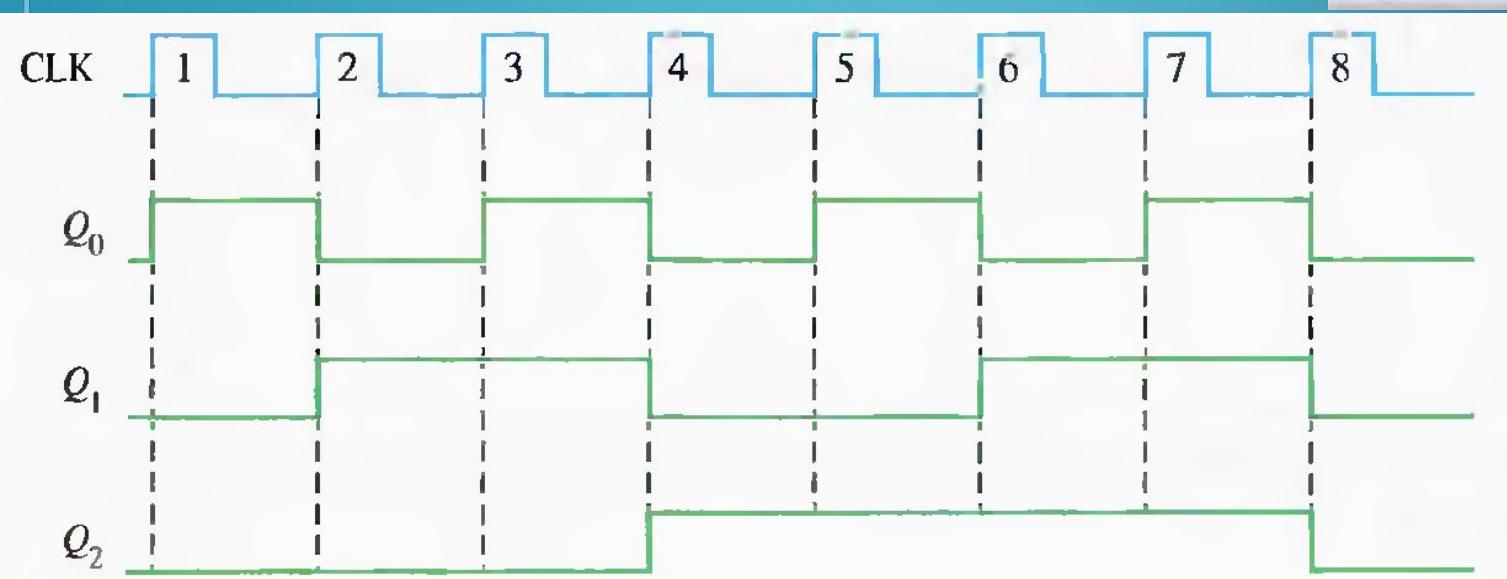
Timing details for the 2-bit synchronous counter operation (the propagation delays of both flip-flops are assumed to be equal).



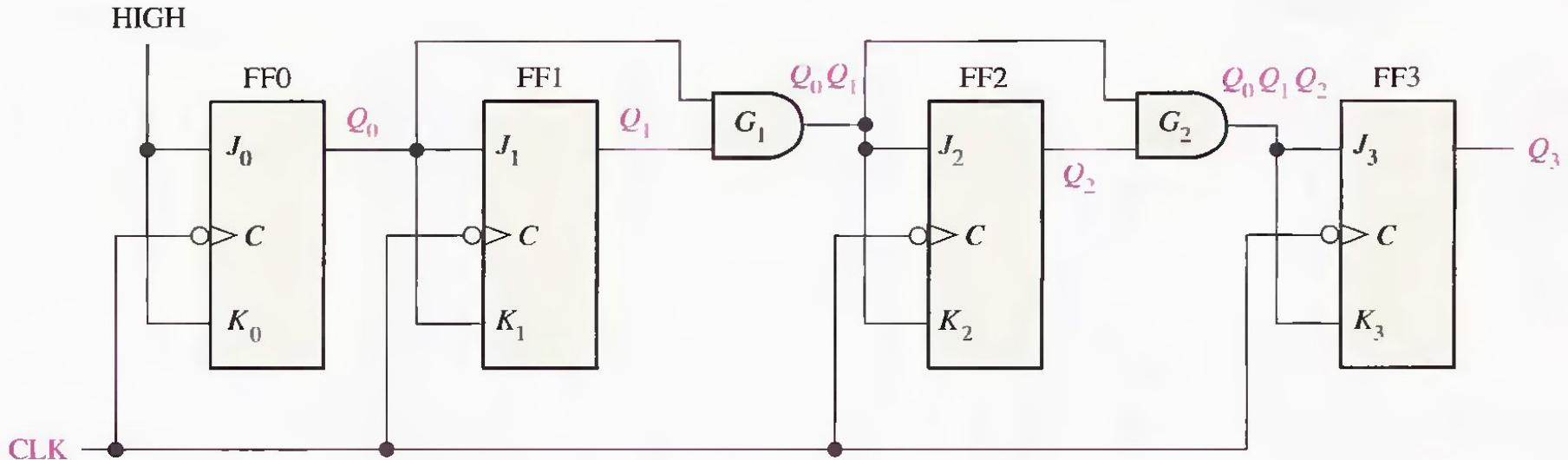
# A 3-Bit Synchronous Binary Counter



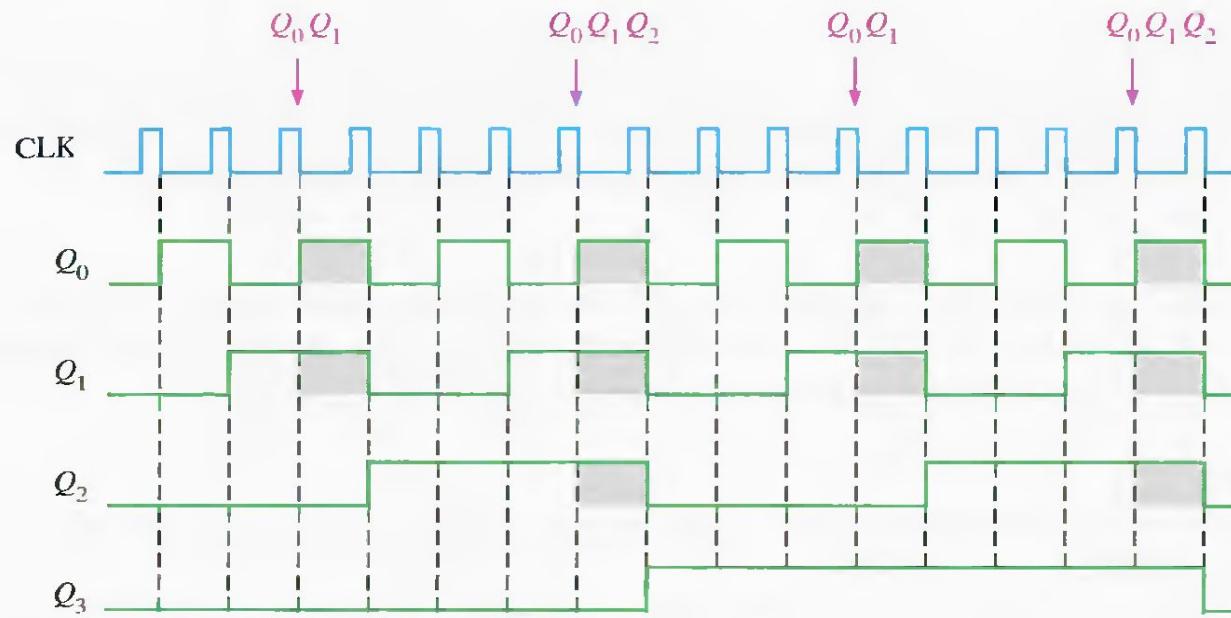
CLOCK PULSE	$Q_2$	$Q_1$	$\cdot Q_0$
Initially	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8 (recycles)	0	0	0



# A 4-Bit Synchronous Binary Counter

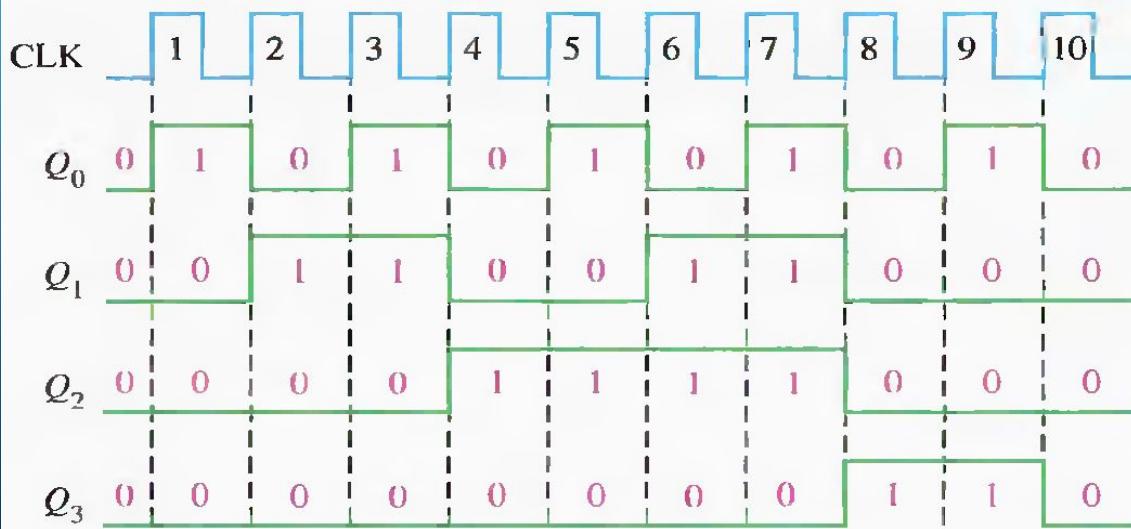
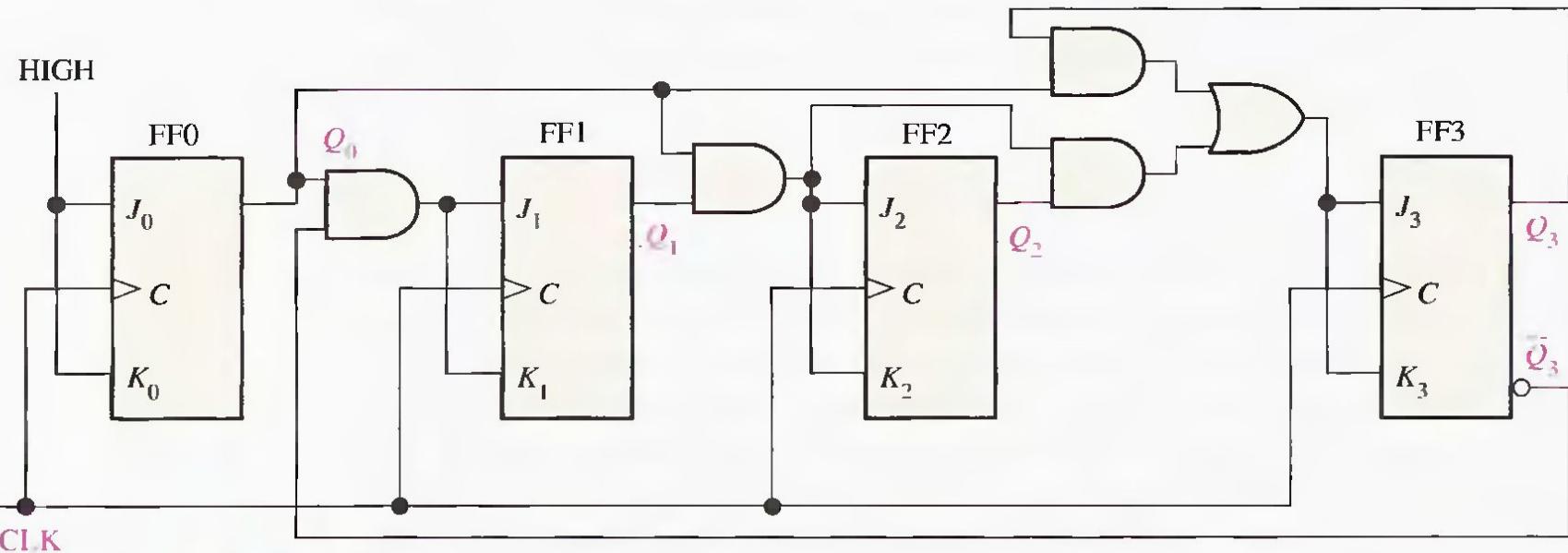


A 4-bit synchronous binary counter and timing diagram. Points where the AND gate outputs are HIGH are indicated by the shaded areas.



# A 4-Bit Synchronous Decade Counter

A synchronous BCD decade counter.



# States of a BCD decade counter.

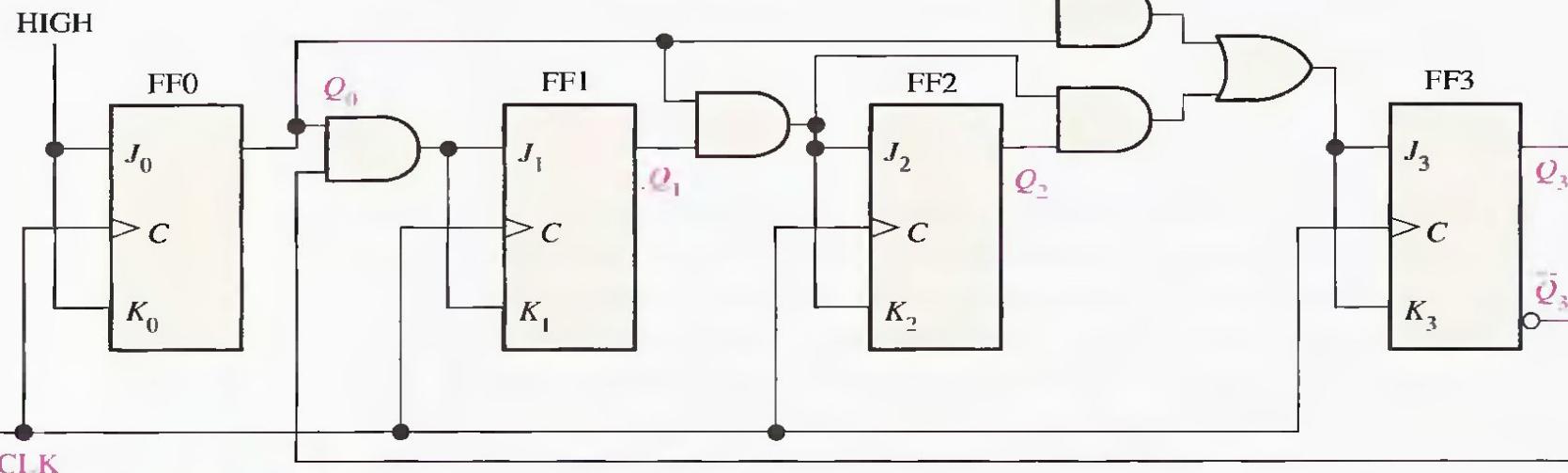
CLOCK PULSE	$Q_3$	$Q_2$	$Q_1$	$Q_0$
Initially	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10 (recycles)	0	0	0	0

$$J_0 = K_0 = 1$$

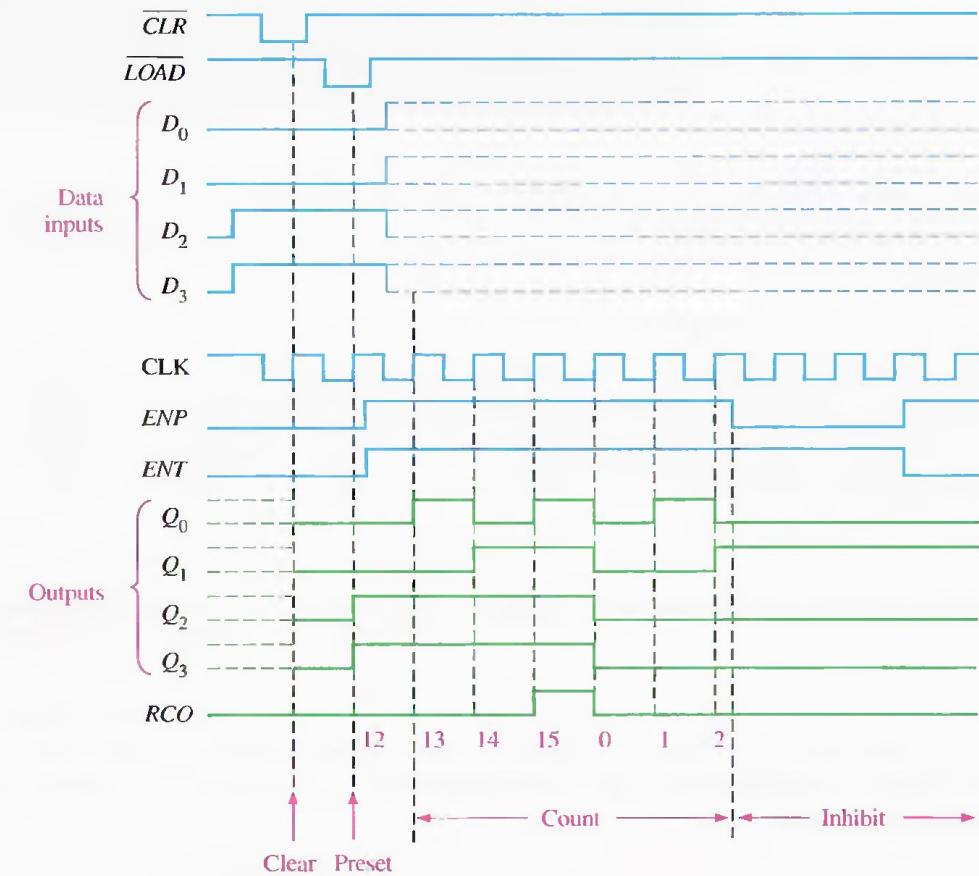
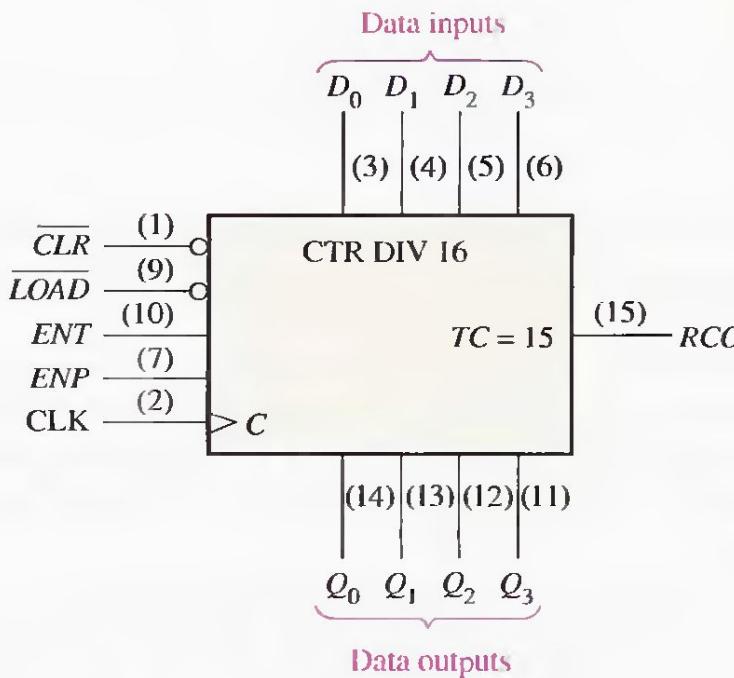
$$J_1 = K_1 = Q_0 \bar{Q}_3$$

$$J_2 = K_2 = Q_0 Q_1$$

$$J_3 = K_3 = Q_0 Q_1 Q_2 + Q_0 Q_3$$



# THE 74HC163 4-BIT SYNCHRONOUS BINARY COUNTER



$CLR \Rightarrow$  reset all flip flop

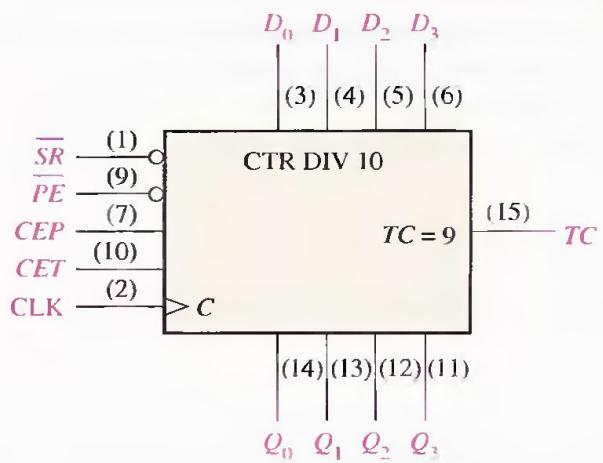
$LOAD \Rightarrow$  (Preset) At Low all sequence starts

$ENT$  &  $ENP$   $\Rightarrow$  Enable , both

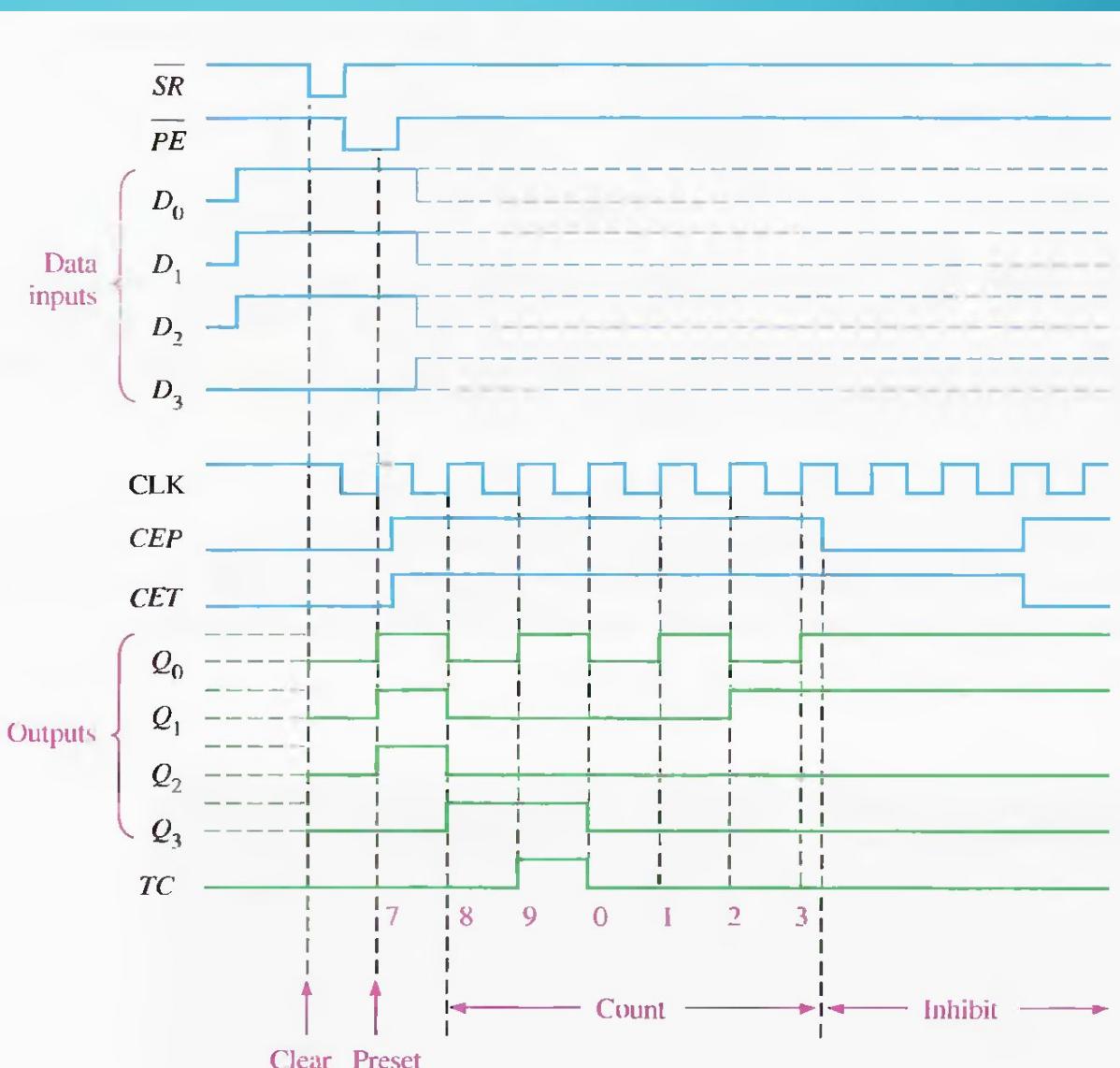
should be HIGH

$RCO \Rightarrow$  goes High when counter reaches a Terminal Count ( $TC=15$ )

# THE 74F162 SYNCHRONOUS BCD DECADE COUNTER



SR = CLR  
 PE = LOAD  
 CEP = ENP  
 CET = ENT



# UP/DOWN SYNCHRONOUS COUNTERS

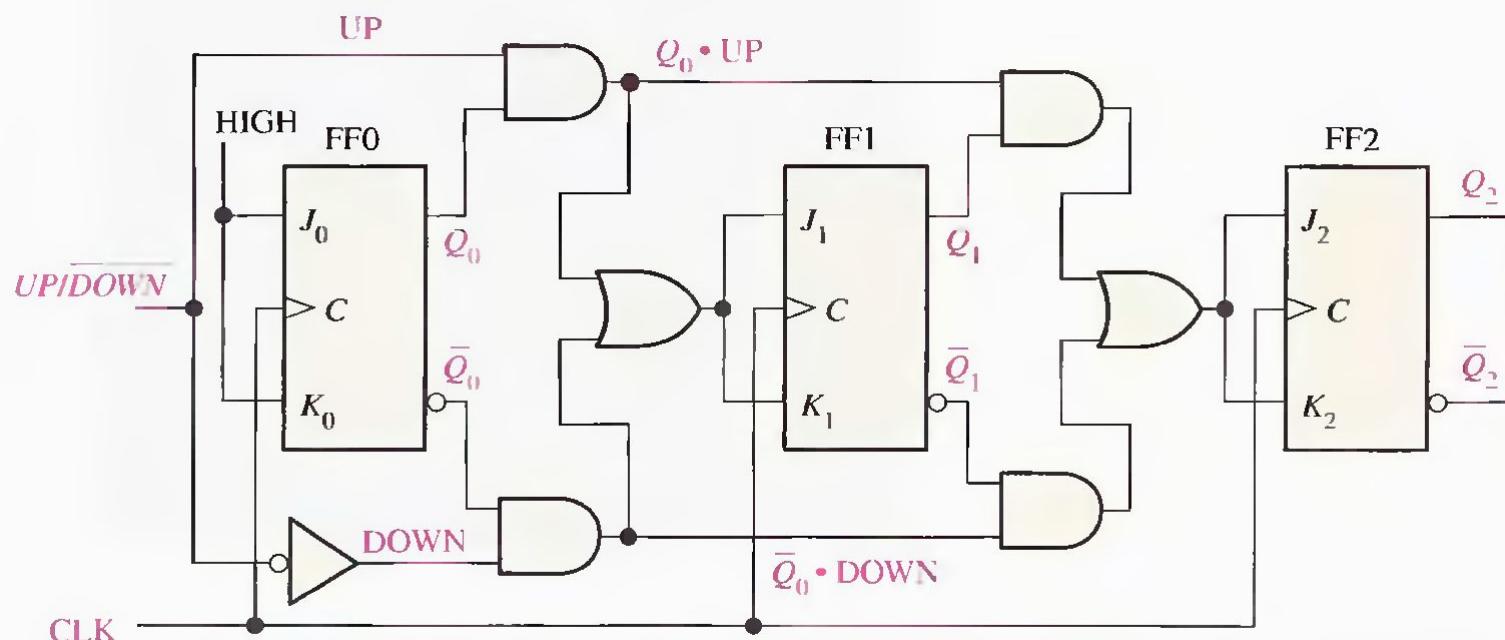
**UP**  
 $0, 1, 2, 3, 4, 5, 4, 3, 2, 3, 4, 5, 6, 7, 6, 5, \text{etc.}$   
**DOWN**

$$J_0 = K_0 = 1$$

$$J_1 = K_1 = (Q_0 \cdot \text{UP}) + (\bar{Q}_0 \cdot \text{DOWN})$$

$$J_2 = K_2 = (Q_0 \cdot Q_1 \cdot \text{UP}) + (\bar{Q}_0 \cdot \bar{Q}_1 \cdot \text{DOWN})$$

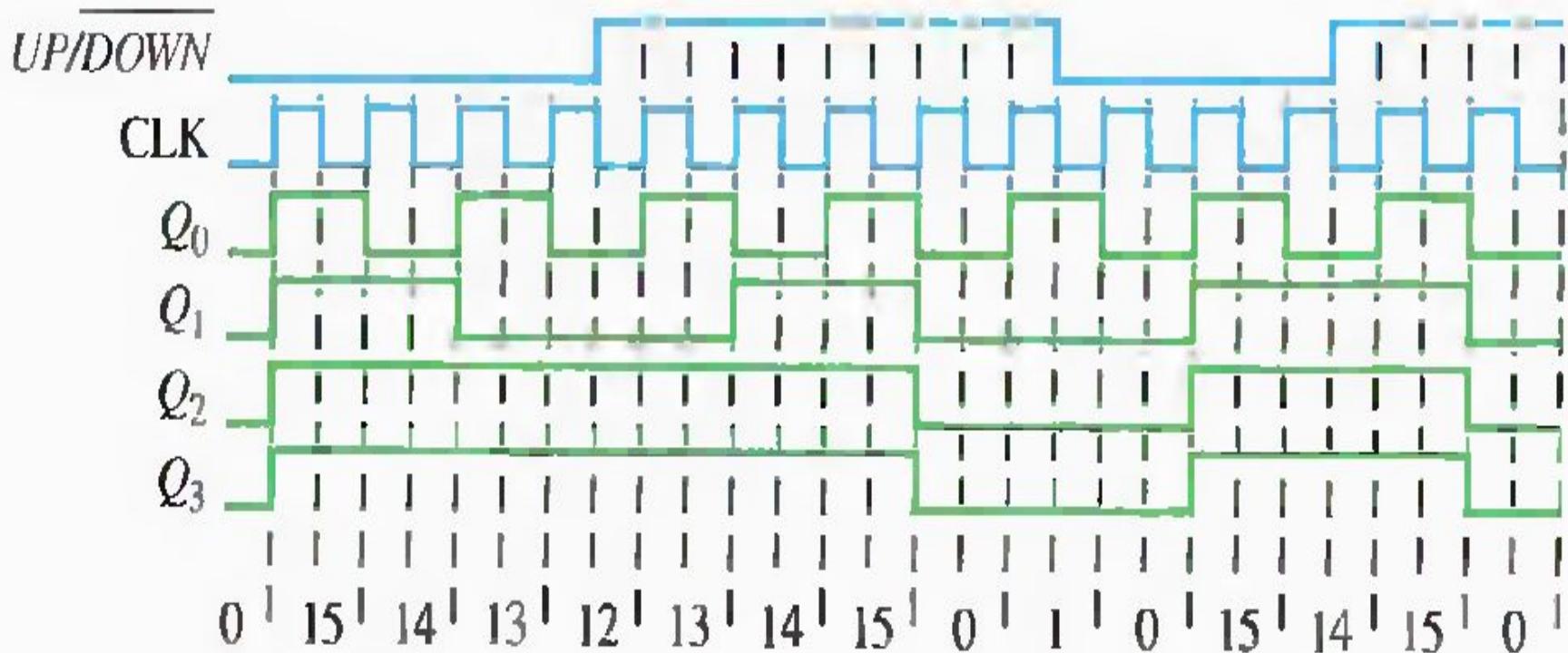
CLOCK PULSE	UP	$Q_2$	$Q_1$	$Q_0$	DOWN
0		0	0	0	
1		0	0	1	
2		0	1	0	
3		0	1	1	
4		1	0	0	
5		1	0	1	
6		1	1	0	
7		1	1	1	



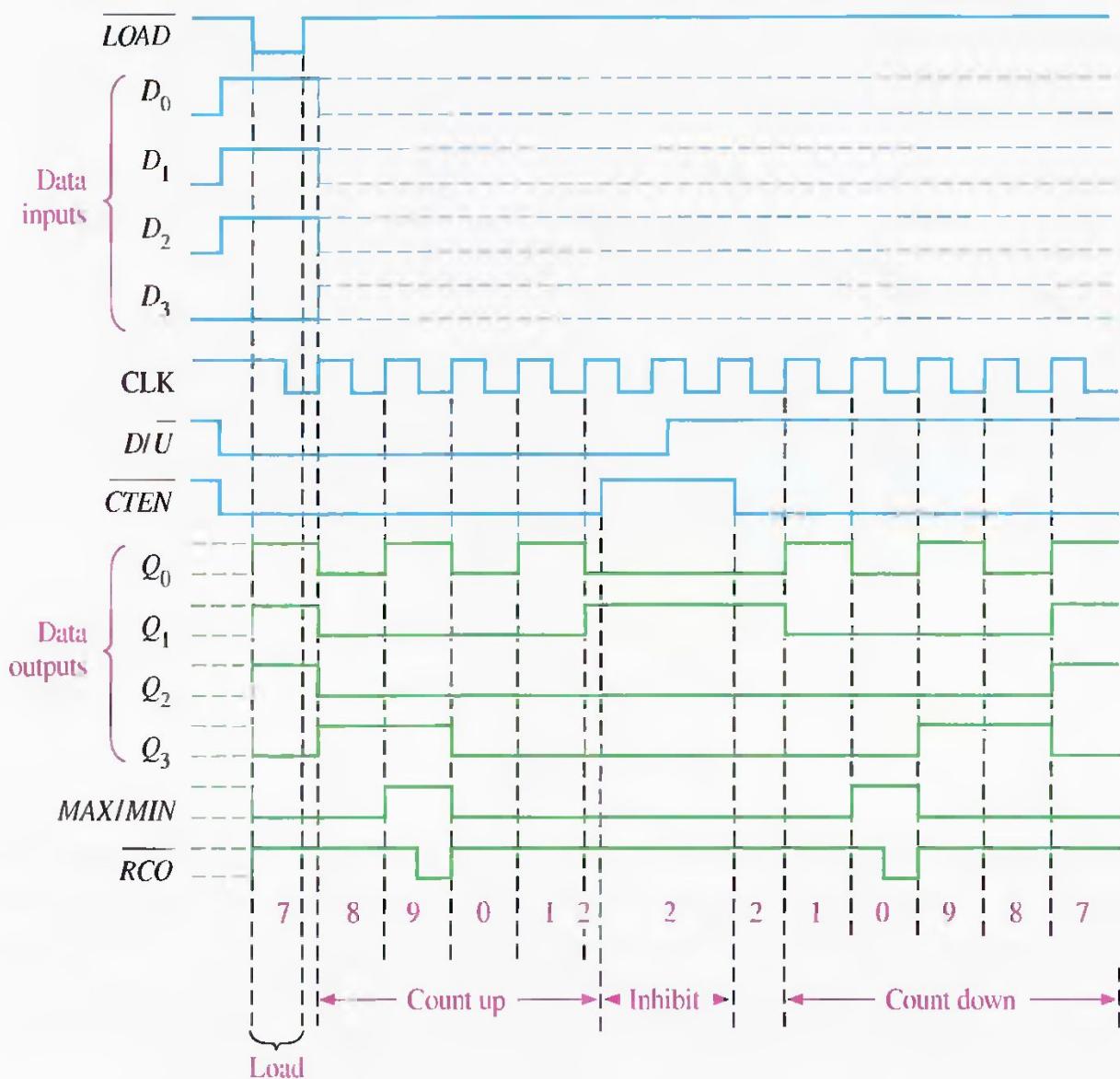
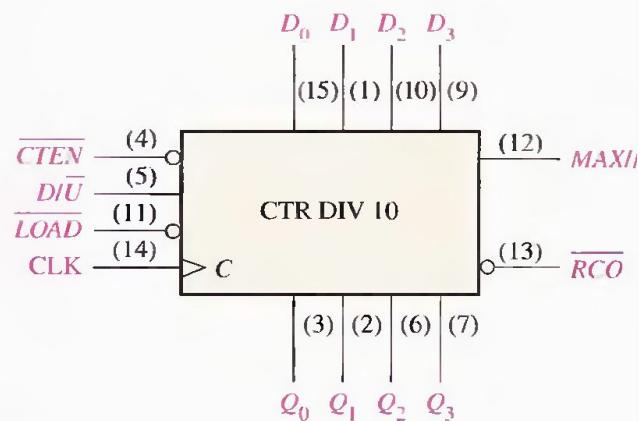
From these Timing waveforms, the counter sequence is as shown in Table

$Q_3$	$Q_2$	$Q_1$	$Q_0$	
0	0	0	0	
0	0	0	1	
0	0	1	0	
0	0	1	1	
0	1	0	0	
0	0	1	1	UP
0	0	1	0	
0	0	0	1	
0	0	0	0	
1	1	1	1	
0	0	0	0	
0	0	0	1	UP
0	0	1	0	
0	0	0	1	
0	0	0	0	DOWN

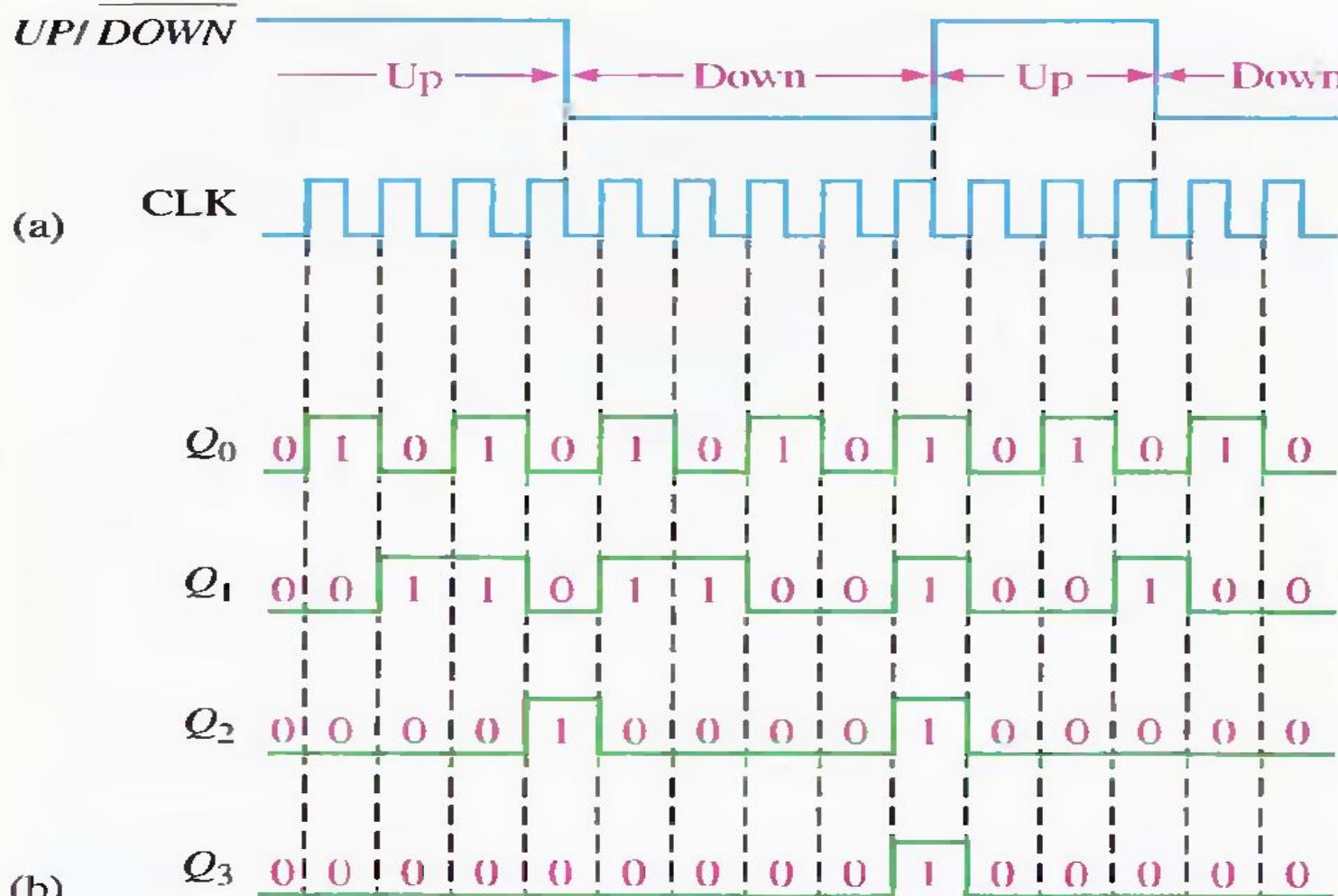
Show the timing diagram if the  $UP/\overline{DOWN}$  control waveform is inverted.



# THE 74HC190 UP/DOWN DECADE COUNTER

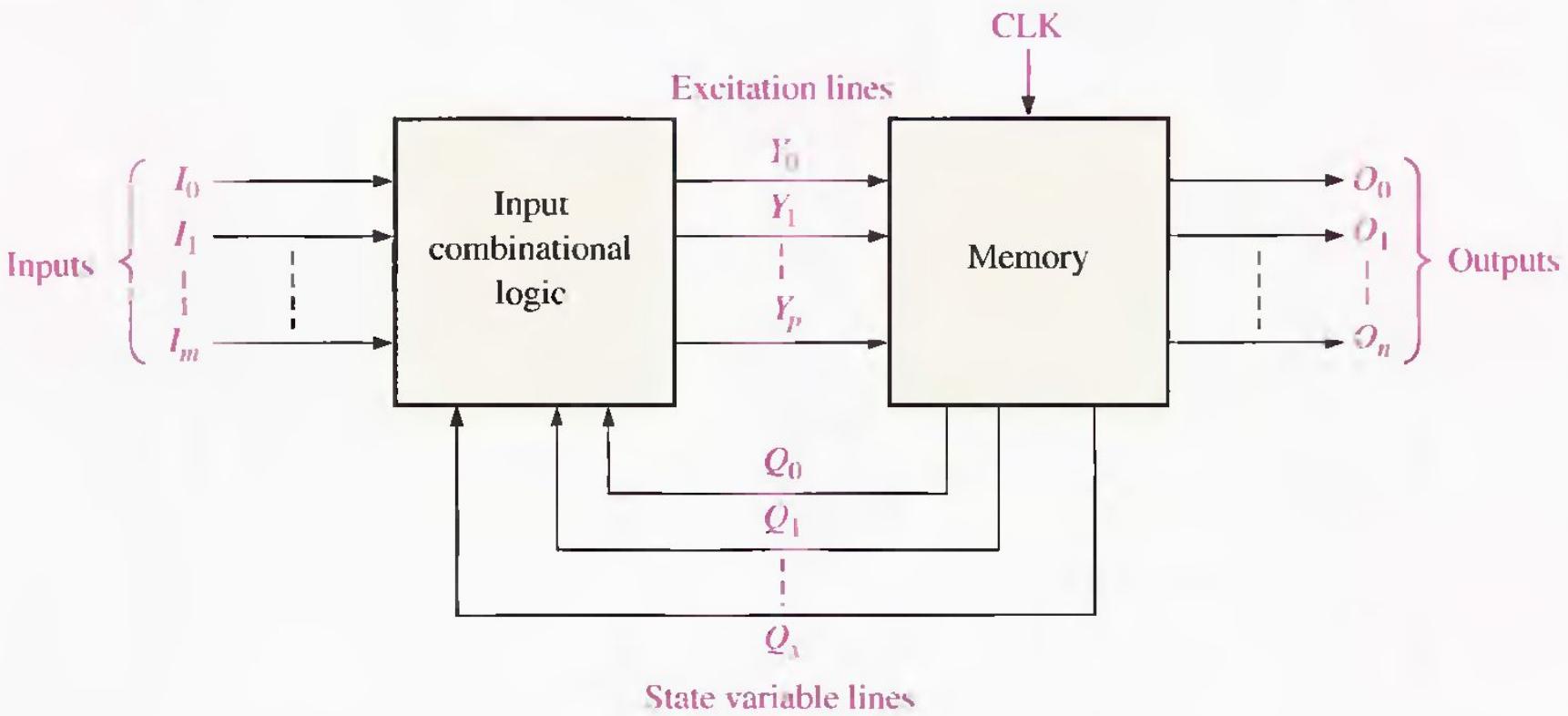


Show the timing diagram and determine the sequence of a 4-bit synchronous binary up/down counter if the clock and *UP/DOWN* control inputs have waveforms as shown in Figure 8–24(a). The counter starts in the all 0s state and is positive edge-triggered.



# DESIGN OF SYNCHRONOUS COUNTERS

## General Model of a Sequential Circuit

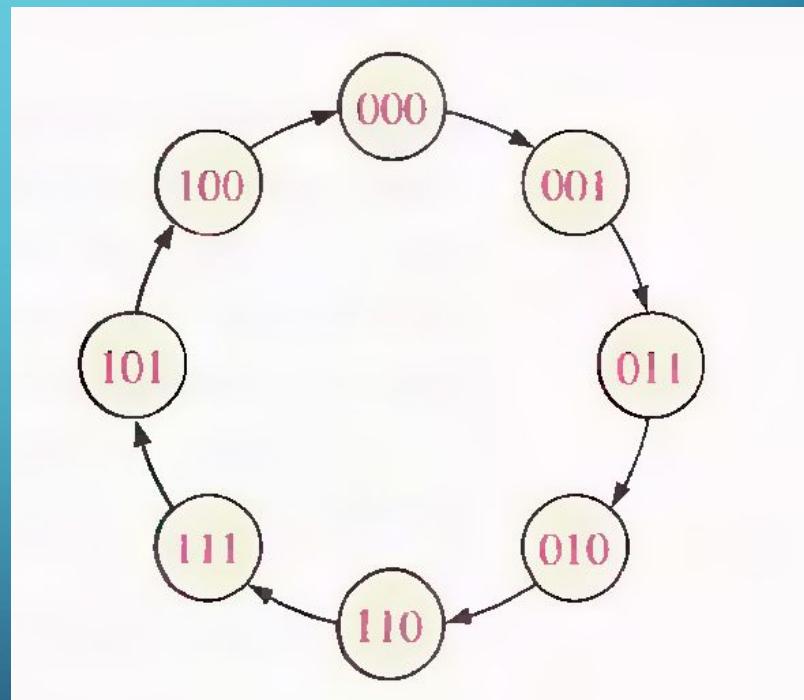


# DESIGN OF SYNCHRONOUS COUNTERS

## Step 1: State Diagram

The first step in the design of a counter is to create a state diagram. A **state diagram** shows the progression of states through which the counter advances when it is clocked.

State diagram for a 3-bit Gray code counter.



# DESIGN OF SYNCHRONOUS COUNTERS

## Step 2: Next-State Table

Next-state table for 3-bit Gray code counter.

PRESENT STATE			NEXT STATE		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

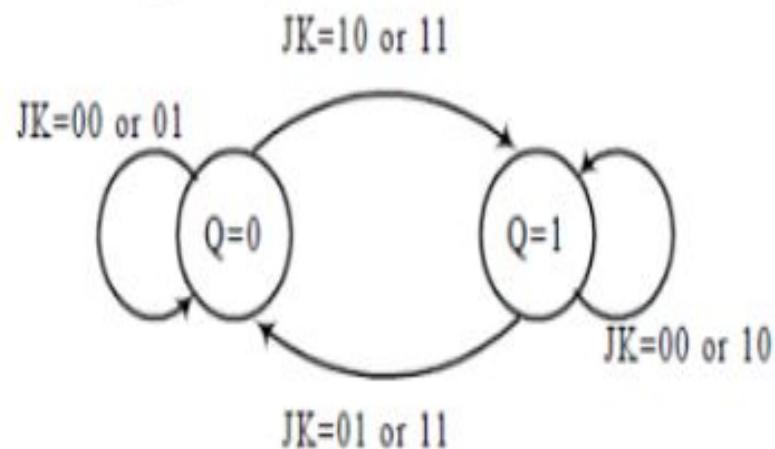
# DESIGN OF SYNCHRONOUS COUNTERS

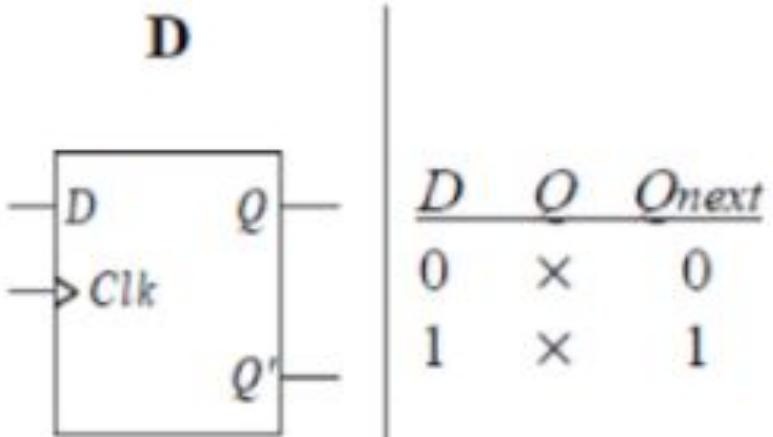
## Step 3: Flip-Flop Transition Table

Transition table for a J-K flip-flop.

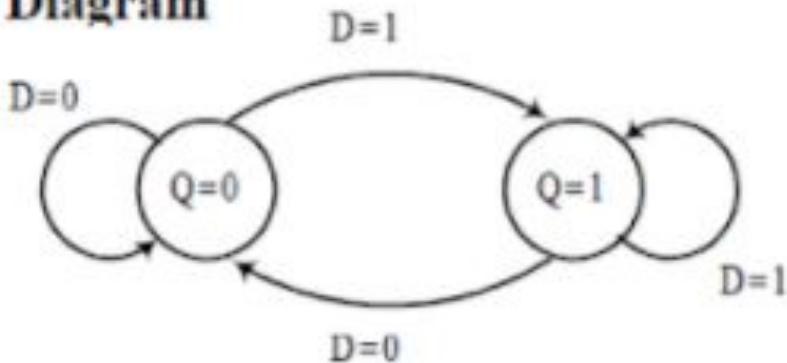
OUTPUT TRANSITIONS		FLIP-FLOP INPUTS	
$Q_N$	$Q_{N+1}$	$J$	$K$
0	→ 0	0	X
0	→ 1	1	X
1	→ 0	X	1
1	→ 1	X	0

$Q_N$ : present state  
 $Q_{N+1}$ : next state  
X: "don't care"





**State Diagram**



Characteristic Equation

$$Q_{\text{next}} = D$$

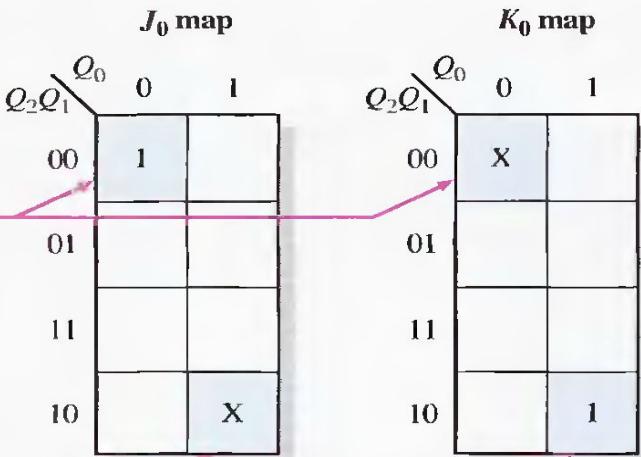
**Excitation Table**

<i>Q</i>	<i>Q<sub>next</sub></i>	<i>D</i>
0	0	0
0	1	1
1	0	0
1	1	1

# DESIGN OF SYNCHRONOUS COUNTERS

## Step 4: Karnaugh Maps

The values of  $J_0$  and  $K_0$  required to produce the transition are placed on each map in the present-state cell.



The values of  $J_0$  and  $K_0$  required to produce the transition are placed on each map in the present-state cell.

Output Transitions		Flip-Flop Inputs	
$Q_N$	$Q_{N+1}$	$J$	$K$
0 → 0		0	X
0 → 1		1	X
1 → 0		X	1
1 → 1		X	0

Flip-flop transition table

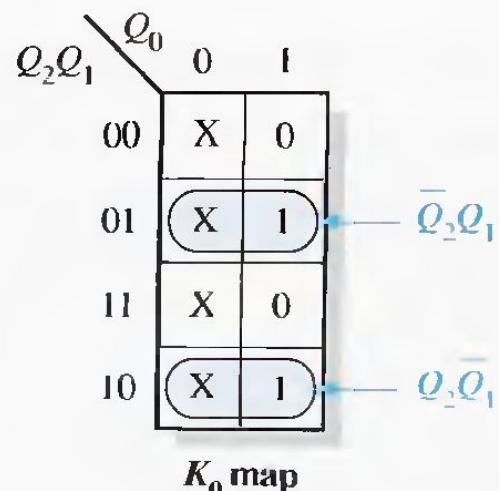
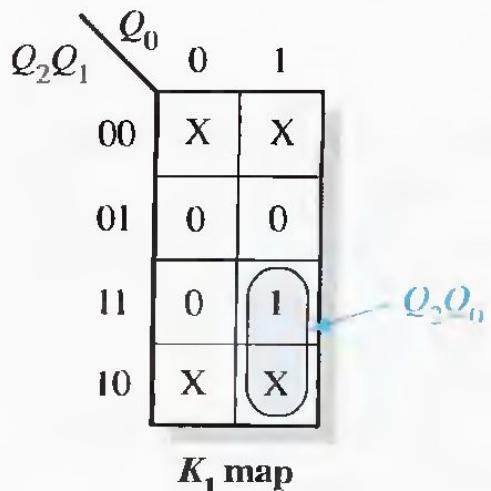
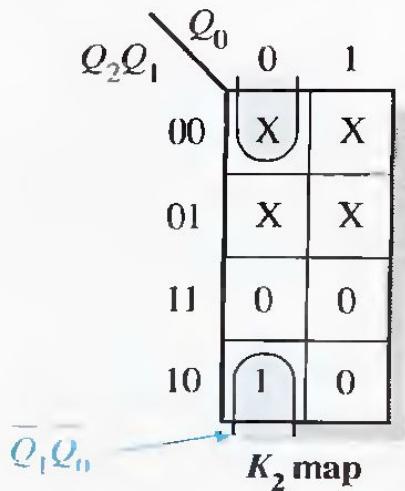
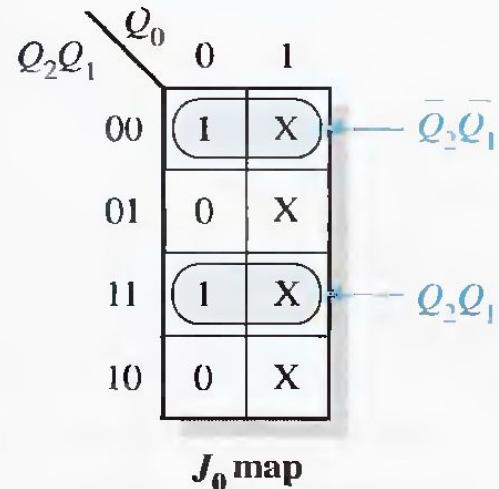
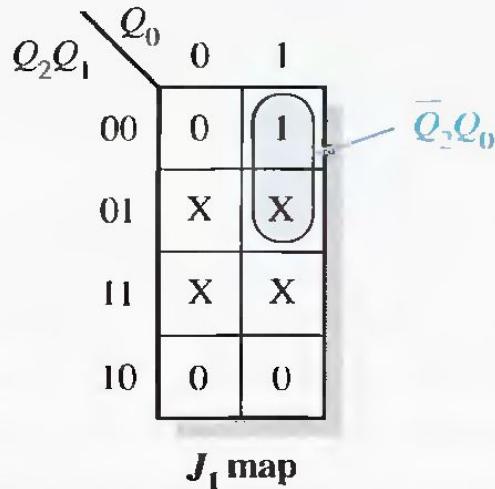
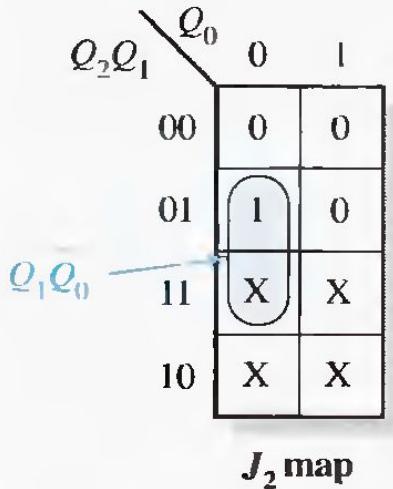
Present State			Next State		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$
0	0	0	0	0	1
0	0	1	0	1	1
0	1	1	0	1	0
0	1	0	1	1	0
1	1	0	1	1	1
1	1	1	1	0	1
1	0	1	1	0	0
1	0	0	0	0	0

Next-state table

For the present state 000,  $Q_0$  makes a transition from 0 to 1 to the next state.

For the present state 101,  $Q_0$  makes a transition from 1 to 0 to the next state.

## Karnaugh maps for present-state $J$ and $K$ inputs.



# DESIGN OF SYNCHRONOUS COUNTERS

## Step 5: Logic Expressions for Flip-Flop Inputs

$$J_0 = Q_2 Q_1 + \bar{Q}_2 \bar{Q}_1 = \overline{Q_2 \oplus Q_1}$$

$$K_0 = Q_2 \bar{Q}_1 + \bar{Q}_2 Q_1 = Q_2 \oplus Q_1$$

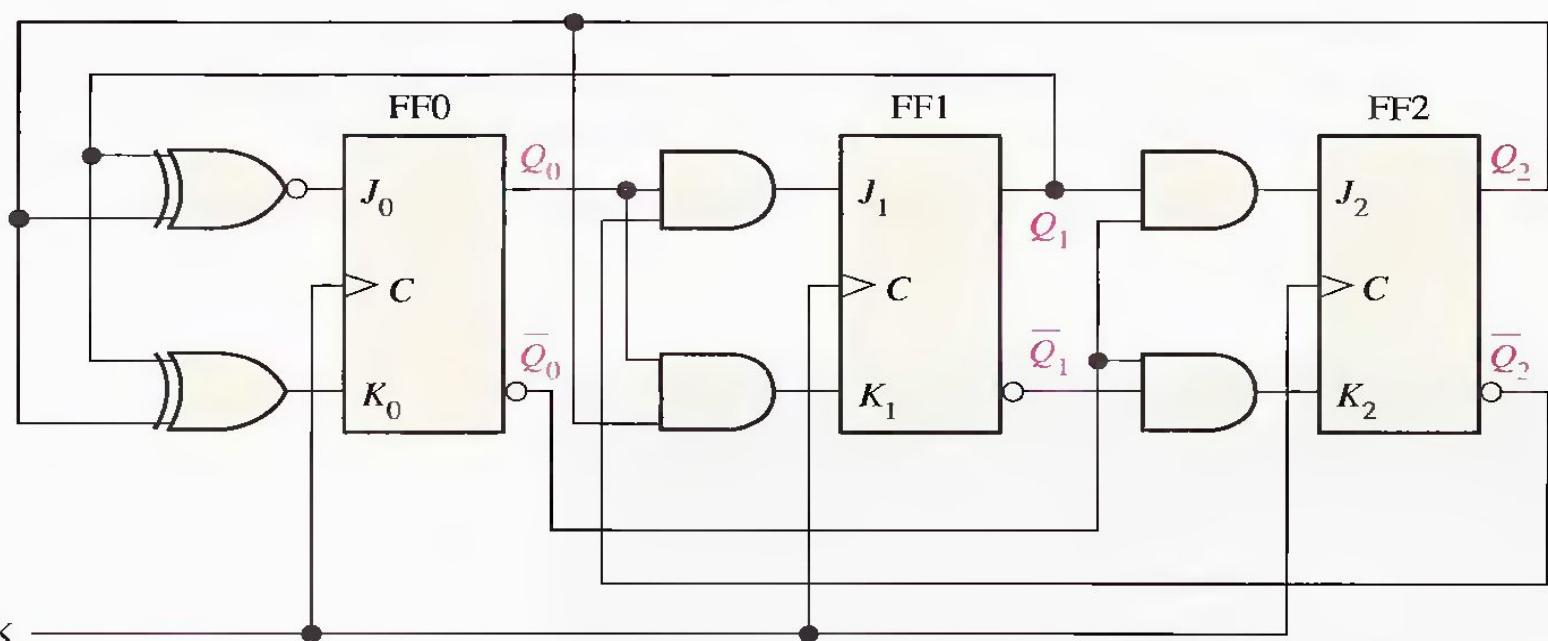
$$J_1 = \bar{Q}_2 Q_0$$

$$K_1 = Q_2 Q_0$$

$$J_2 = Q_1 \bar{Q}_0$$

$$K_2 = \bar{Q}_1 \bar{Q}_0$$

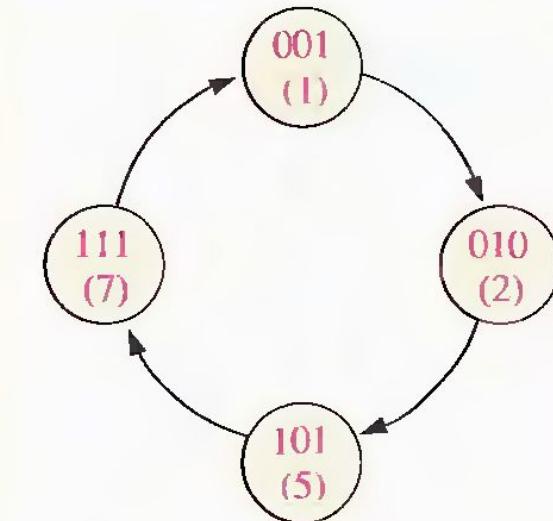
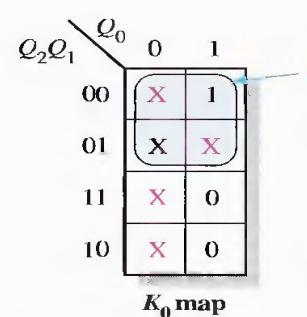
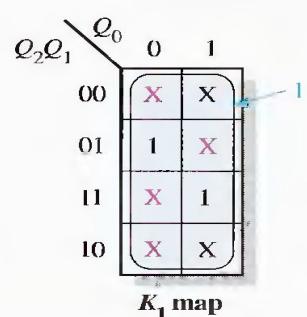
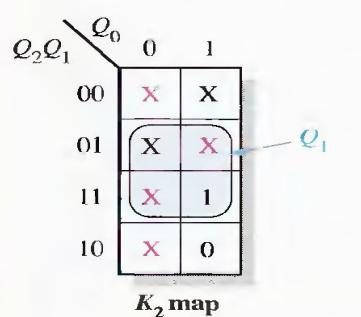
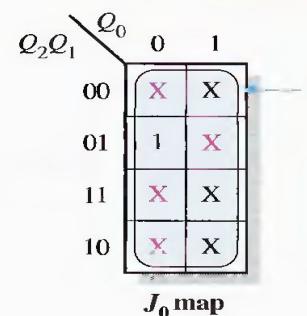
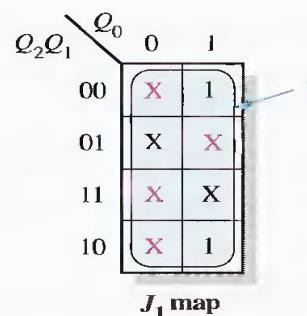
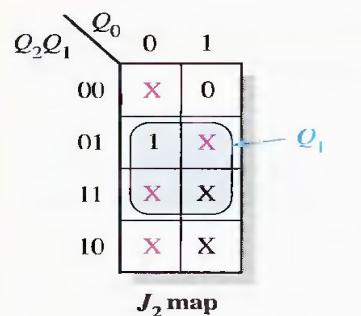
## Step 6: Counter Implementation



Design a counter with the irregular binary count sequence shown in the state diagram of Figure 8–32. Use J-K flip-flops.

**Step 2:** The next-state table is developed from the state diagram and is given in Table 8–9.

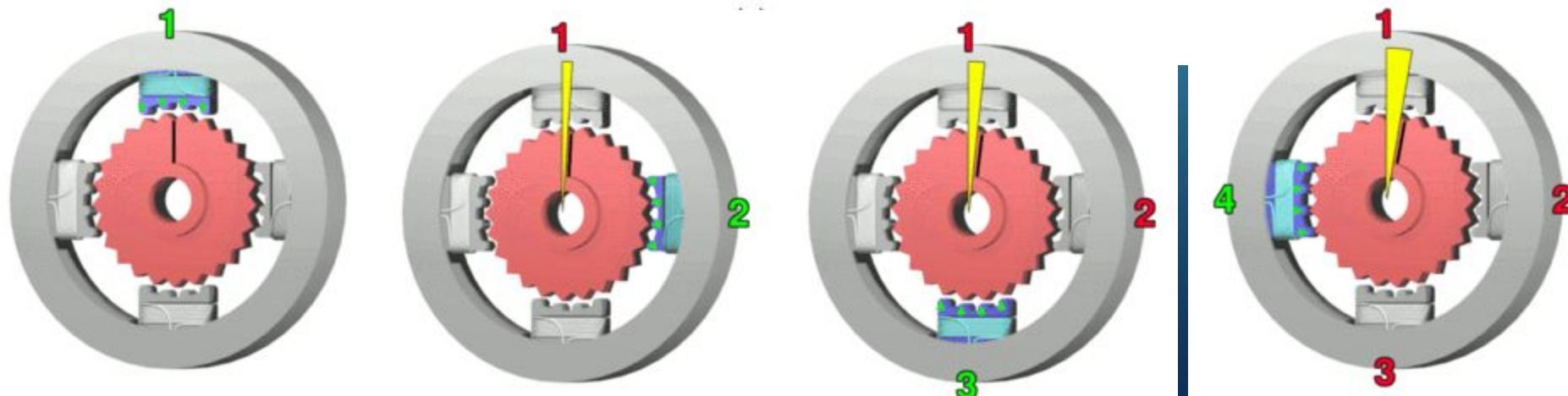
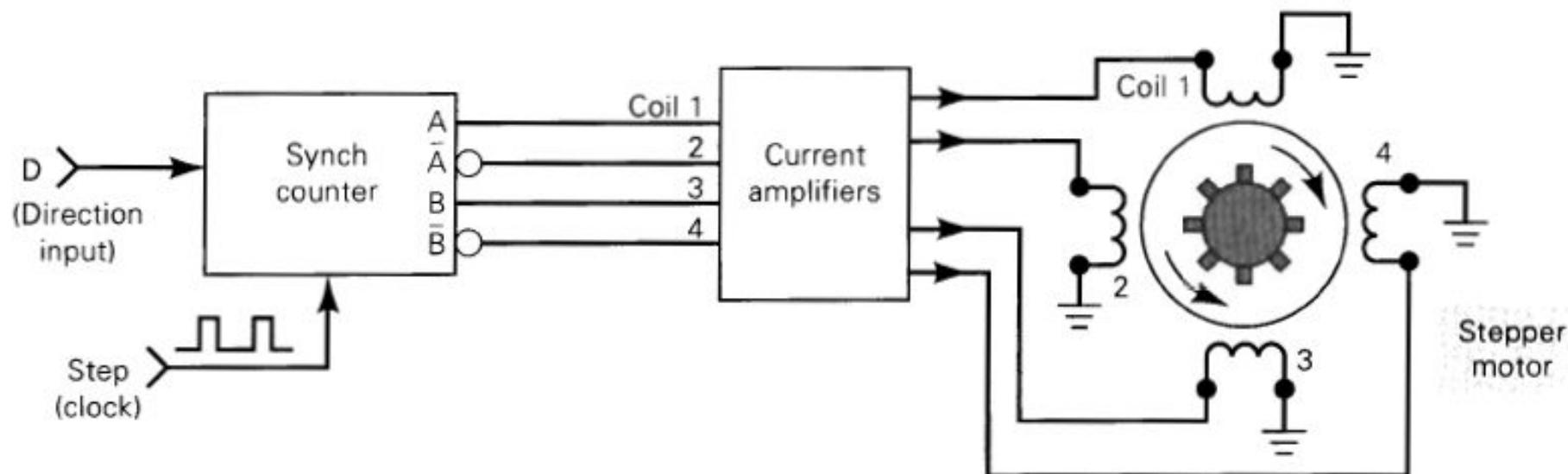
PRESENT STATE			NEXT STATE		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$
0	0	1	0	1	0
0	1	0	1	0	1
1	0	1	1	1	1
1	1	1	0	0	1



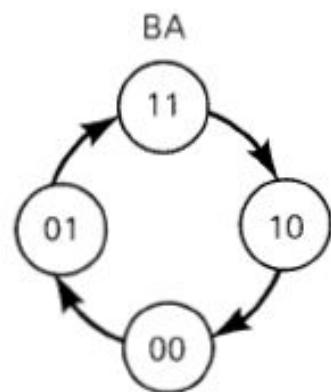
OUTPUT TRANSITIONS		FLIP-FLOP INPUTS	
$Q_N$	$Q_{N+1}$	$J$	$K$
0	→ 0	0	X
0	→ 1	1	X
1	→ 0	X	1
1	→ 1	X	0

# Stepper Motor Control

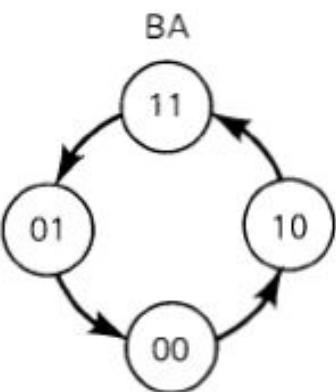
We will now apply this design procedure to a practical situation—driving a *stepper motor*. A stepper motor is a motor that rotates in steps rather than in a continuous motion, typically  $15^\circ$  per step.



CW rotation  
D = 0



CCW rotation  
D = 1



PRESENT State			NEXT State			$J_B$	$K_B$	$J_A$	$K_A$
D	B	A	D	B	A				
0	0	0	0	0	1	0	x	1	x
0	0	1	0	1	1	1	x	x	0
0	1	0	0	0	0	0	1	0	x
0	1	1	0	1	0	0	x	x	1
1	0	0	1	1	0	1	x	0	x
1	0	1	1	0	0	0	0	x	1
1	1	0	1	1	1	1	x	0	1
1	1	1	1	0	1	0	x	1	0

	$\bar{D}$	D	
$\bar{B}A$	0	1	
$\bar{B}A$	1	0	
BA	x	x	
BA	x	x	

$$J_B = \bar{D}A + D\bar{A} \\ = D \oplus A$$

	$\bar{D}$	D	
$\bar{B}A$	x	x	
$\bar{B}A$	x	x	
BA	0	1	
BA	1	0	

$$K_B = \bar{D}A + D\bar{A} \\ = D \oplus A$$

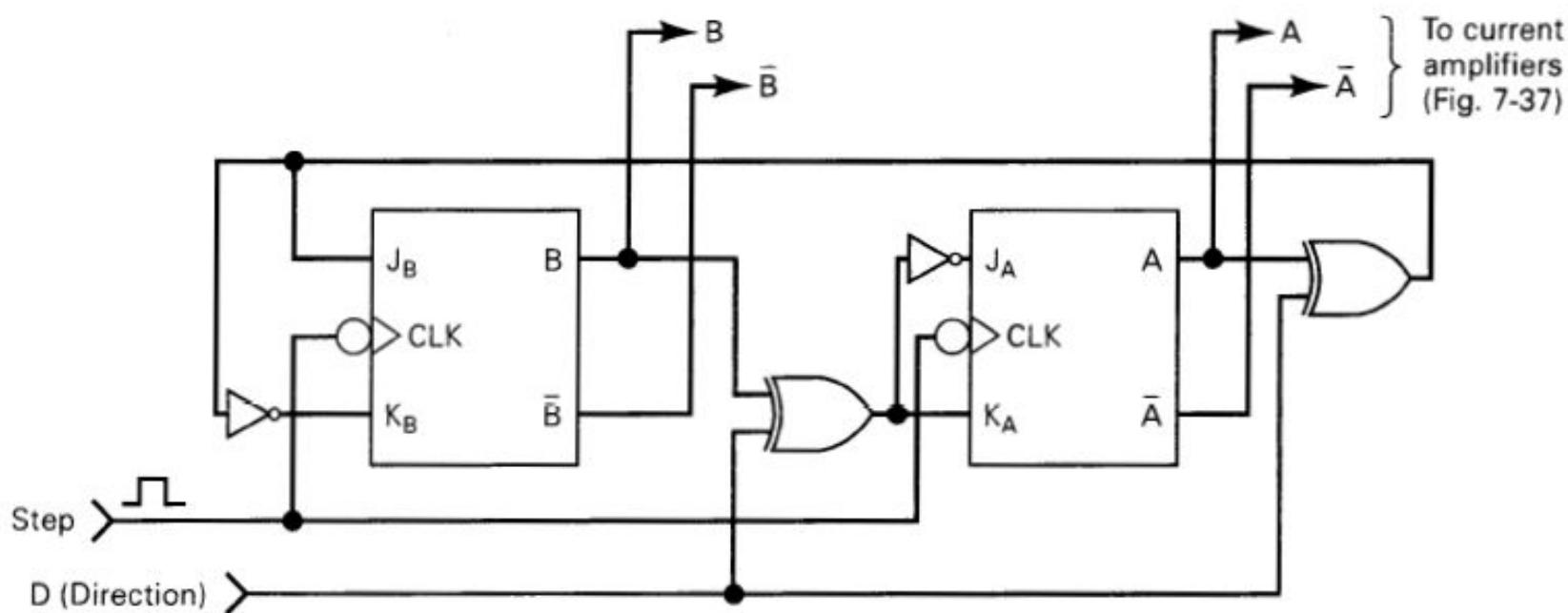
	$\bar{D}$	D	
$\bar{B}A$	1	0	
$\bar{B}A$	x	x	
BA	x	x	
BA	0	1	

$$J_A = \bar{D}\bar{B} + D\bar{B} \\ = D \oplus B$$

	$\bar{D}$	D	
$\bar{B}A$	x	x	
$\bar{B}A$	0	1	
BA	1	0	
BA	x	x	

$$K_A = \bar{D}\bar{B} + D\bar{B} \\ = D \oplus B$$

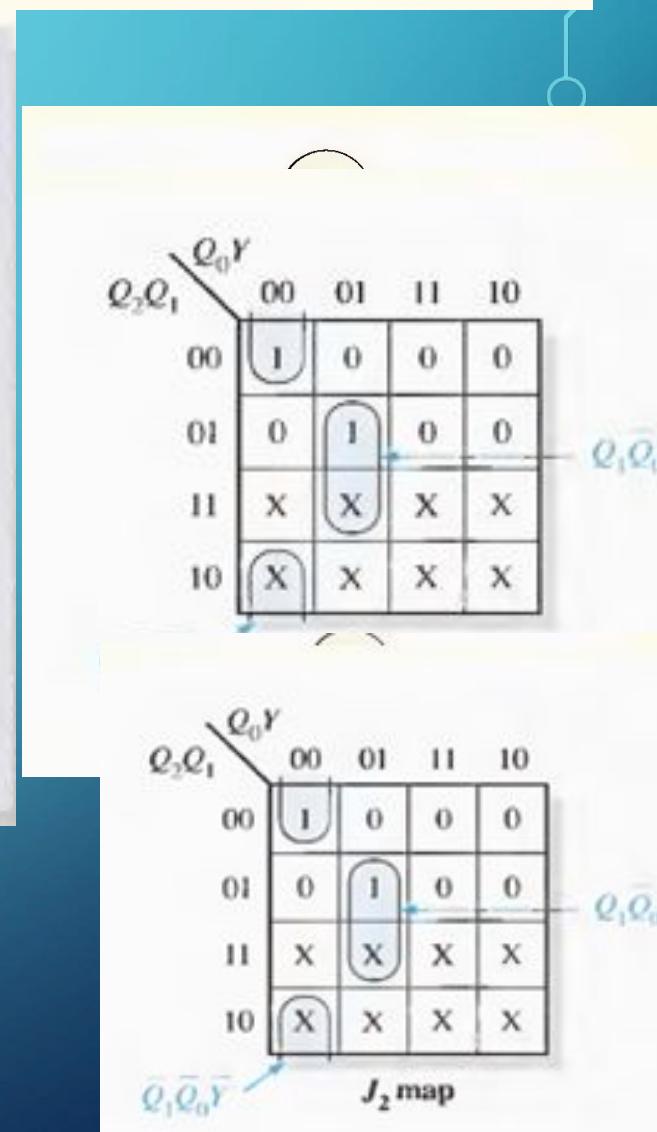
## Synchronous counter implemented from the $J$ , $K$ equations.



Develop a synchronous 3-bit up/down counter with a Gray code sequence. The counter should count up when an UP/DOWN control input is 1 and count down when the control input is 0.

PRESENT STATE			NEXT STATE					
			$Y = 0$ (DOWN)			$Y = 1$ (UP)		
$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$	$Q_2$	$Q_1$	$Q_0$
0	0	0	1	0	0	0	0	1
0	0	1	0	0	0	0	1	1
0	1	1	0	0	1	0	1	0
0	1	0	0	1	1	1	1	0
1	1	0	0	1	0	1	1	1
1	1	1	1	1	0	1	0	1
1	0	1	1	1	1	1	0	0
1	0	0	1	0	1	0	0	0

$Y$  = UP/DOWN control input.



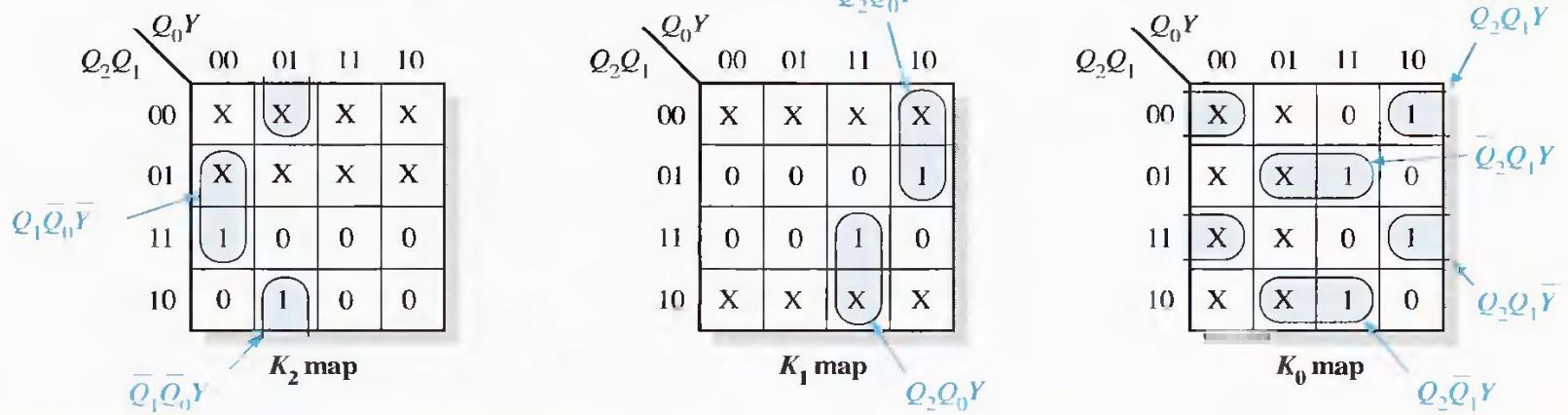
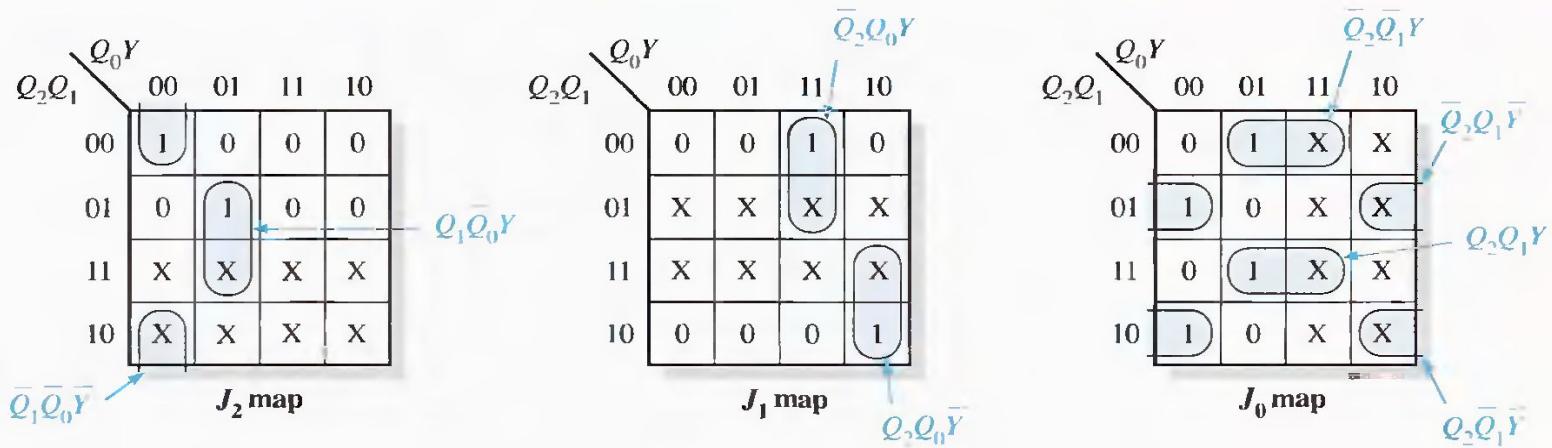


FIGURE 8-36

$$J_0 = Q_2 Q_1 Y + Q_2 \bar{Q}_1 \bar{Y} + \bar{Q}_2 \bar{Q}_1 Y + \bar{Q}_2 \bar{Q}_1 \bar{Y}$$

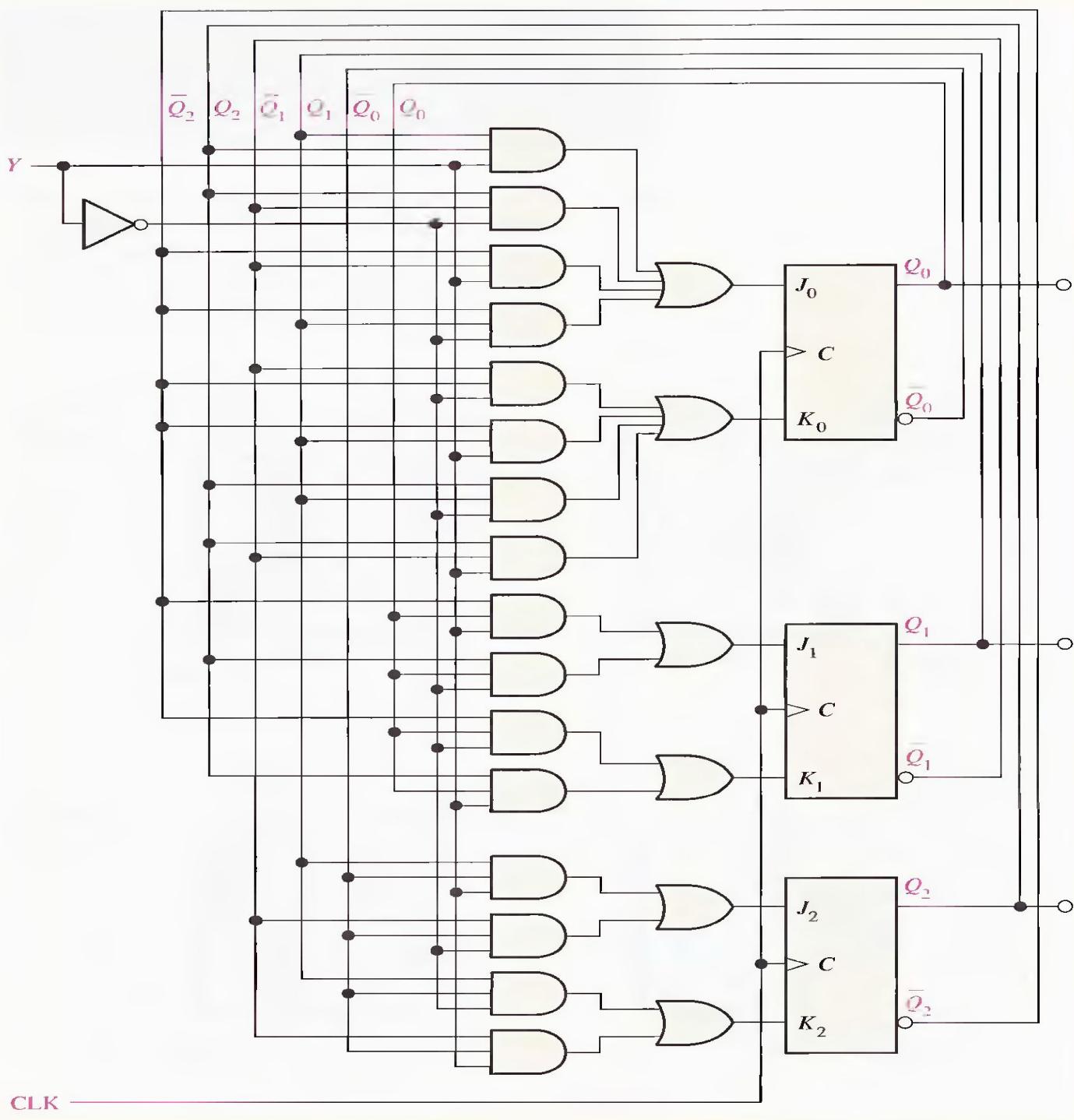
$$J_1 = \bar{Q}_2 Q_0 Y + Q_2 Q_0 \bar{Y}$$

$$J_2 = Q_1 \bar{Q}_0 Y + \bar{Q}_1 \bar{Q}_0 \bar{Y}$$

$$K_0 = \bar{Q}_2 \bar{Q}_1 \bar{Y} + \bar{Q}_2 Q_1 Y + Q_2 \bar{Q}_1 Y + Q_2 Q_1 \bar{Y}$$

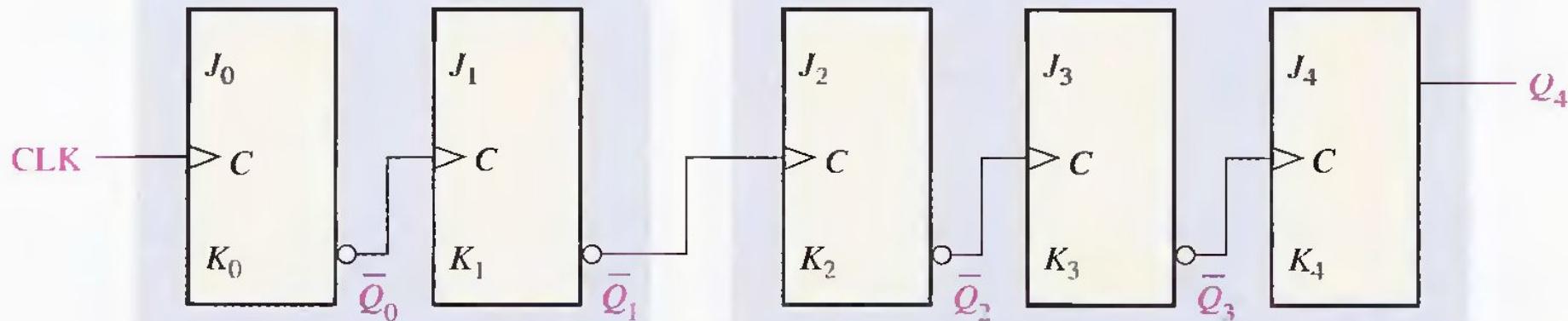
$$K_1 = \bar{Q}_2 Q_0 \bar{Y} + Q_2 Q_0 Y$$

$$K_2 = Q_1 \bar{Q}_0 \bar{Y} + \bar{Q}_1 \bar{Q}_0 Y$$

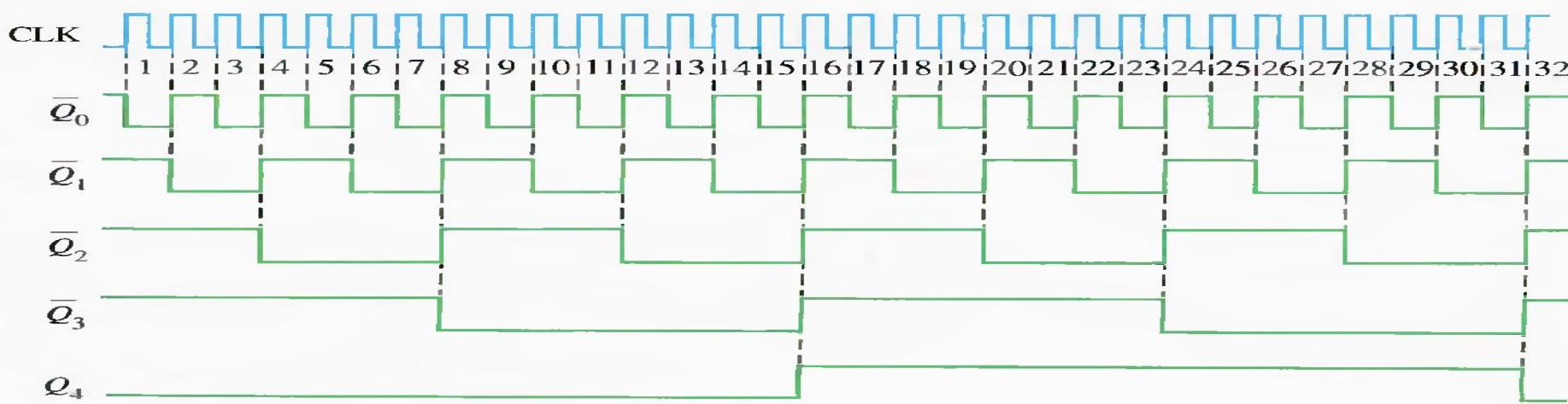


# CASCADED COUNTERS

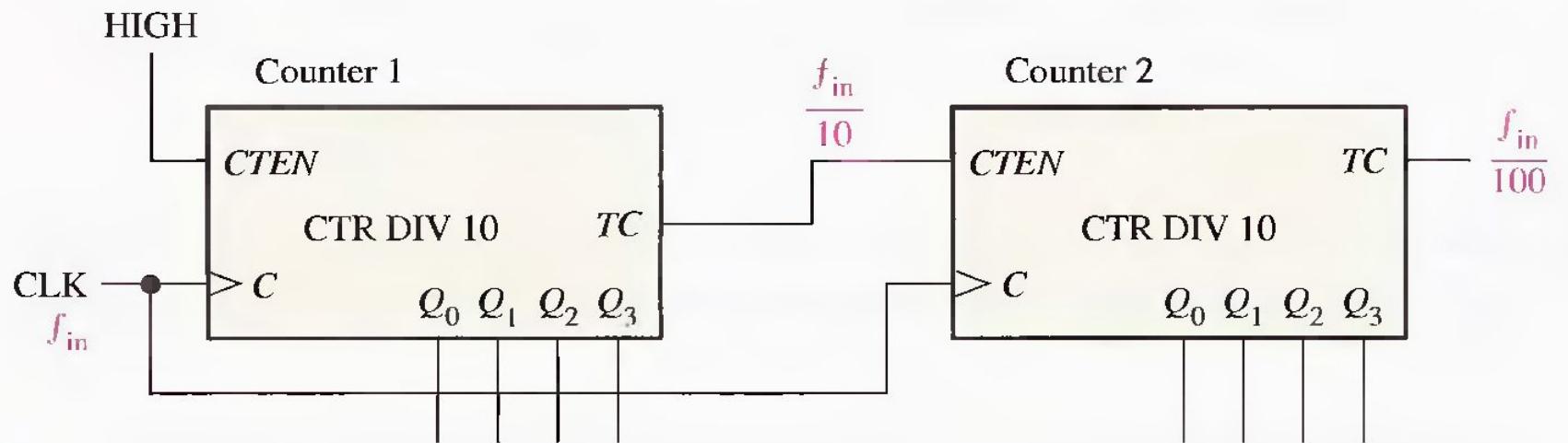
Counters can be connected in cascade to achieve higher-modulus operation. In essence, **cascading** means that the last-stage output of one counter drives the input of the next counter.



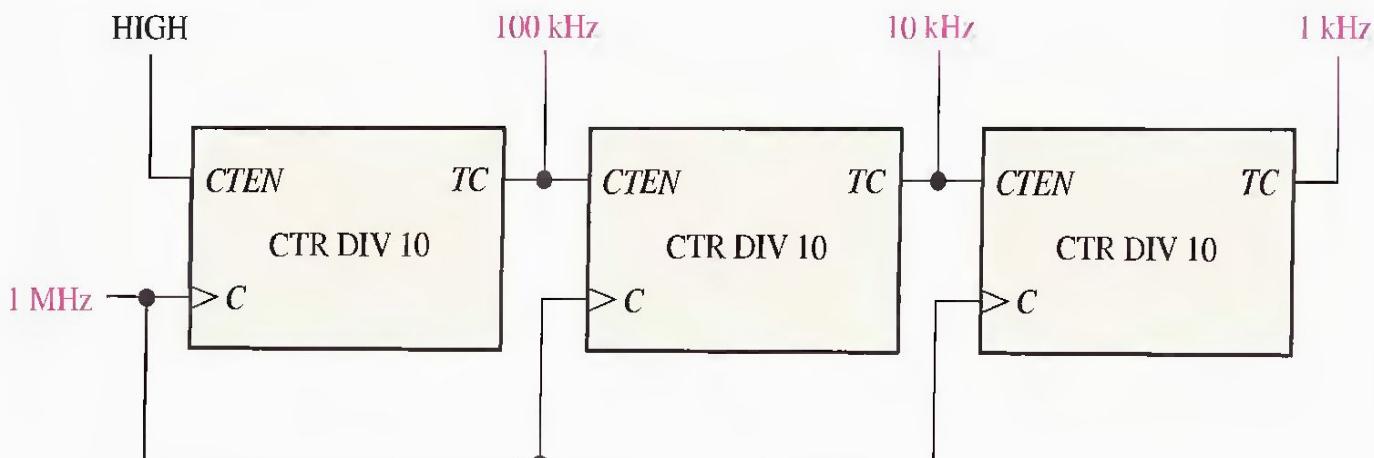
Modulus-4 counter



A modulus-100 counter using two cascaded decade counters.

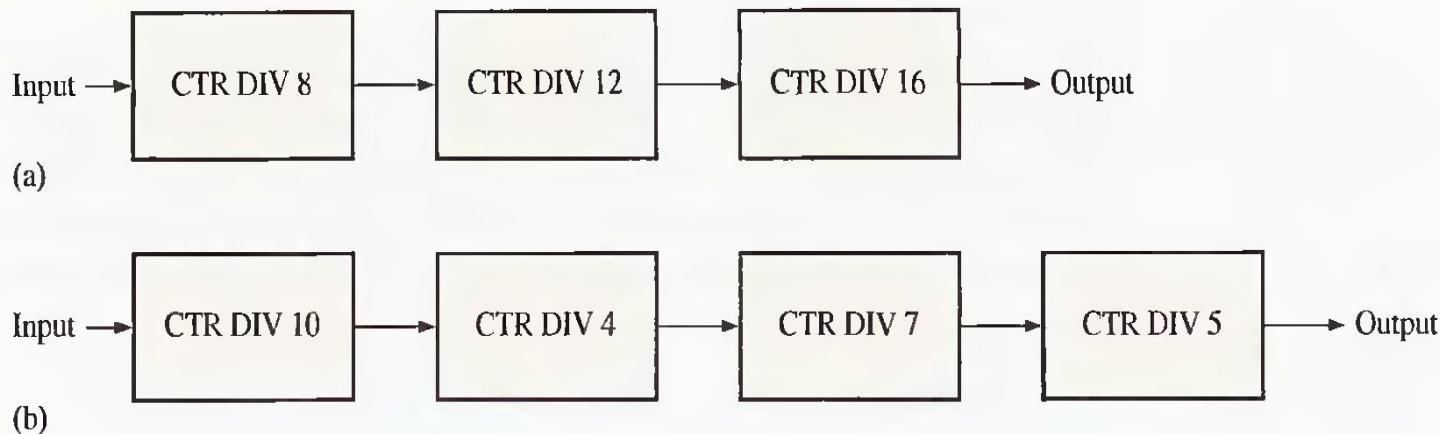


Three cascaded decade counters forming a divide-by-1000 frequency divider with intermediate divide-by-10 and divide-by-100 outputs.



## EXAMPLE 8-7

Determine the overall modulus of the two cascaded counter configurations in Figure 8-42.



▲ FIGURE 8-42

**Solution** In Figure 8-42(a), the overall modulus for the 3-counter configuration is

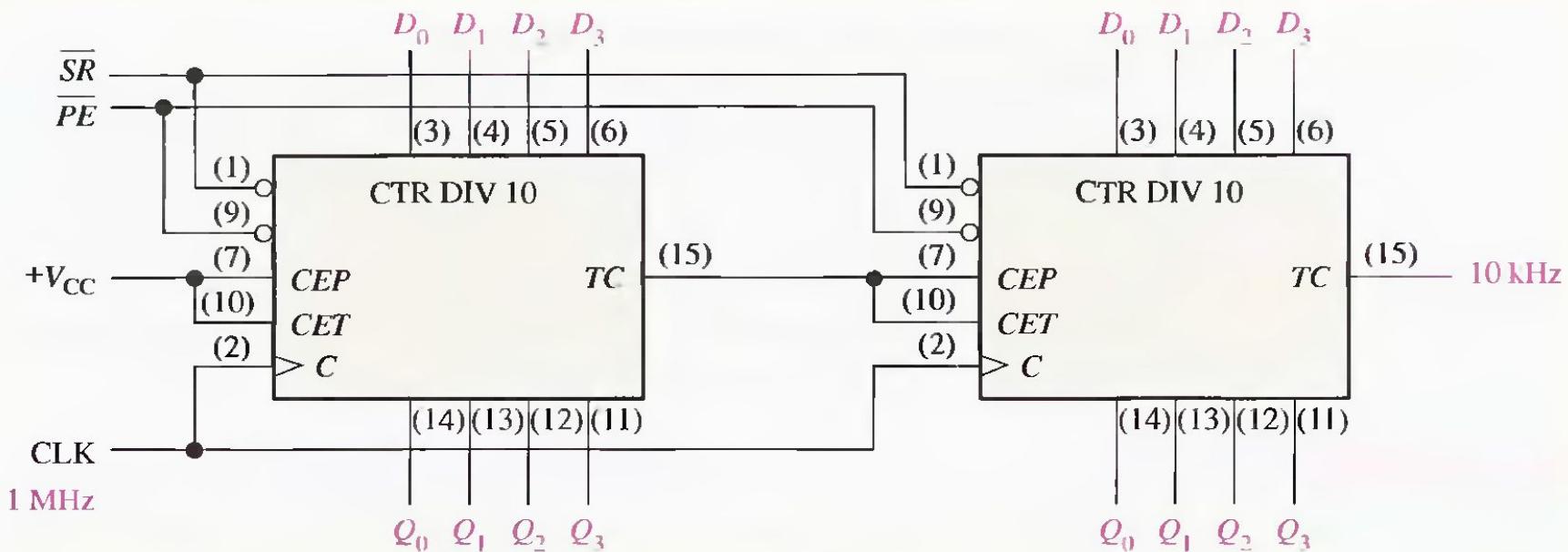
$$8 \times 12 \times 16 = 1536$$

In Figure 8-42(b), the overall modulus for the 4-counter configuration is

$$10 \times 4 \times 7 \times 5 = 1400$$

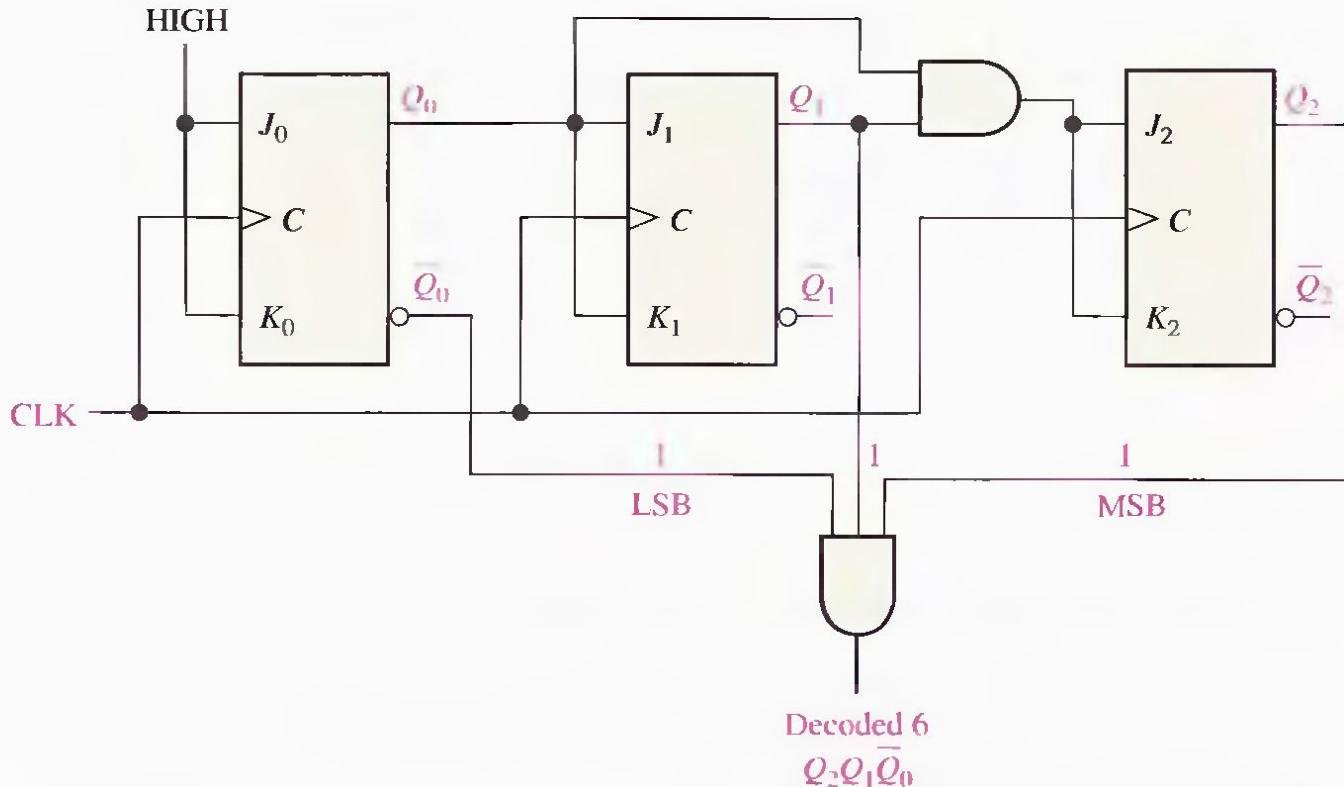
Use 74F162 decade counters to obtain a 10 kHz waveform from a 1 MHz clock. Show the logic diagram.

**Solution** To obtain 10 kHz from a 1 MHz clock requires a division factor of 100. Two 74F162 counters must be cascaded as shown in Figure 8–43. The left counter produces a *TC* pulse for every 10 clock pulses. The right counter produces a *TC* pulse for every 100 clock pulses.

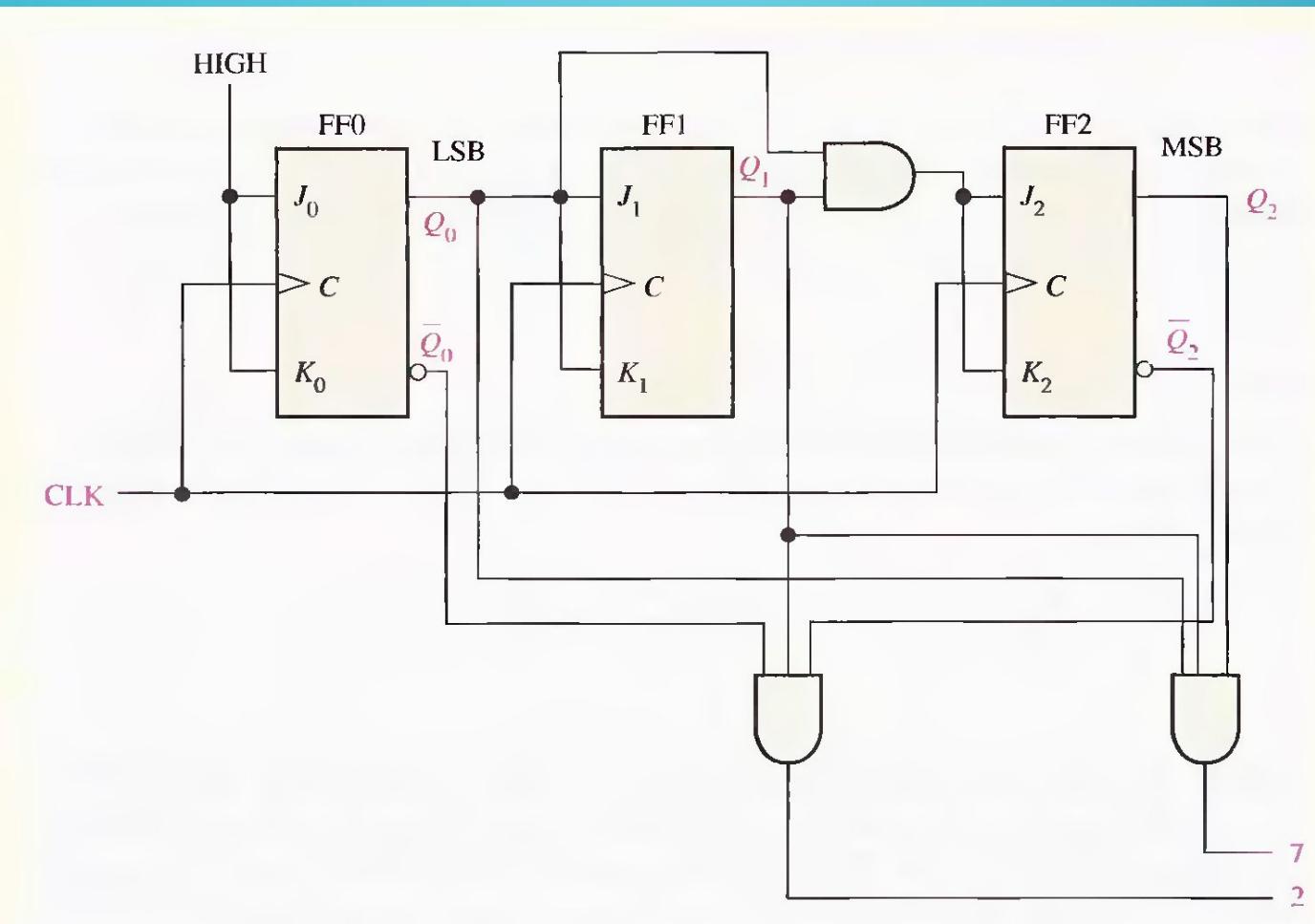


# COUNTER DECODING

Suppose that you wish to decode binary state 6 (110) of a 3-bit binary counter. When  $Q_2 = 1$ ,  $Q_1 = 1$ , and  $Q_0 = 0$ , a HIGH appears on the output of the decoding gate, indicating that the counter is at state 6. This can be done as shown in Figure 8–45. This is called *active-HIGH decoding*. Replacing the AND gate with a NAND gate provides active-LOW decoding.



Implement the decoding of binary state 2 and binary state 7 of a 3-bit synchronous counter. Show the entire counter timing diagram and the output waveforms of the decoding gates. Binary 2 =  $\bar{Q}_2\bar{Q}_1\bar{Q}_0$  and binary 7 =  $Q_2Q_1Q_0$ .



Implement the decoding of binary state 2 and binary state 7 of a 3-bit synchronous counter. Show the entire counter timing diagram and the output waveforms of the decoding gates. Binary 2 =  $\bar{Q}_2\bar{Q}_1\bar{Q}_0$  and binary 7 =  $Q_2Q_1Q_0$ .

