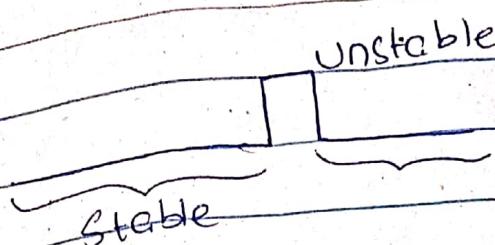
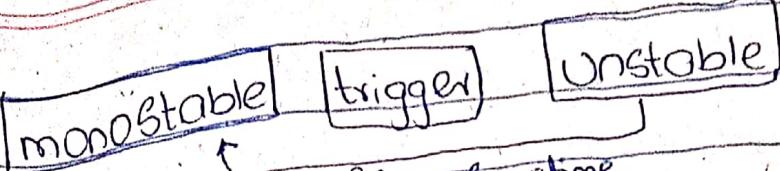
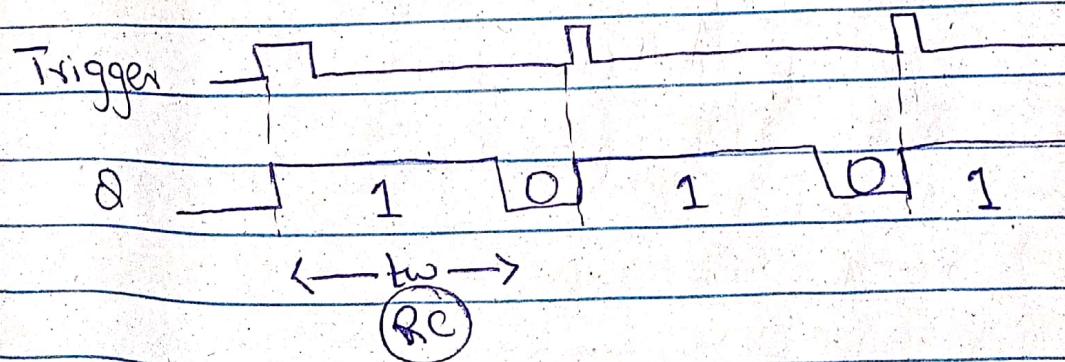
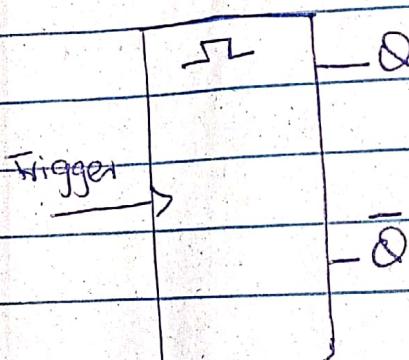


One-Shot

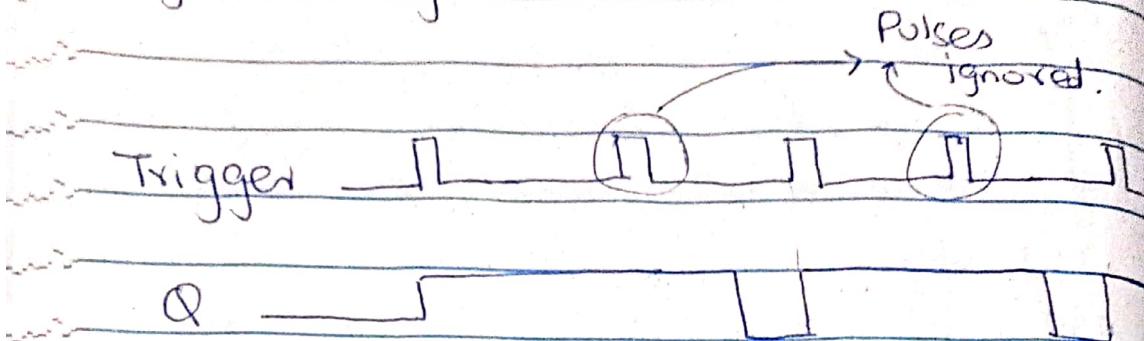


To summarize, the output of inverter G₂ goes High in response to the trigger input. It remains high High for a time set by the RC time constant. At the end of this time it goes Low.



If frequency of trigger is faster than
then pulse rate then

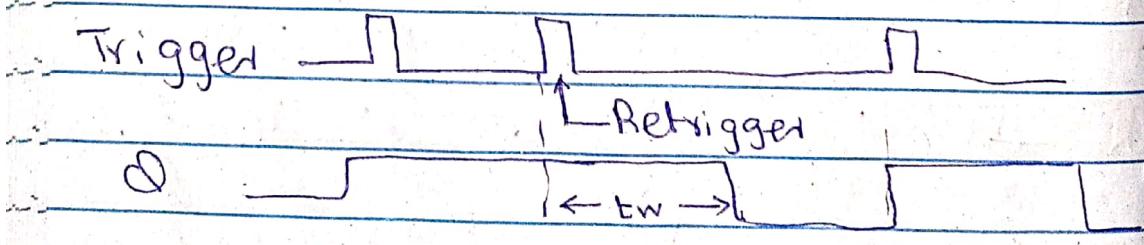
If frequency of trigger is faster than the pulse rate, then these pulses are ignored by one-shot.



To solve this issue either:

- Use a capacitor that reduces time period of pulse of Q.
- Use retriggerable one-shots.

Alters capacitors or use external resistors, we can change pulse-width as it will retrigger the one shot.



Shift Register Input/Output types

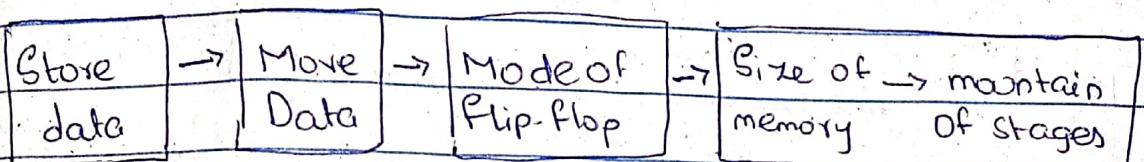
How many bits can one flip-flop store?

Ans) Only 1 bit can be stored that is called Q (either 1 or 0).

Set $Q = 1$

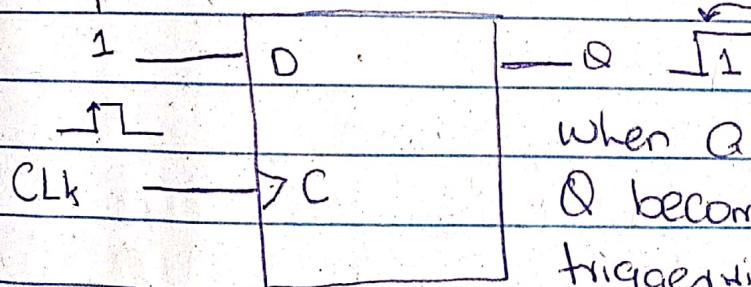
Reset $Q = 0$

Digital Circuit



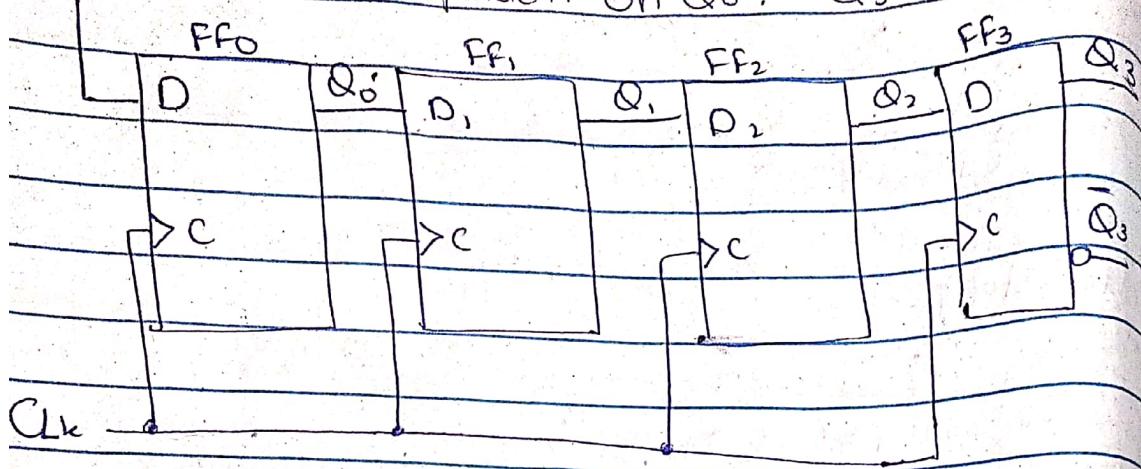
D - flipflop +ve edge triggered will be used

→ 1 is stored and appears on output



When Q 1 is on 0,
Q becomes a 1 at the
triggering edge of Clk,
Or remains a 1 if
already in set state.
For 0 vice-versa.

Serial In / Serial Out Shift Registers :



At first clock trigger, the Q₀ will be sent in ff1, then after second clock trigger Q₁ will be sent to ff2, then after third CLK trigger Q₂ will be sent to ff3 and so on.

For Spawning Data:-

Clk	FF ₀ (Q ₀)	FF ₁ (Q ₁)	FF ₂ (Q ₂)	FF ₃ (Q ₃)
Initial	0	0	0	0
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	0	1	0

For Saving Data:- $Q_3 Q_2 Q_1 Q_0 = 0101$

	(Q_0)	(Q_1)	(Q_2)	(Q_3)
Clk	FF ₀	FF ₁	FF ₂	FF ₃ (Q_3)
Initial	0	0	0	0
1	0	0	0	0
2	1	0	0	0
3	0	1	0	0
4	1	0	1	0

Reading Data :-

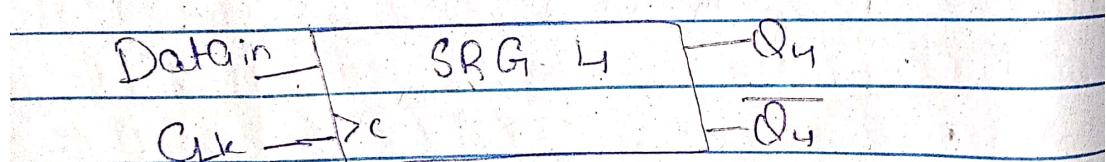
Clk	FF ₀	FF ₁	FF ₂	FF ₃
Initial	1	0	1	0 →
5	0	1	0	1 →
6	0	0	1	0 →
7	0	0	0	1 →
8	0	0	0	0

Output 01010

Note: For a 5 bit register Connect
5 ~~FF~~ Flip-flops.

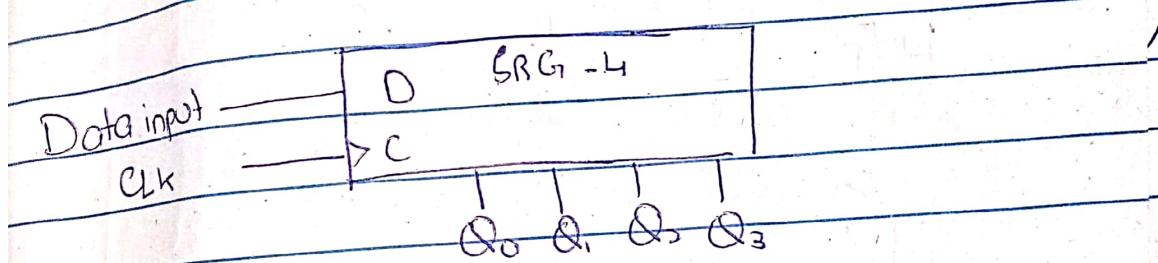
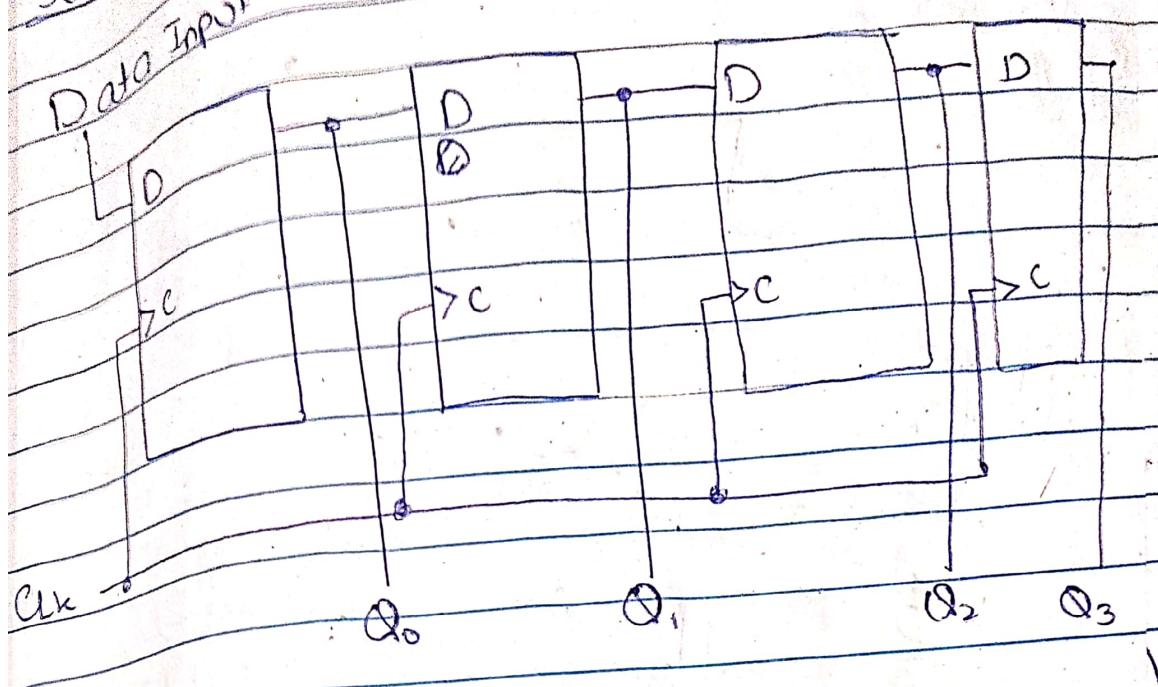
The first data bit is entered into the register on the first clock pulse and then shifted from left to right as the remaining bits are entered and shifted. The register contains $Q_4 Q_3 Q_2 Q_1 Q_0 = 11010$ after five clock pulses.

Clk	1	1	0	1	0	
Data input	1	1	0	1	0	
Q_0	1	1	0	1	0	
Q_1	0	1	1	0	1	
Q_2	0	1	1	1	0	
Q_3			1	1		
Q_4				1		
Output 11010						



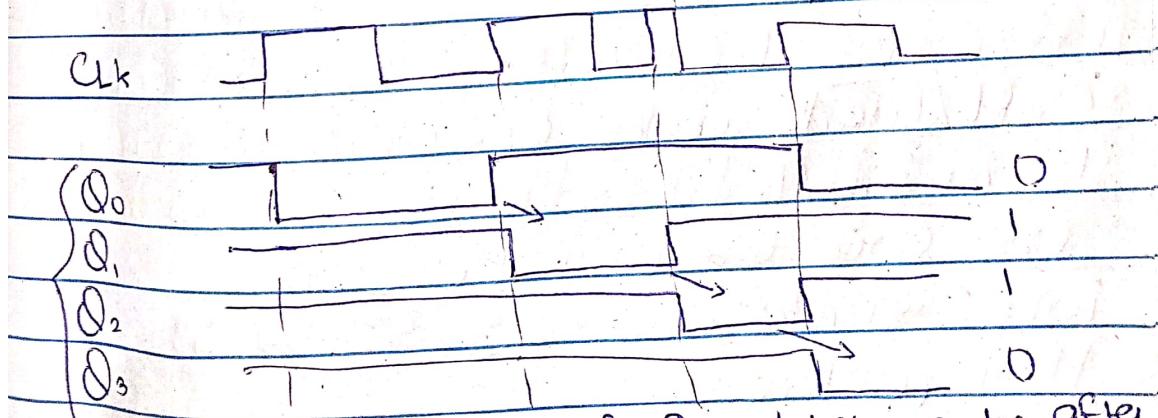
4 bit Serial Register.

Serial In / Parallel Out / Shift Registers :-



Only readable after 4 cycle

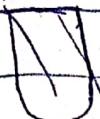
Data in	0	1	1	0	initially 1
---------	---	---	---	---	-------------



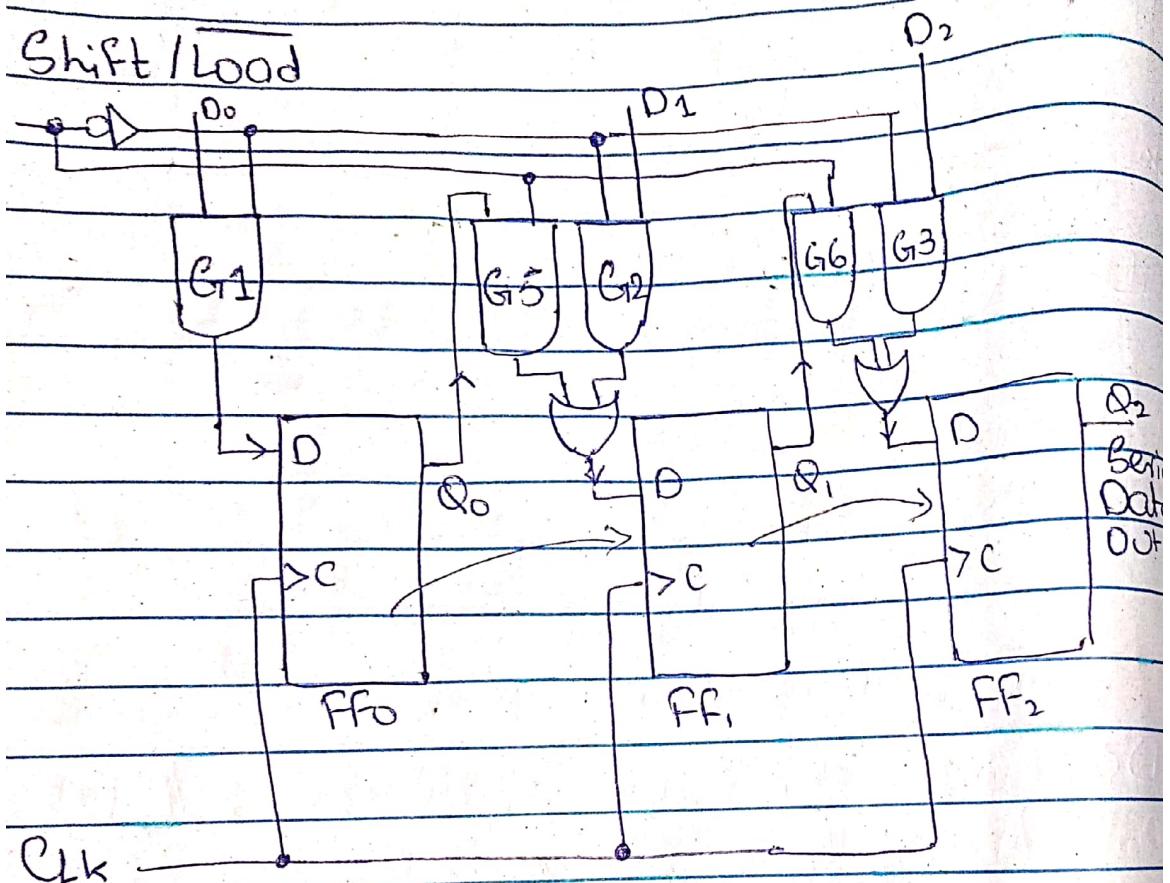
Q₃ gets data of Q₂ which gets after every pulse, data of Q₁ will receive data of Q₀.

Parallel In / Serial Out Shift Registers:-

Shift / Load



Shift / Load

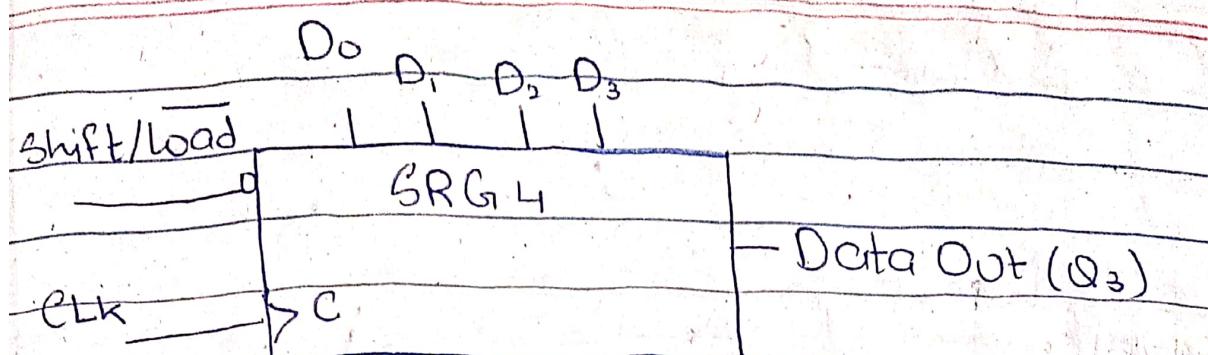


Shift / Load works on Active, low inputs.
When Shift / Load is 1 G1 is low and
G5 and G6 will be Active.

When Shift / Load is 0 G1, G2, G3 will be
High (Active).

At 0 loading is occurred and data is loaded
in flip-flops

At Shift (i.e 1) the data will be shifted in flip-flops to right and output at Q_3 .

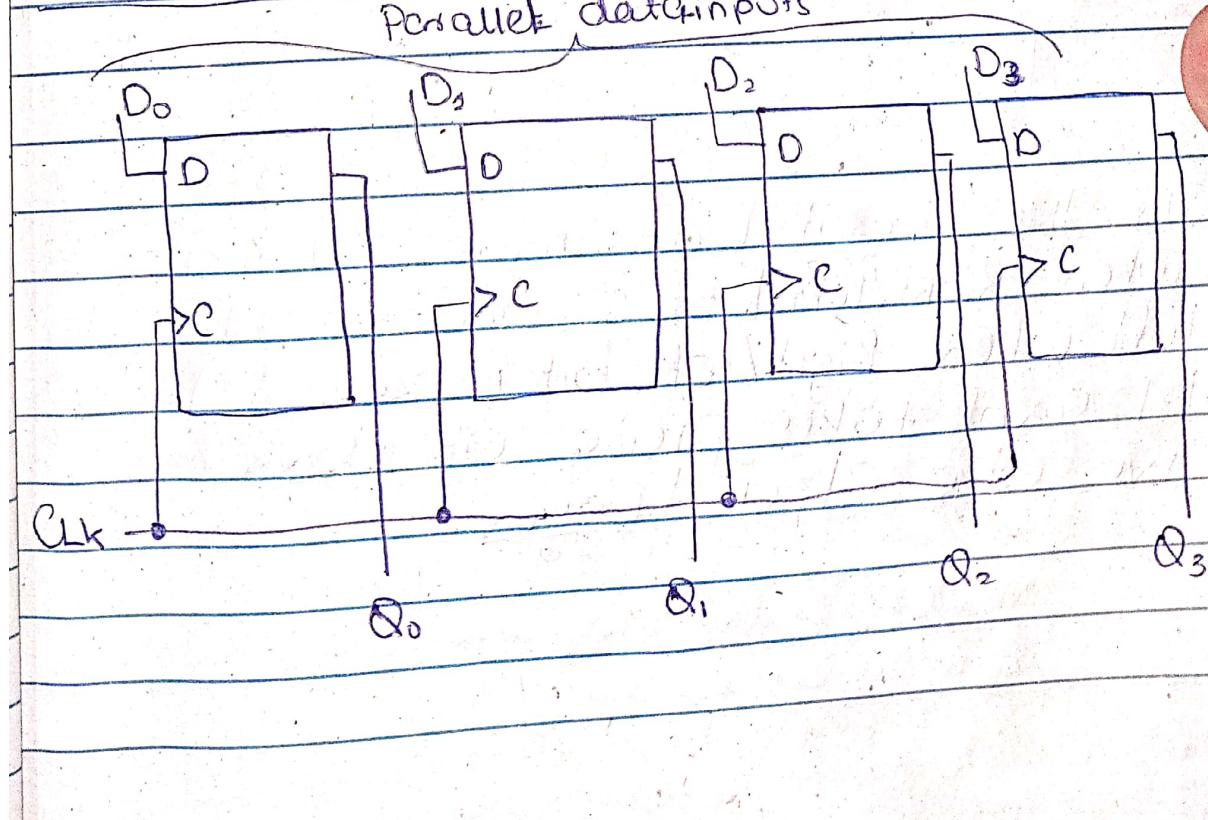


Clk	1	2	3	4	5	6
Shift/Load	1					
Data Out (Q_3)	0	1	0	1	1	1

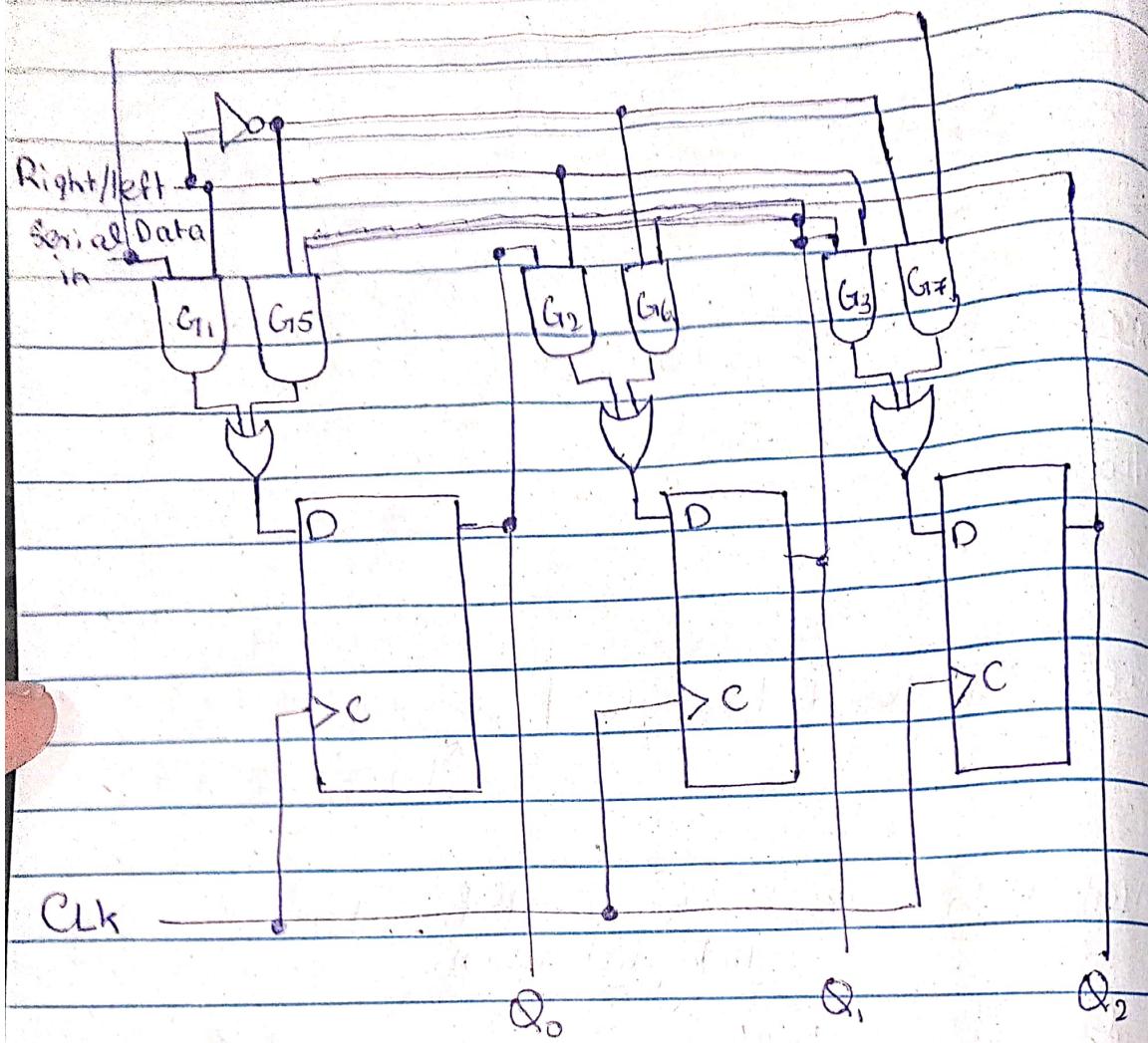
^ Last Data bit.

Parallel In / Parallel Out Shift Registers:-

Parallel data inputs

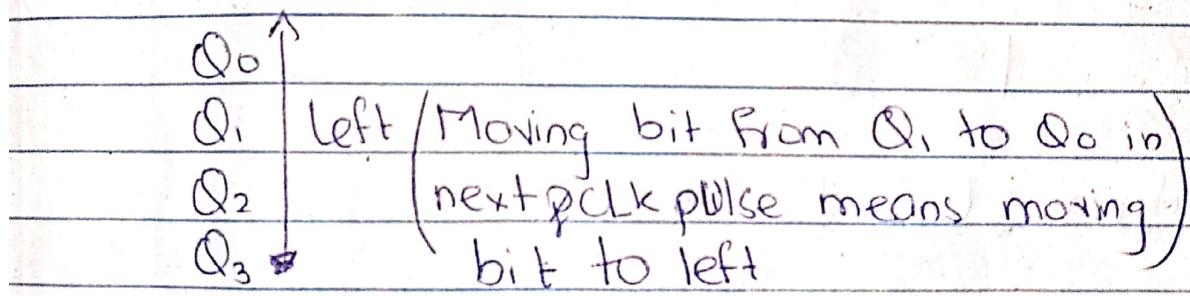
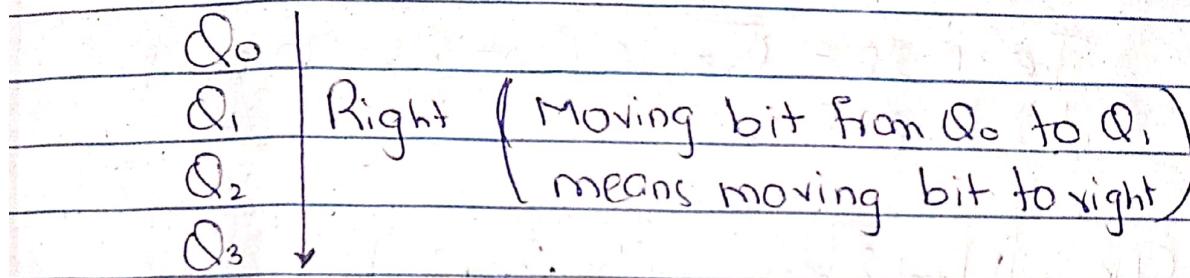
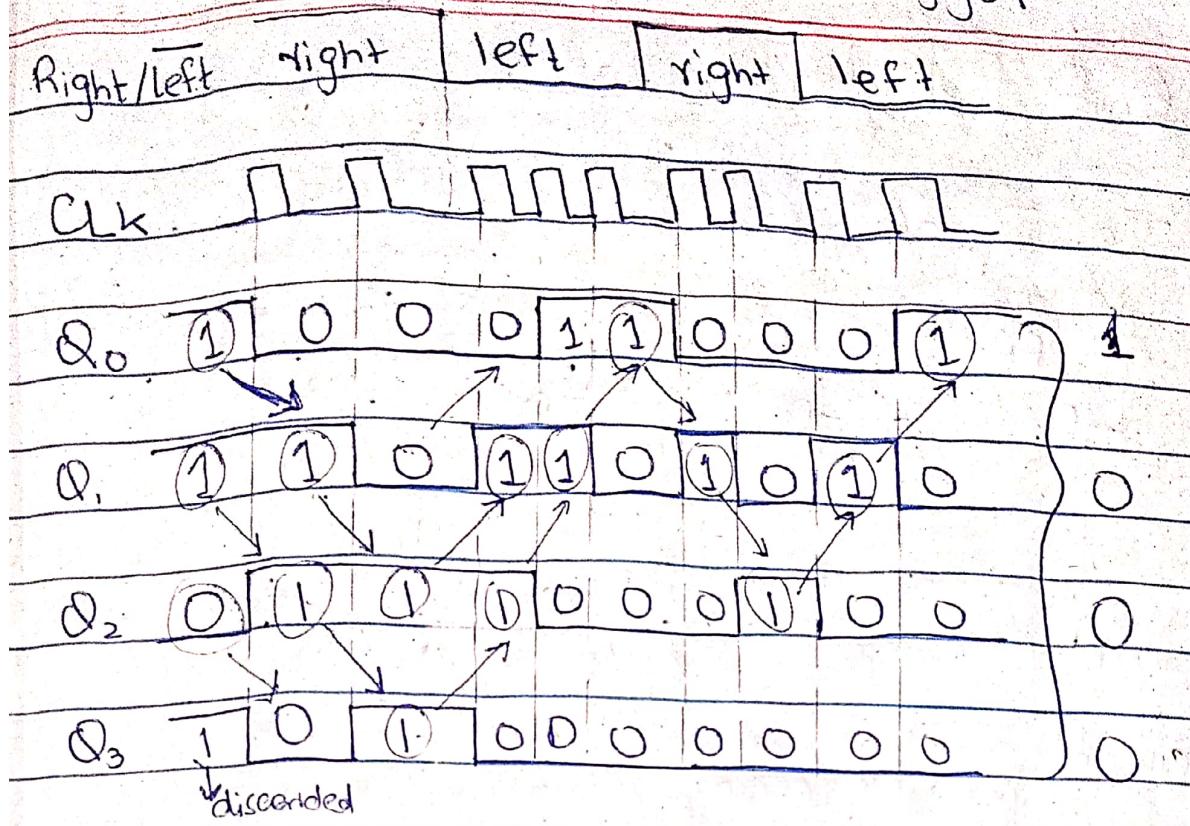


Bidirectional Shift Register and Shift Register Counter



In this Circuit Data moves to Right when Right/left bit is 1 And moves towards left when Right/left bit is zero. Data Movement takes place at Clock every +ve edge Clock trigger.

Changes occur at the clock trigger



when right/left is 1 more bits in order

$Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$ but each

transfer must be made in

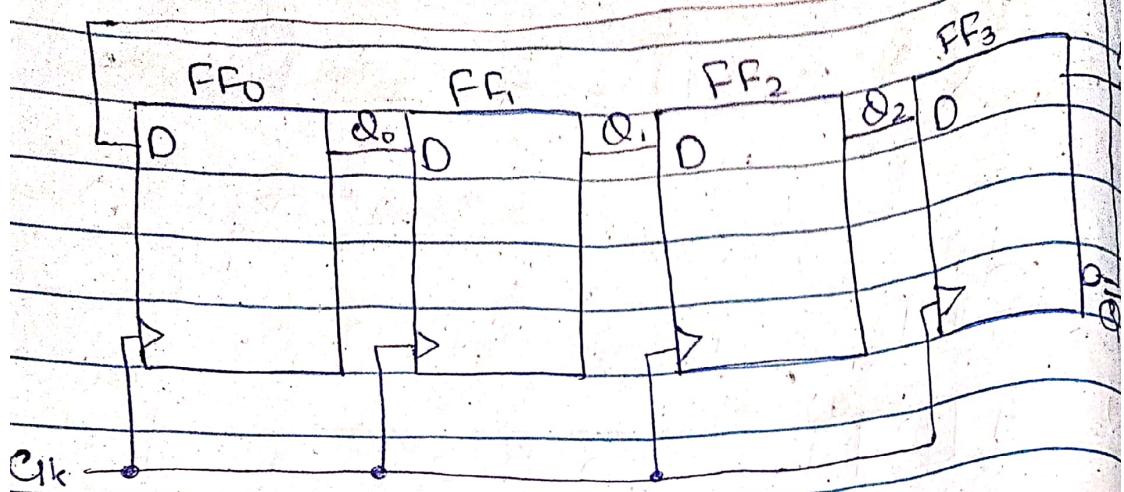
separate clock pulse

for right/left = 0 vice versa.

$Q_0 \leftarrow Q_1 \leftarrow Q_2 \leftarrow Q_3$

Shift Register Counters

The Johnson Counter:- (4-stage)

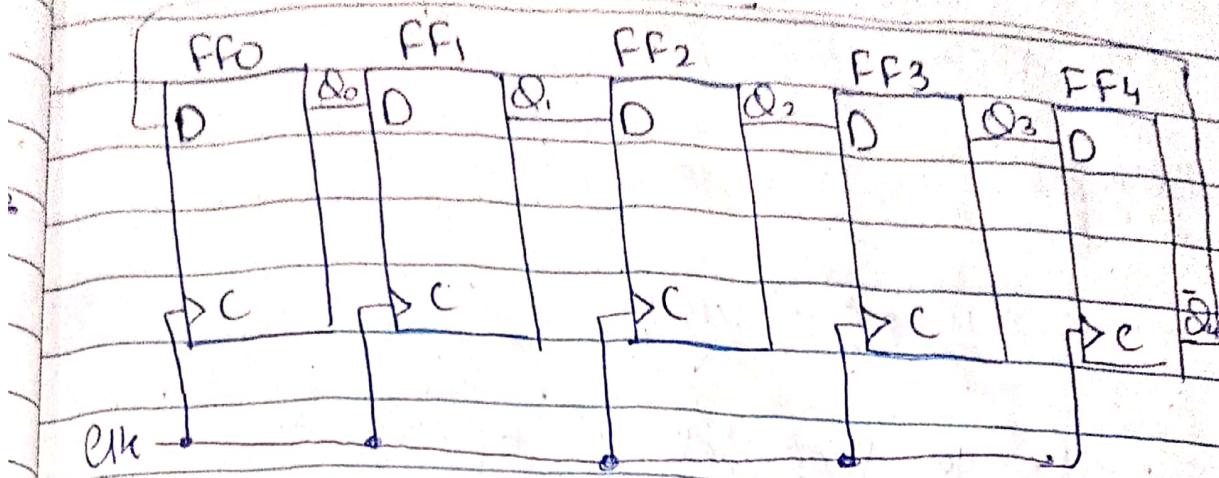


The output \bar{Q}_3 is sent as an input to Flip-Flop 0.

Clk	1	2	3	4	5	6	7	8
Q_0	0	1	1			0		
Q_1	0	0	1					
Q_2	0	0						
Q_3	0	0	1					

values of Q_3 are inverted and sent to Q_1 at every clock pulse

5 Stage Johnson Counter:-



Every output from Q_4 will be inverted and sent as an input to FlipFlop 0.

All the bits at every clock pulse trigger will move to right ($Q_0 \rightarrow Q_1 \rightarrow Q_2 \rightarrow Q_3$)

After all cycles initial state will be formed again.

Ring Counter:-

In Ring Counter again the bits will shift down at every clock pulse trig.

The output inverted bit will be reverted back to first flip flop input and after all cycles the output bits will get back to their initial bit form.

Time-Delay Applications:-

To record time delay

Per clock trig time-Delay \times N.o of flip-flops.

$$1\text{us} \times 8 = 8\text{ us}$$

To change time-delay (i.e 1us) we
will change clock-cycle frequency.

also. by increasing number of ffs.