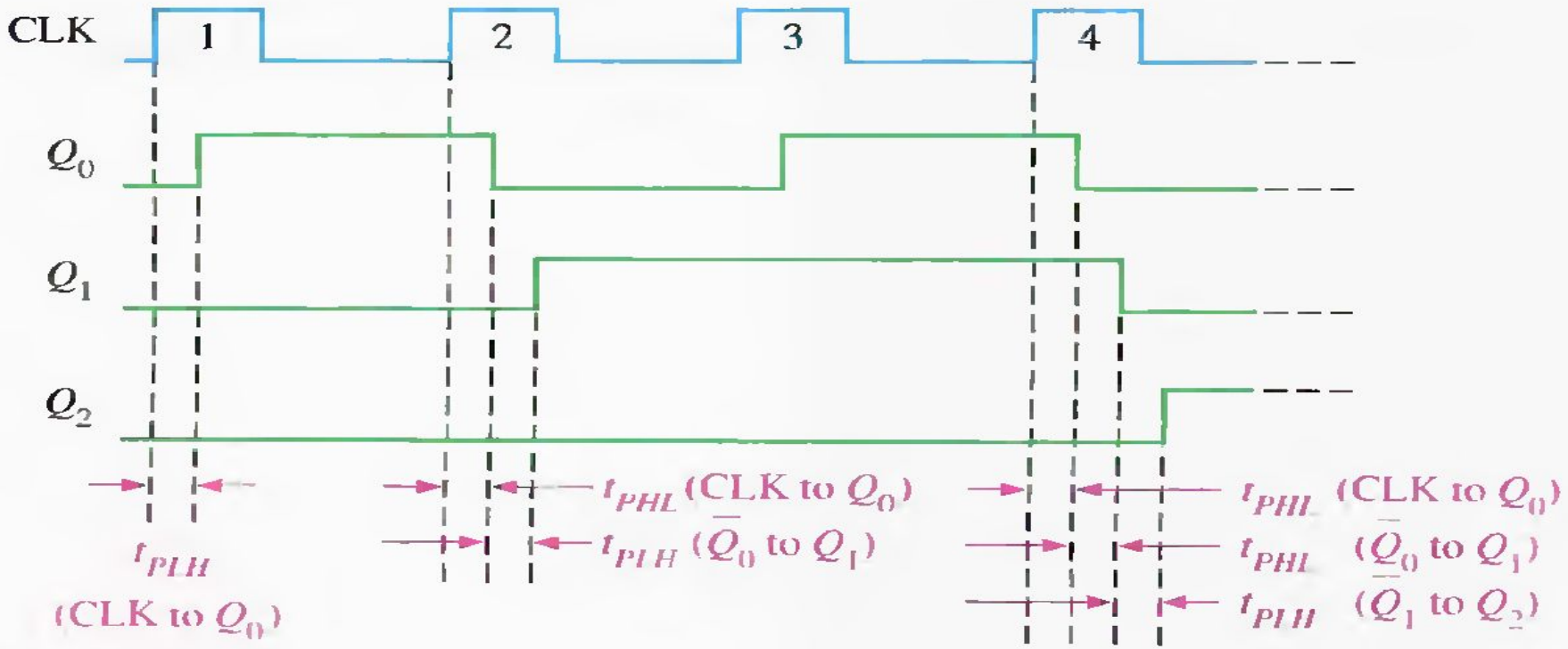
Chapter No:9
Counters

Outlines

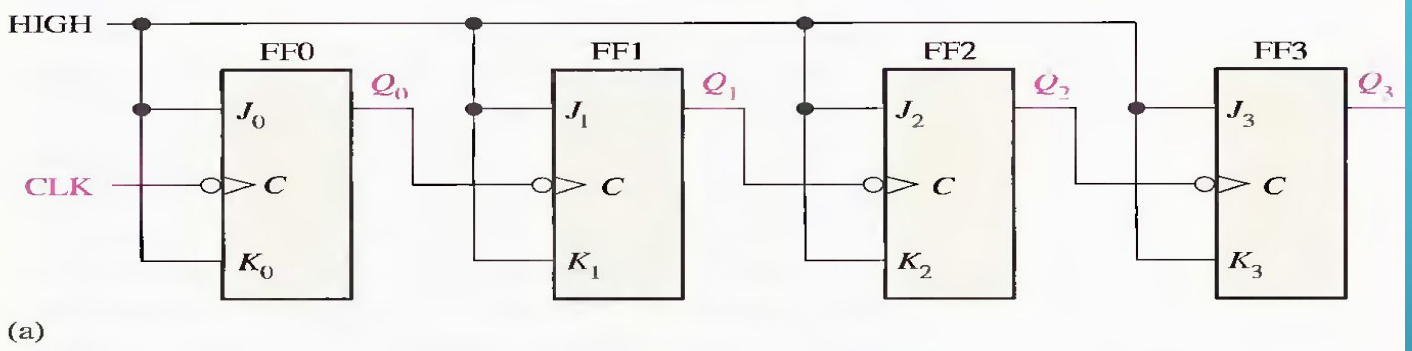
Asynchronous Counters
Synchronous Counters
Up/Down Synchronous Counters
Design of Synchronous Counters
Cascaded Counters
Counter Decoding
Counter Applications

Propagation Delay

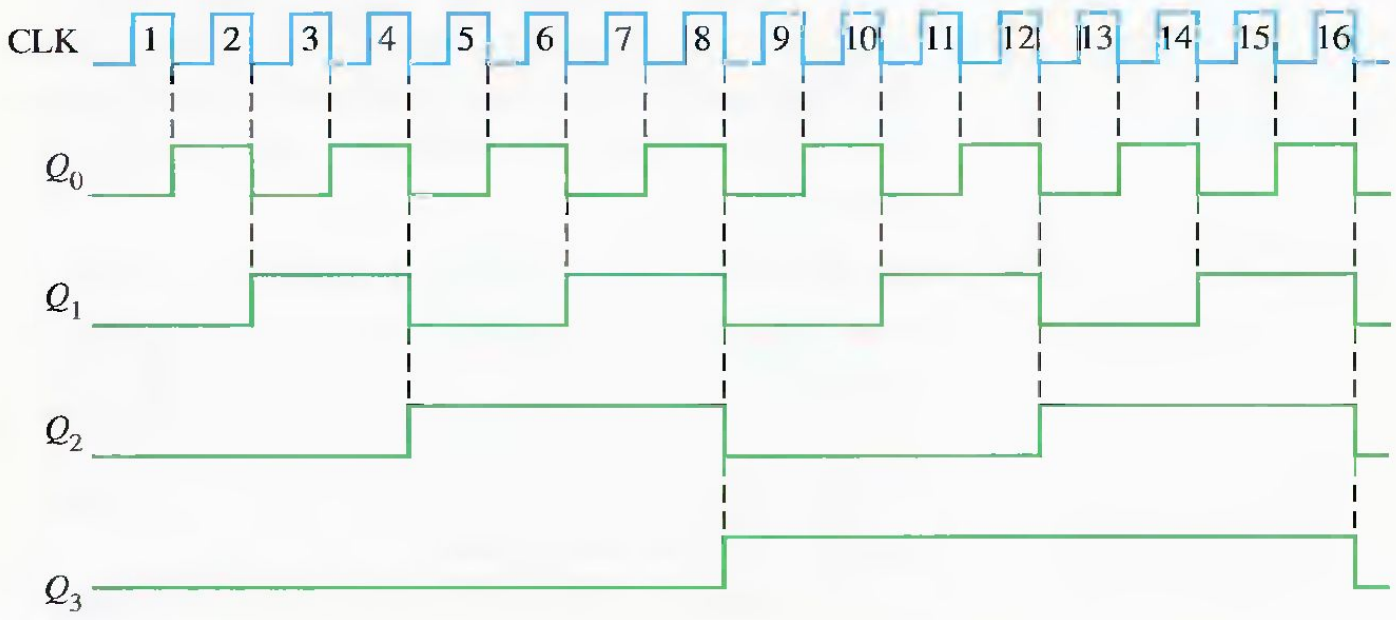
Propagation Delay Asynchronous counters are commonly referred to as **ripple counters** for the following reason: The effect of the input clock pulse is first "felt" by FF0. This effect cannot get to FF1 immediately because of the propagation delay through FF0. Then there is the propagation delay through FF1 before FF2 can be triggered. Thus, the effect of an input clock pulse "ripples" through the counter. taking some time, due to propagation delays, to reach the last flip-flop.



A 4-bit asynchronous binary counter is shown in Figure 8–5(a). Each flip-flop is negative edge-triggered and has a propagation delay for 10 nanoseconds (ns). Develop a timing diagram showing the Q output of each flip-flop, and determine the total propagation delay time from the triggering edge of a clock pulse until a corresponding change can occur in the state of Q_3. Also determine the maximum clock frequency at which the counter can be operated.



(a)



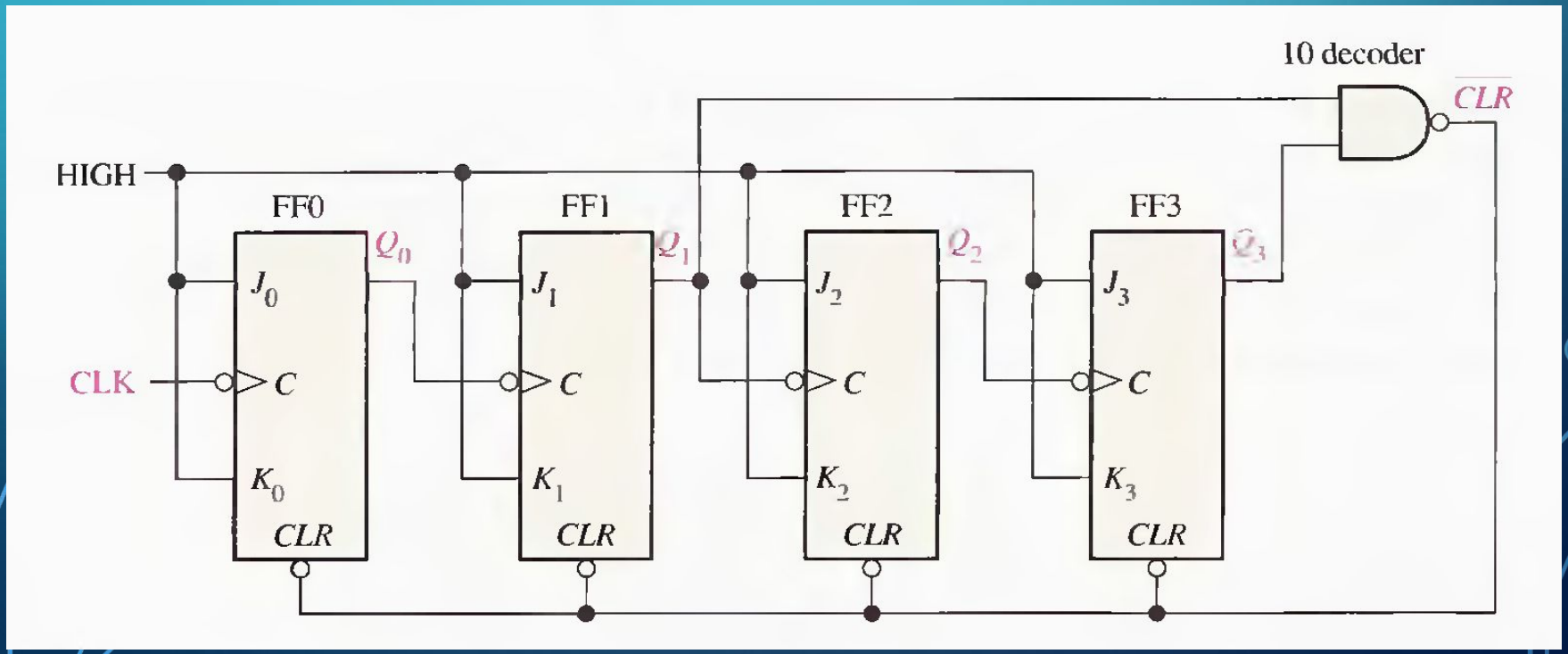
$$t_{p(tot)} = 4 \times 10 \text{ ns} = \mathbf{40 \text{ ns}}$$

$$f_{max} = \frac{1}{t_{p(tot)}} = \frac{1}{40 \text{ ns}} = \mathbf{25 \text{ MHz}}$$

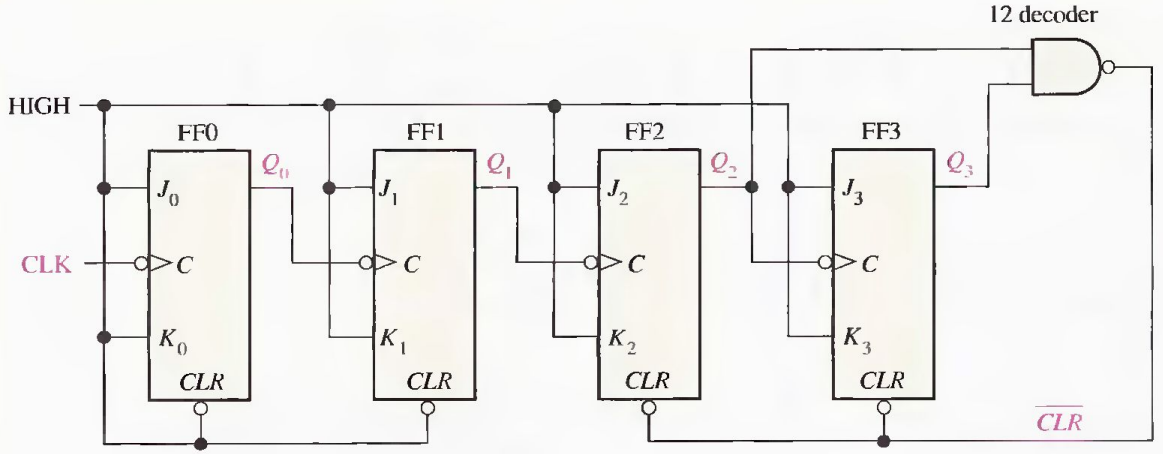
Asynchronous Decade Counters

The **modulus** of a counter is the number of unique states through which the counter will sequence. The maximum possible number of states (maximum modulus) of a counter is 2^n, where n is the number of flip-flops in the counter. Counters can be designed to have a number of states in their sequence that is less than the maximum of 2^n. This type of sequence is called a *truncated sequence*.

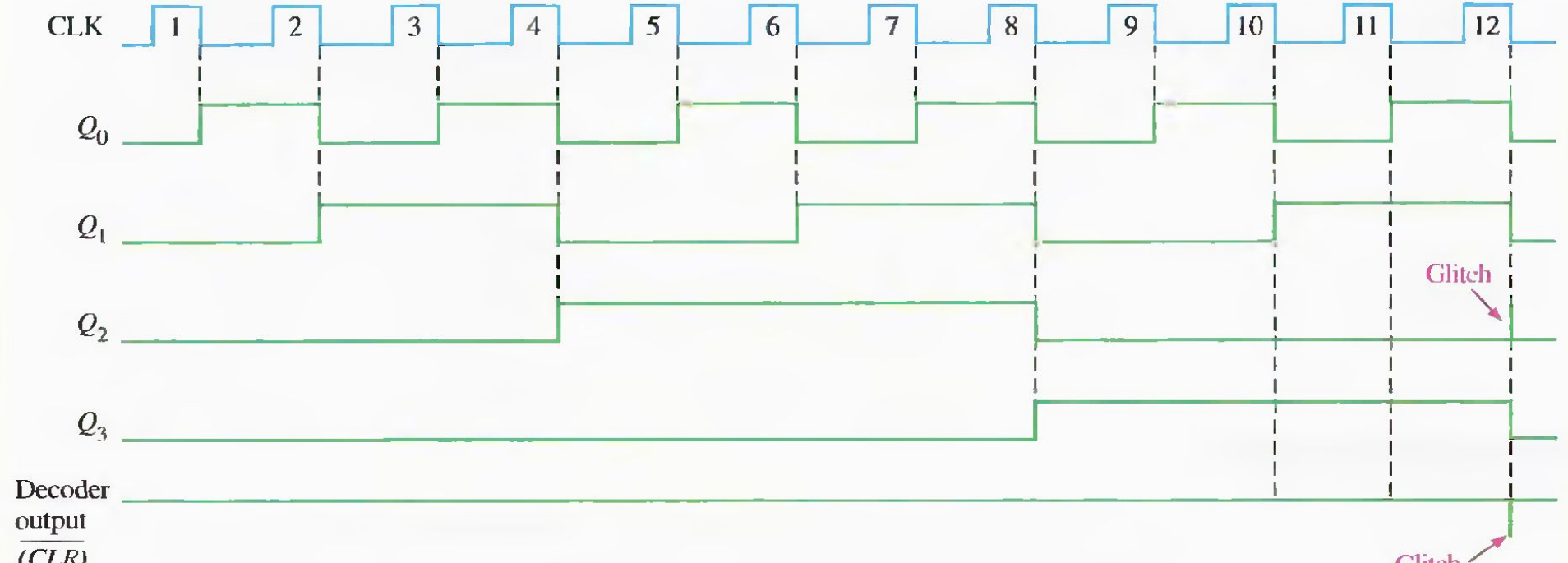
One common modulus for counters with truncated sequences is ten (called MOD10). Counters with ten states in their sequence are called **decade** counters.



Show how an asynchronous counter can be implemented having a modulus of twelve with a straight binary sequence from 0000 through 1011.

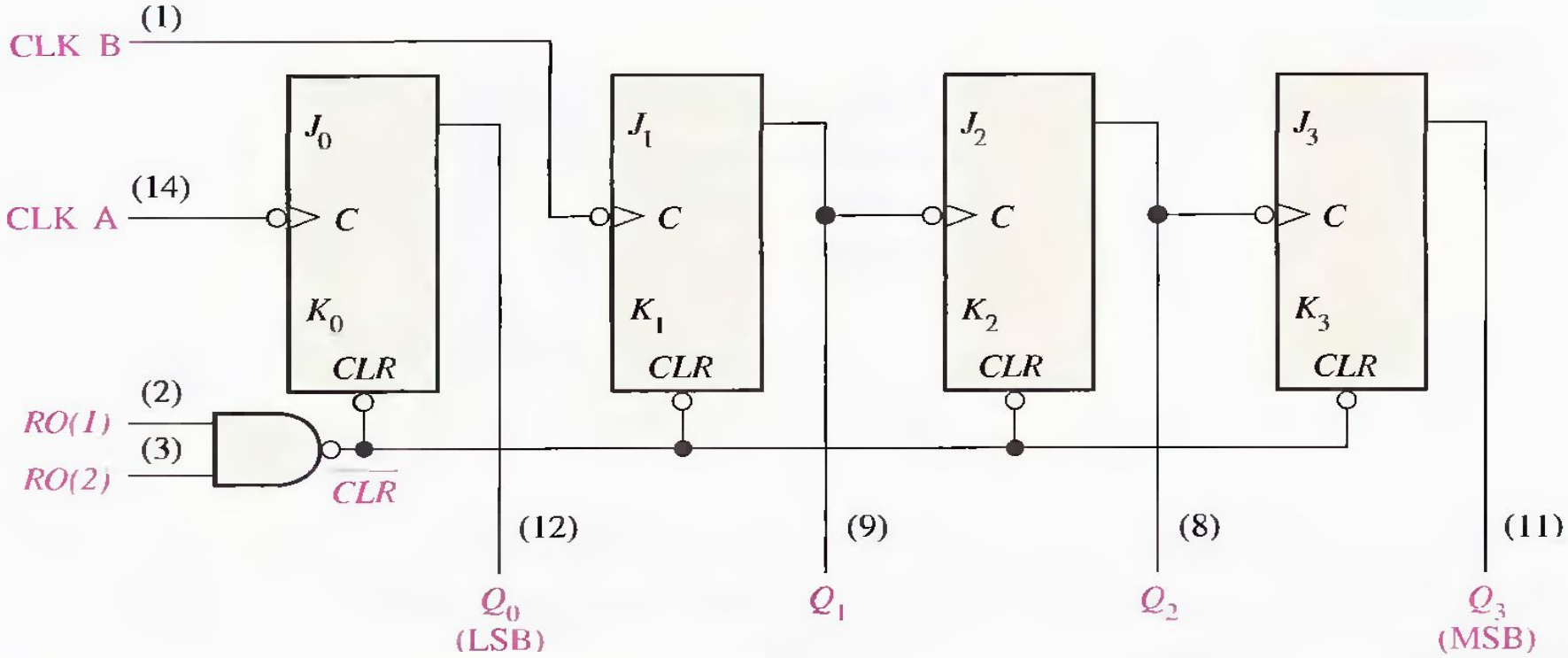


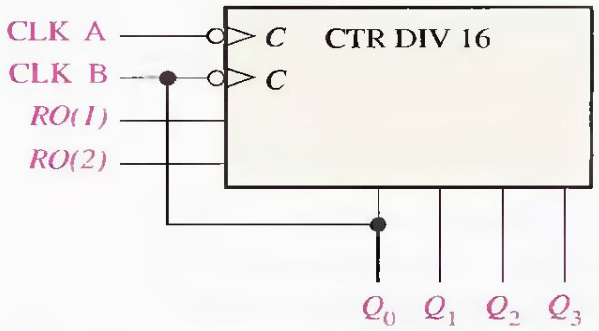
Q_3	Q_2	Q_1	Q_0	
0	0	0	0	← Recycles
.	.	.	.	
.	.	.	.	
.	.	.	.	
1	0	1	1	← Recycles
1	1	0	0	← Normal next state



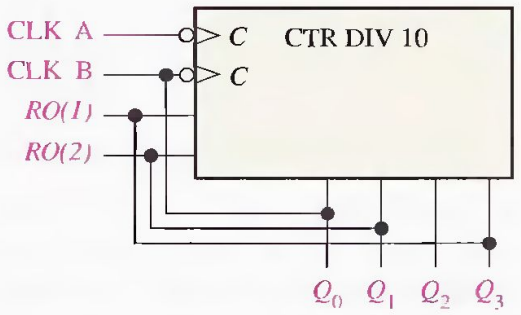
THE 74LS93 4-BIT ASYNCHRONOUS BINARY COUNTER

The 74LS93 4-bit asynchronous binary counter logic diagram. (Pin numbers are in parentheses, and all *J* and *K* inputs are internally connected HIGH.)



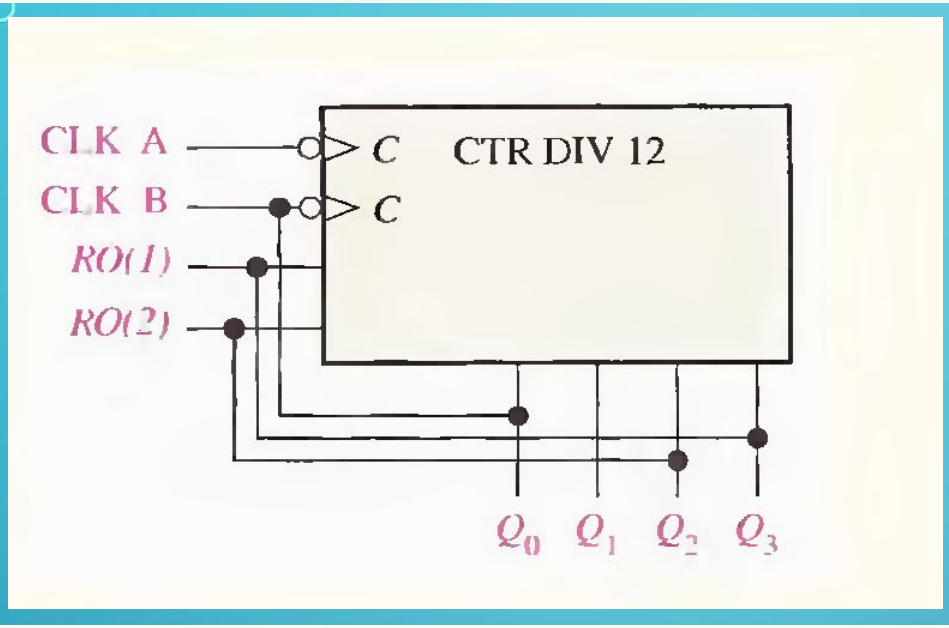


(a) 74LS93 connected as a modulus-16 counter



(b) 74LS93 connected as a decade counter

Show how the 74LS93 can be used as a modulus-12 counter.



Show how the 74LS93 can be connected as a modulus-13 counter.