Digital Logic Design (EL-227)

LABORATORY MANUAL

Spring-2021

LAB 07
Binary Decoder

NATIONAL UNIVERSITY OF COMPUTER AND EMERGING SCIENCES (NUCES), KARACHI

Date: 05/04/2021

Lab Session 07: Binary Decoder

OBJECTIVES:

After completing this lab, you would be able to know

- To study the basic operation and design of the decoder circuits
- Explain the working principle of 3-8 line decoder & BCD to Seven Segment decoder
- Understand the usage of Seven Segment Display
- To learn the concept of enabling a signal (active-low and active-high enable)

APPARATUS:

- Logics Trainer, Logics works

COMPONENTS:

- 74LS138 (3-8 line decoder)
- 74LS47 (BCD to Seven Segment Decoder)
- 74LS08, 74LS32, 74LS04, 74LS00, 74LS02

INTRODUCTION:

Decoder is a multiple-input, multiple-output logic circuit that converts coded inputs into coded output coded outputs. The basic function of decoder is to detect the presence of a specified combination of bits (code) at its input and indicate the presence of that code by a specified output. Various kinds of decoding include n-to-2^n decoding & binary-coded decimal decoding. Decoder has Enable inputs which must be on for the decoder to function. A decoder is a combinational circuit that decodes the encoded inputs. A binary decoder has n inputs and a maximum of 2^n outputs. An n-bit binary number provides 2^n minterms or maxterms. The decoder that produces 2^n minterms as its outputs is said to be a decoder with active high outputs, whereas, the decoder that produces 2^n maxterms as its outputs is said to be a decoder with active low outputs. Let us take n=2 as an example, so that we obtain the 2-to-4 line decoder with active high outputs. Figure 7-1 shows the block diagram of 2x4 decoder.

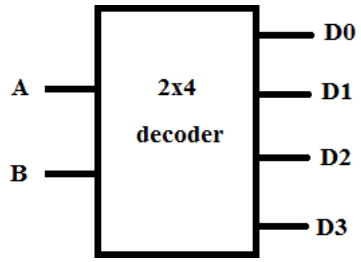


Figure 1 2x4 decoder Block Diagram

Inputs		Outputs			
A	**B**	**D0**	**D1**	**D2**	**D3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Boolean Expressions of Outputs:

D0: (AB)’

D1: A’B

D2: AB’

D3: AB

The Boolean expressions show that four outputs of 2x4 decoder show four min-terms of two binary variables A and **B**

Circuit diagram for 2x4 decoder with active high outputs:

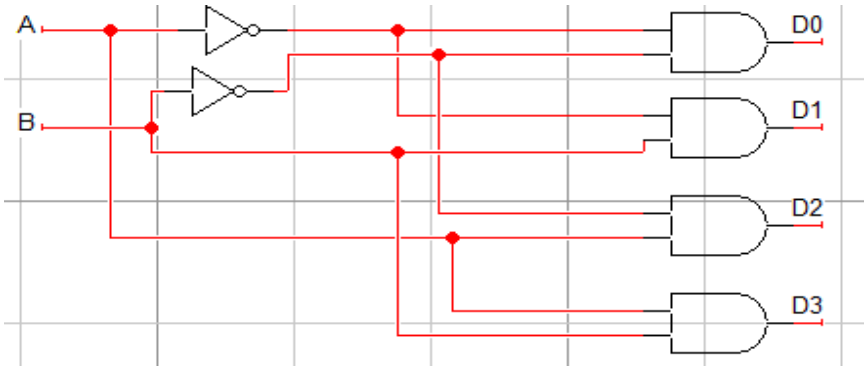


Figure 2 2x4 decoder schematic

Circuit Diagram For 2x4 Decoder With Active High Outputs And Active High Enable:

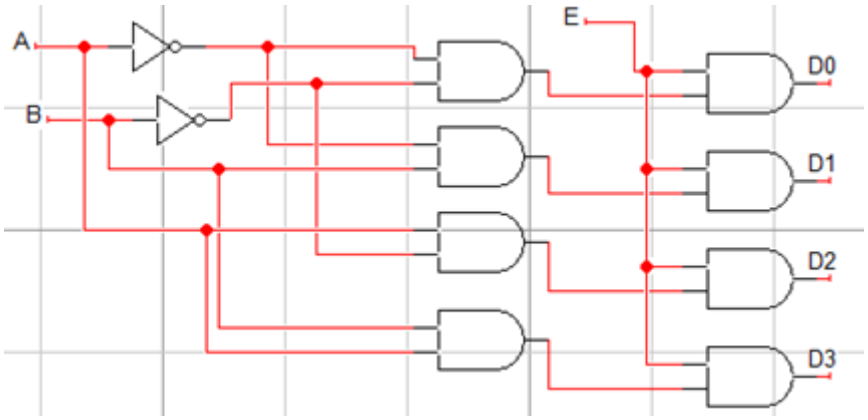


Figure 3 2x4 decoder schematic with enabling

3-LINE TO 8-LINE DECODER

The 74LS137 is a three-line to eight-line decoder/demultiplexer with latches on the three address inputs. When the latch-enable input (GL\) is low, the 74LS137 acts as a decoder/demultiplexer. When GL\ goes from low to high, the address present at the select inputs (A, B, and C) is stored in the latches. Further address changes are ignored as long as GL\ remains high. The output enable controls, G1 and G\2, control the state of the outputs independently of the select or latch-enable inputs. All of the outputs are high unless G1 is high and G\2 is low. The 74LS137 is ideally suited for implementing glitch-free decoders in strobed (stored-address) applications in bus-oriented systems.

WORKING:

Apply the inputs to the input slot as shown below and check outputs on the output slot (J22) and verify the truth table for different sets of input values.

Figure 5-1: Slots explanation for 3 to 8 line decoder

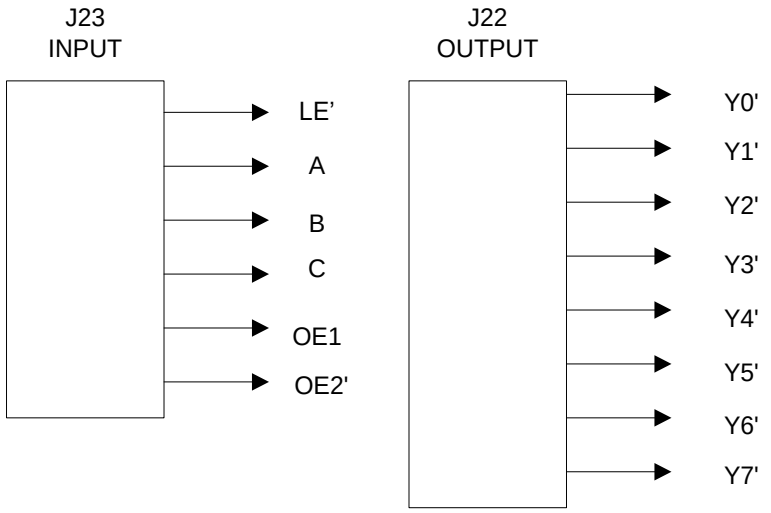


Table 5-1: Truth table

INPUTS						OUTPUTS							
ENABLE			SELECT										
G2A'	G1	G2B'	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	H	H	H	H	H	H	H	H
X	L	X	X	X	X	H	H	H	H	H	H	H	H
L	H	L	L	L	L	L	H	H	H	H	H	H	H
L	H	L	L	L	H	H	L	H	H	H	H	H	H
L	H	L	L	H	L	H	H	L	H	H	H	H	H
L	H	L	L	H	H	H	H	H	L	H	H	H	H
L	H	L	H	L	L	H	H	H	H	L	H	H	H
L	H	L	H	L	H	H	H	H	H	H	L	H	H
L	H	L	H	H	L	H	H	H	H	H	H	L	H
L	H	L	H	H	H	H	H	H	H	H	H	H	L

Implementation of 3-8 line Decoder using IC 74LS138

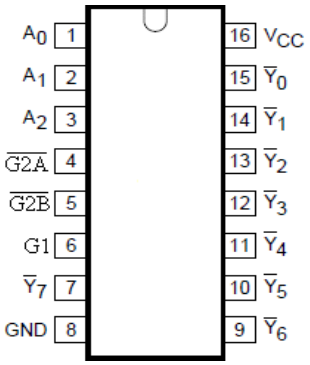


Fig 4. Pin Configuration

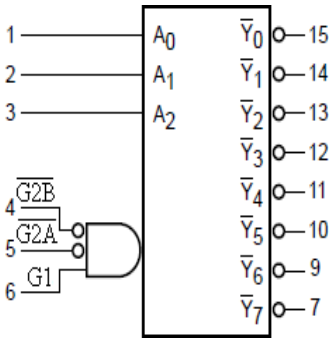


Fig 5 . Logic Symbol

This decoder decodes one of eight lines depending on the three binary select inputs and three enable pins. It is an octal decoder capable of decoding eight possible three-bit combinations to eight separate active-Low outputs.

A0–A2	InputBits
G2A',G2B'	Enable (Active LOW) Inputs
G1	Enable (Active HIGH) Inputs
Y0'-Y7'	Active LOW Outputs

SEVEN SEGMENT

A **seven-segment display** (**SSD**), or **seven-segment indicator**, is a form of electronic display device for displaying decimal numerals that is an alternative to the more complex dot-matrix displays.Typically 7-segment displays consist of seven individual colored LED's (called the segments), within one single display package. In order to produce the required numbers or HEX characters from 0 to 9 and A to F respectively, on the display the correct combination of LED segments needs to be illuminated. Figure5-2a shows seven segment indicator, i.e. seven LEDs labeled a through g. By forward-biasing different LEDs, we can display the digits 0 through 9(see figure 5-2b). For instance, to display 0 we need to light up segments a,b,c,d,e and f. To light up 5 we need segments a,c,d,f and g.

Seven segment indicators may be the common-anode type where all anodes are connected together (figure 5-3a) or the common-cathode type where all cathodes are connected together (figure 5-3b).

The 7447 chip is used to drive 7 segment display. You must use the 7447 with a common anode 7-segment display. The input to the 7447 is a binary number DCBA. The inputs DCBA often come from a binary counter.

The display is only sensible if the binary number is between DCBA=0000 (0) and DCBA=1001 (9); this is called Binary Coded Decimal or BCD for short. If the number is larger than 9 you get a strange output on the display. The inputs $\overline{BI}/\overline{RBO}$, $\overline{RBI}$ and $\overline{LT}$ are usually connected to 5v.

Figure 5-2: Seven-segment indicator

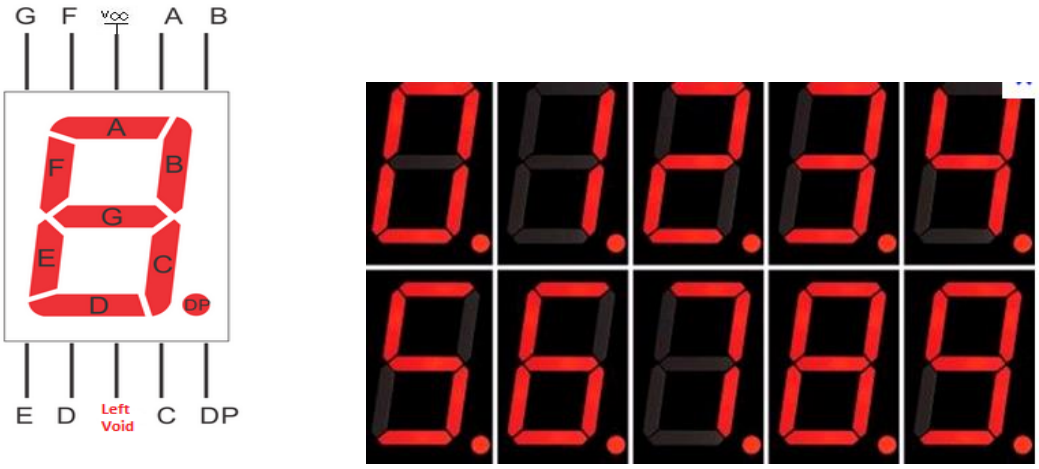


Figure 5-3: Cathode Types

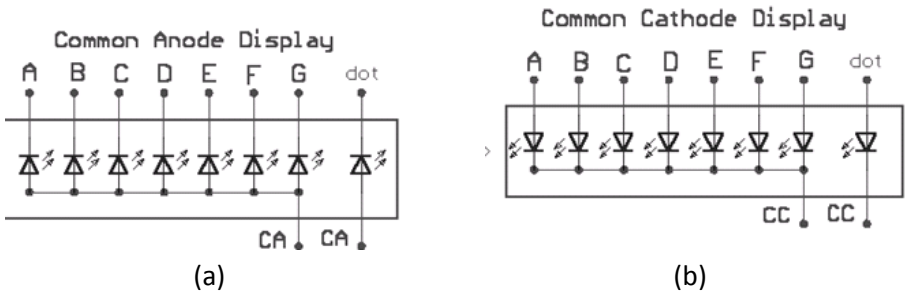


Figure 5-4: Connection Display in Logic Works5

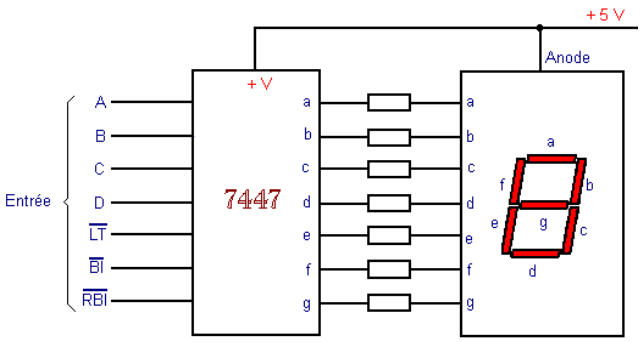
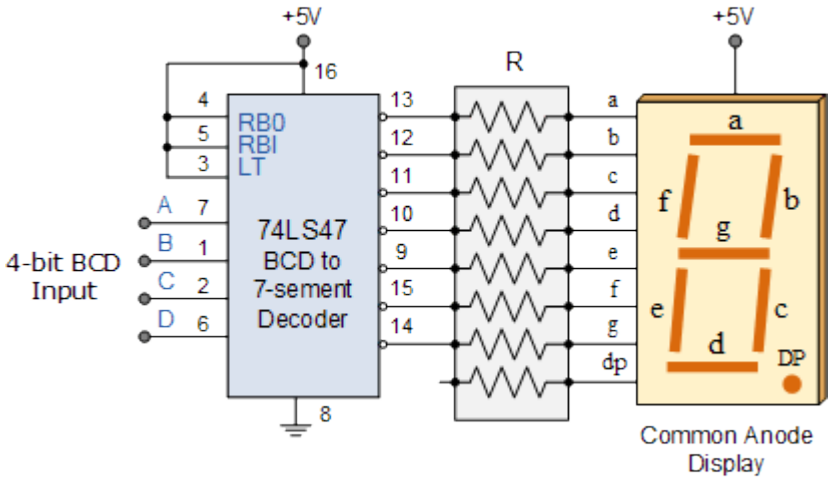


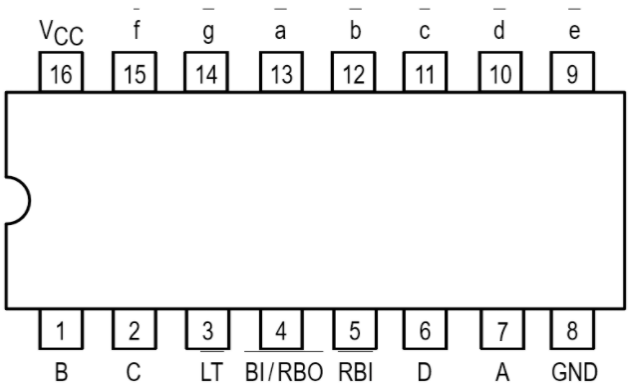
Figure 5-5: Connection Display on BreadBoard



WORKING

Apply the inputs to the input as shown below and check output on seven segment indicator and verify the truth table for different sets of input values.

Figure 5-6: Slots explanation for 7-Segment Display



A0–A3	BCD-Inputs
RBI’	Ripple Blanking Input (Active LOW)
LT’	Lamp Test Input (Active LOW)
BI'/RBO'	Blanking Input or Ripple Blanking Output (Active LOW)
a'– g'	Active LOW Outputs

Table 5-1: Truth table

INPUTS							OUTPUTS						
D	**C**	**B**	**A**	**LT'**	**RB1'**	**RB0/B1'**	**a**	**b**	**c**	**d**	**e**	**f**	**g**
0	0	0	0	1	1	1	0	0	0	0	0	0	1
0	0	0	1	1	1	1	1	0	0	1	1	1	1
0	0	1	0	1	1	1	0	0	1	0	0	1	0
0	0	1	1	1	1	1	0	0	0	0	1	1	0
0	1	0	0	1	1	1	1	0	0	1	1	0	0
0	1	0	1	1	1	1	0	1	0	0	1	0	0
0	1	1	0	1	1	1	0	1	0	0	0	0	0
0	1	1	1	1	1	1	0	0	0	1	1	1	1
1	0	0	0	1	1	1	0	0	0	0	0	0	0
1	0	0	1	1	1	1	0	0	0	1	1	0	0

LAB TASKS

Lab Task#1:

Design and implement a 2-to-4 line decoder with active low outputs along with active low enable input E. When E is low, the decoder will operate normally, when E is high, all outputs should be high regardless of the inputs.

a) **Write truth table**

b) **Find minimal SOP and POS expressions for the 2x4 decoder outputs using K-map. Draw separate K-map for each output in the space given below**

Lab Task #2:

Implementation of 3-8 line Decoder using IC 74LS138 Observations and draw the circuit diagram:

3-8 line Decoder

INPUTS						OUTPUTS							
Enable			Select										
G_1	G_{2A}'	G_{2B}'	A_2	A_1	A_0	Y_0'	Y_1'	Y_2'	Y_3'	Y_4'	Y_5'	Y_6'	Y_7'

Lab Task #3:

Implementation of BCD to Seven Segment Decoder using IC 74LS47 Observations:

BCD to Seven Segment Decoder

LT'	RBI'	BI' / RBO,	INPUTS				OUTPUTS						
			A_3	A_2	A_1	A_0	a'	b'	c'	d'	e'	f'	g'