
Department of Electrical and Computer Engineering

ENEL 453: Digital System Design

Fall 2021

# Lab 4: PWM DAC BUZZER

## 1. Overview

In this lab project, you will interface your distance measurer from Lab 3 to a buzzer, such that the measurer will measure a distance to an object (your hand, for example) and the buzzer will produce a different sound depending on the measured distance. The buzzer must be driven by a PWM output from the FPGA. Under user control, the distance measurement will modulate the frequency of the buzzer, all within the audible range.

All asynchronous inputs must be synchronized. The design must meet a minimum timing of 50 MHz.

This lab is worth 45% of your final grade and is broken up as:

- Pre-lab: 2 mark
- In-lab demonstration in your second lab period: 43 marks.

See the grading rubric on the last page for the deadlines and late penalties.

## 2. Demonstrations

The buzzer will be driven directly from a PWM output from the FPGA. Under frequency modulation, the distance of the hand from the sensor will make the sound higher or lower in pitch. The buzzer must be audible to the instructors.

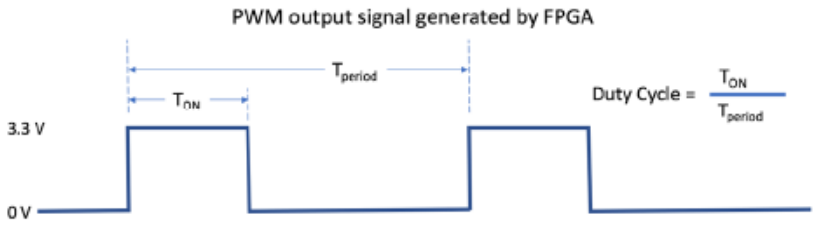
## 3. Development approach

You will have to exercise good engineering judgement and good engineering practice to successfully complete this design challenge. Recommendations are:

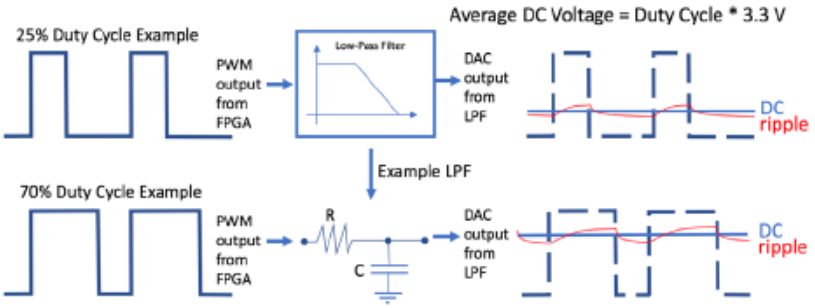
1. Develop **incrementally** and **iteratively**.
    a. Start with a working design (e.g. your distance measurer),
    b. Add some additional functionality (don't try to do too much in one iteration),
    c. Test that it works (and if not, you generally know where the error is localized),
    d. Repeat the process to add additional functionality, until the design is complete.
2. Don't be hesitant to redesign a part to make it better for future development.
3. Use testbenches and simulation to complete **unit testing** of the components you want to add.
4. Use testbenches and simulation to complete **system-level testing** of the integrated system.
5. Complete periodic **synthesis checks** to ensure your code makes correct hardware and double-check the RTL schematic, as you incrementally develop your system.
6. Periodically download to your board and check the incremental functionality in the real system.

# 4. PWM DAC

A brief description of the PWM DAC operation is given below.



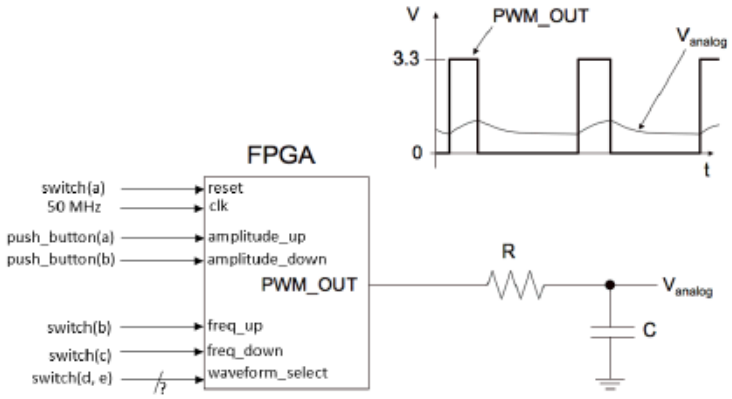

The FPGA output is a square wave with a variable ON time, or $T_{ON}$. The period of the square wave is $T_{period}$. The ratio of $T_{ON}$/ $T_{period}$ is the Duty Cycle, and this is the percentage of the period that the square wave is high.




In the two examples above, the PWM output from the FPGA is fed into a Low-Pass Filter (LPF) and the LPF can be as simple as an RC filter, as shown in the second example. The output of the LPF is a smoothed signal. This signal has an average DC voltage, which is the 3.3 V supply voltage of the FPGA I/O, scaled by the Duty Cycle. For example, if the PWM waveform had a Duty Cycle of 25%, then the average DC voltage would be:

25% * 3.3 V = 0.825 V.

However, the LPF output signal is not typically a smooth DC value. There is a voltage ripple, as indicated by the red line. The voltage ripple would be the actual voltage seen at the output of the LPF and it depends on the characteristics of the LPF, the PWM period, and the PWM duty cycle. A more detailed illustration is shown below, with example input and outputs to the FPGA.

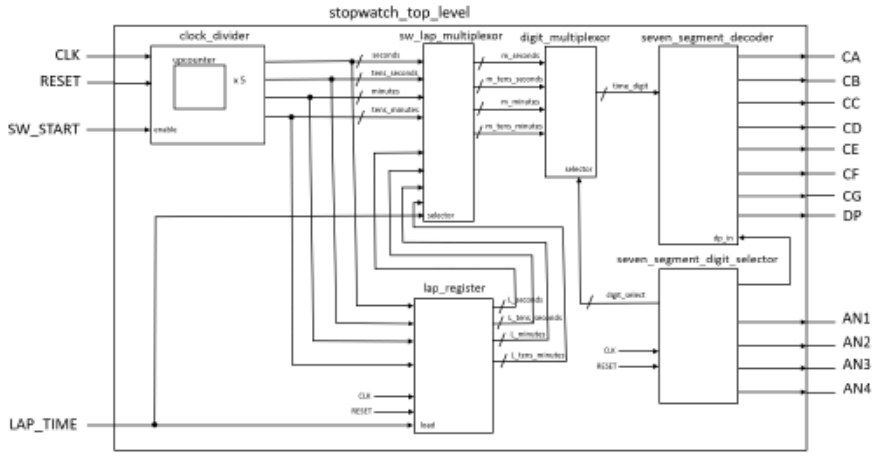



# 5. PRE-LAB ASSIGNMENT

The individual pre-lab assignment is a top-level block diagram of your system. To help you get started, we have provided you with an example of a block diagram from last year's course, to show you what a block diagram looks like. This example block diagram for a stopwatch is not meant to give you guidance for completing your design, as the design challenge is completely different for this year.

Your block diagram should show the general approach you might take to break down the design problem into smaller blocks. Your block diagram should also show the input and output signals to your design, and the interconnections between the blocks. You do not have to follow the design approach described in your block diagram, but it should be a useful reference or starting point for you.

The block diagram should be neat and easily readable. It can be hand-drawn or computer generated.



# 6. Design Record Document

Within 24 hours of completing your demonstration, upload to D2L the following (**for each group**):

1. Your VHDL design files for the complete design as demonstrated.
2. Your constraints files (.sdc and .qsf).
3. Your top-level VHDL testbench.
4. Your Design Record document with the following:

   4.1 Your name and your partner's name on the first page of your document.

   4.2 A screenshot of your top-level RTL schematic.

   4.3 Screenshot of your Timing Report, showing the maximum clock frequency of your design.

   4.4 Screenshots of the simulation waveforms showing the correct operation of the top-level design.

   4.5 Note that no write-up is required.

# 7. GRADING

Your Lab 4 project demo will be assessed in the last 15 minutes of the lab period, your TA will inform you of your timeslot.

You must show the following to the TA to obtain your credit for the lab, and the TA may request further demonstration than listed below.

All team members must be able to explain their design and answer questions about any part of the lab project in order to receive credit for the project.

| Description | Marks |
|---|---|
| Pre-lab assignment | 2 |
| In-lab demonstration:<br><br>1. Distance controlled buzzer modulating sound frequency as specified in this document.<br><br>The above functionality must be demonstrated to receive credit for completing the lab. Students **must be able to explain their design and answer questions to receive credit** for completing the lab.<br><br>The maximum frequency in the Timing Summary must be **at least 50 MHz**. The design must be synchronous:<br>• all asynchronous inputs to the system **must be synchronized** (i.e. pushbuttons and switches),<br>• only one clock edge must be used, i.e. only **rising_edge(clk)**.<br><br>Late demonstrations can be held by uploading design, simulation, and implementation videos after the deadline until Monday Dec. 6 at 9:30 am, for a reduction of 10 marks. Further delays will result in 0 marks for the lab.<br><br>B01 demonstration: Thursday Nov. 25<br>B02 demonstration: Thursday Dec. 2<br><br>You must successfully demonstrate **the buzzer, as described above, to be eligible to pass the course**. | 43 |
| To receive the above marks and credit for the lab, **all the files specified in Section 6 must be uploaded by each group to the Dropbox in D2L within 24 hours after you demonstrate**. Do not worry about special formatting or documenting the screenshots, just paste them into a Word document, PDF it, and upload the PDF. | |