

## ENEL 453 LAB 4 – SUBMISSION

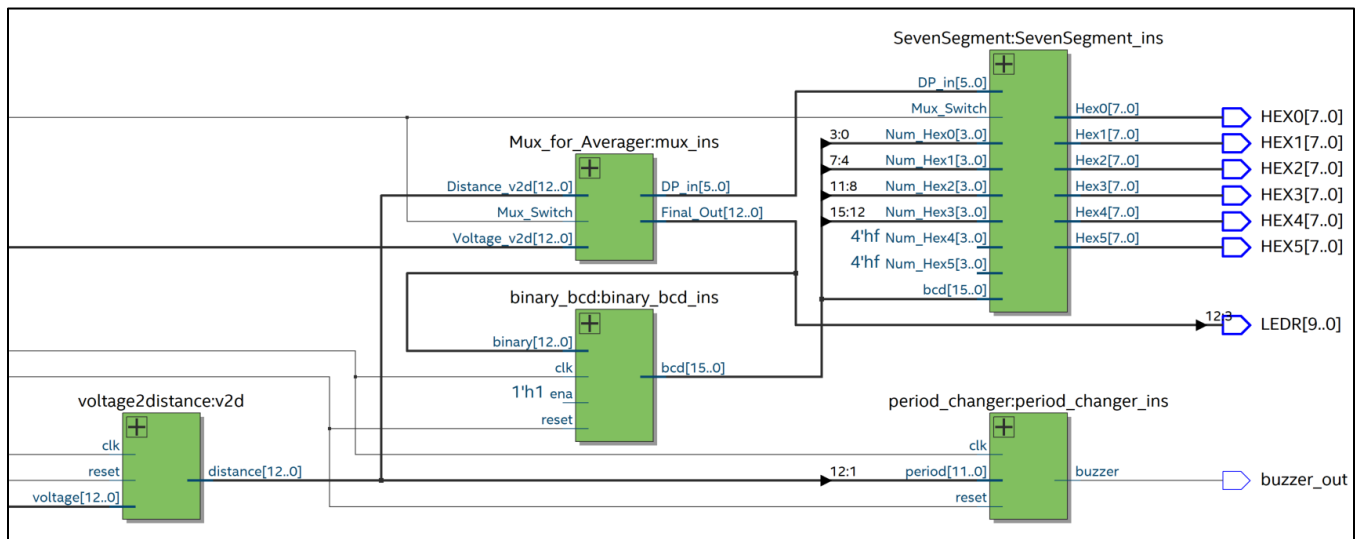
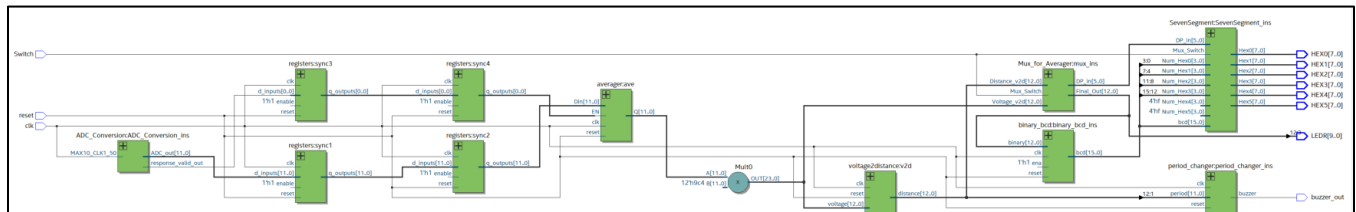
Bilal Dawood – 30092405

Yahia Abrini - 30090288

Zaid Mujtaba - 30095352

### Top level RTL Schematic:

*Note: the first figure shows the full RTL design, and the second figure is zoomed into the right portion (where we've added a new final for lab 4). The PWM output comes from the period\_changer component.*



**Screenshot of timing analysis:**

Slow 1200mV 85C Model Fmax Summary				
<<Filter>>				
	Fmax	Restricted Fmax	Clock Name	Note
1	61.07 MHz	61.07 MHz	clk	
2	121.85 MHz	121.85 MHz	ADC_Conversion_ins u0...l_sys sd1 pll7 clk[0]	

Slow 1200mV 0C Model Fmax Summary				
<<Filter>>				
	Fmax	Restricted Fmax	Clock Name	
1	66.53 MHz	66.53 MHz	clk	
2	130.01 MHz	130.01 MHz	ADC_Conversion_ins u0...l_sys sd1 pll7 clk[0]	

## Screenshot of Waveform Simulation:

*Note: random binary values were placed inside a newly-created input called “test\_input” to verify the correct operations of “buzzer\_out” for the ModelSim simulation. Buzzer\_out can be seen to be changing in accordance with the specified requirements to generate the desired pitch. As can be seen, the bigger the test\_input the lower frequency buzzer\_out has (and thus, pitch is lower representing further distance). The opposite is also true. Reset can also be seen working (buzzer\_out = 0 when reset = 1).*

