

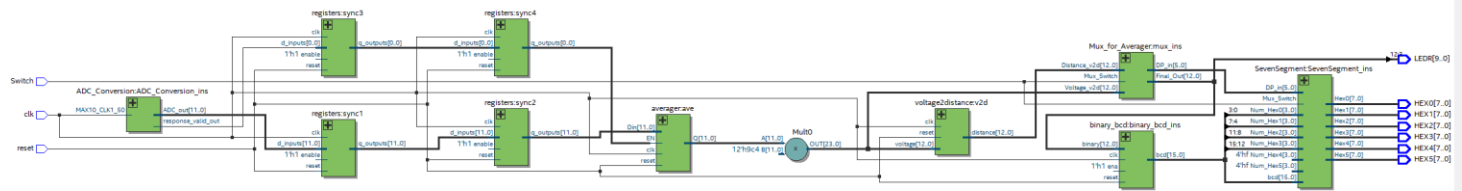
Prelab Top level testbench:

	Msgs								
/tb_prelab/clk	-No Data-								
/tb_prelab/clk_period	-No Data-	25000 ps							
/tb_prelab/HEX0	-No Data-	255							
/tb_prelab/HEX1	-No Data-	255							
/tb_prelab/HEX2	-No Data-	192	255	192	255	192	255		
/tb_prelab/HEX3	-No Data-	64	127	64	127	64	127		
/tb_prelab/HEX4	-No Data-	192	255	192	255	192	255		
/tb_prelab/HEX5	-No Data-	192	255	192	255	192	255		
/tb_prelab/LEDR	-No Data-	0	X	0	X	0	X		
/tb_prelab/reset	-No Data-								
/tb_prelab/switch	-No Data-								

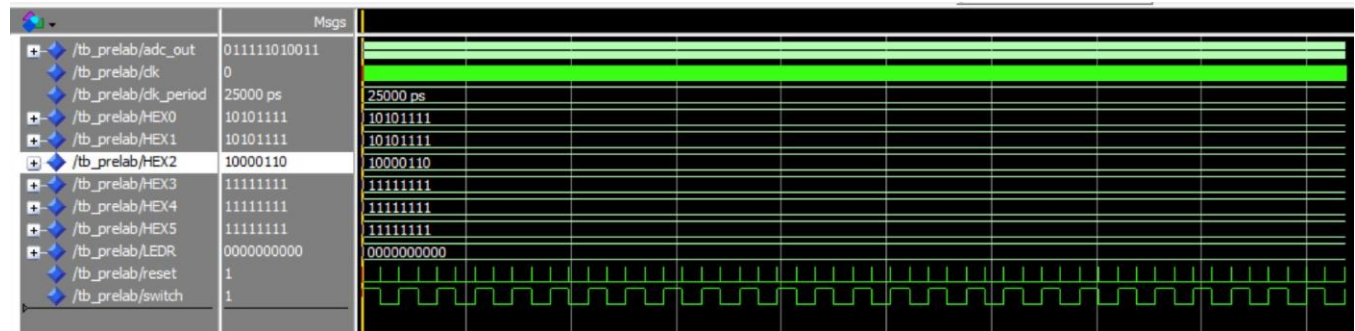
In-lab submission is on next page.

ENEL 453 LAB 3 – SUBMISSION

Screenshot of RTL:



Screenshot of simulation of distance measurer:



Screenshot of timing analysis:

The screenshot shows the Xilinx ISE timing analysis tool. The left pane displays the 'Table of Contents' with the 'Timing Analyzer' expanded. The main pane shows the 'Slow 1200mV 85C Model Fmax Summary' report. The report includes a table with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	64.69 MHz	64.69 MHz	clk	
2	119.8 MHz	119.8 MHz	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]]	

Below the table, a note states: 'This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of'.

The screenshot shows the Xilinx ISE timing analysis tool. The left pane displays the 'Table of Contents' with the 'Timing Analyzer' expanded. The main pane shows the 'Slow 1200mV 0C Model Fmax Summary' report. The report includes a table with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	70.21 MHz	70.21 MHz	clk	
2	127.52 MHz	127.52 MHz	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]]	

Below the table, a note states: 'This panel reports FMAX for every clock in the design, regardless of the user-specified clock periods. FMAX is only computed for paths where the source and destination registers or ports are driven by the same clock. Paths of'.