

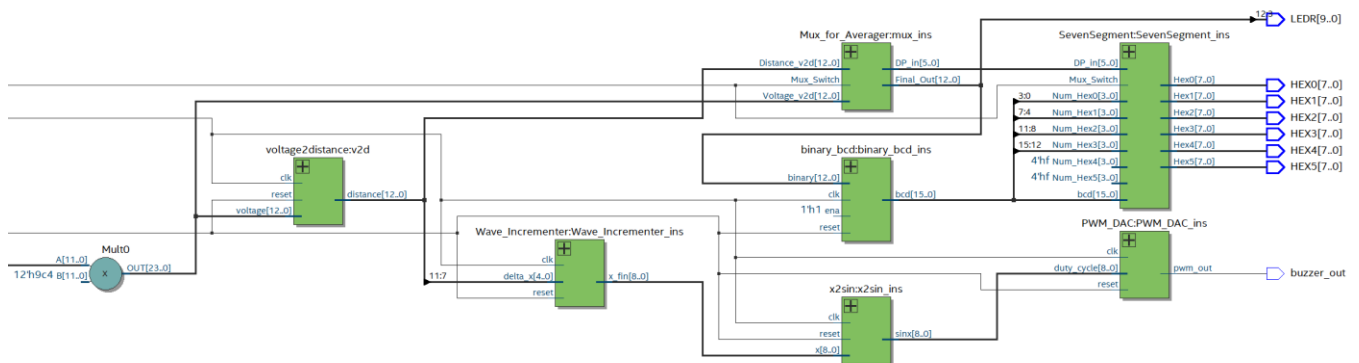
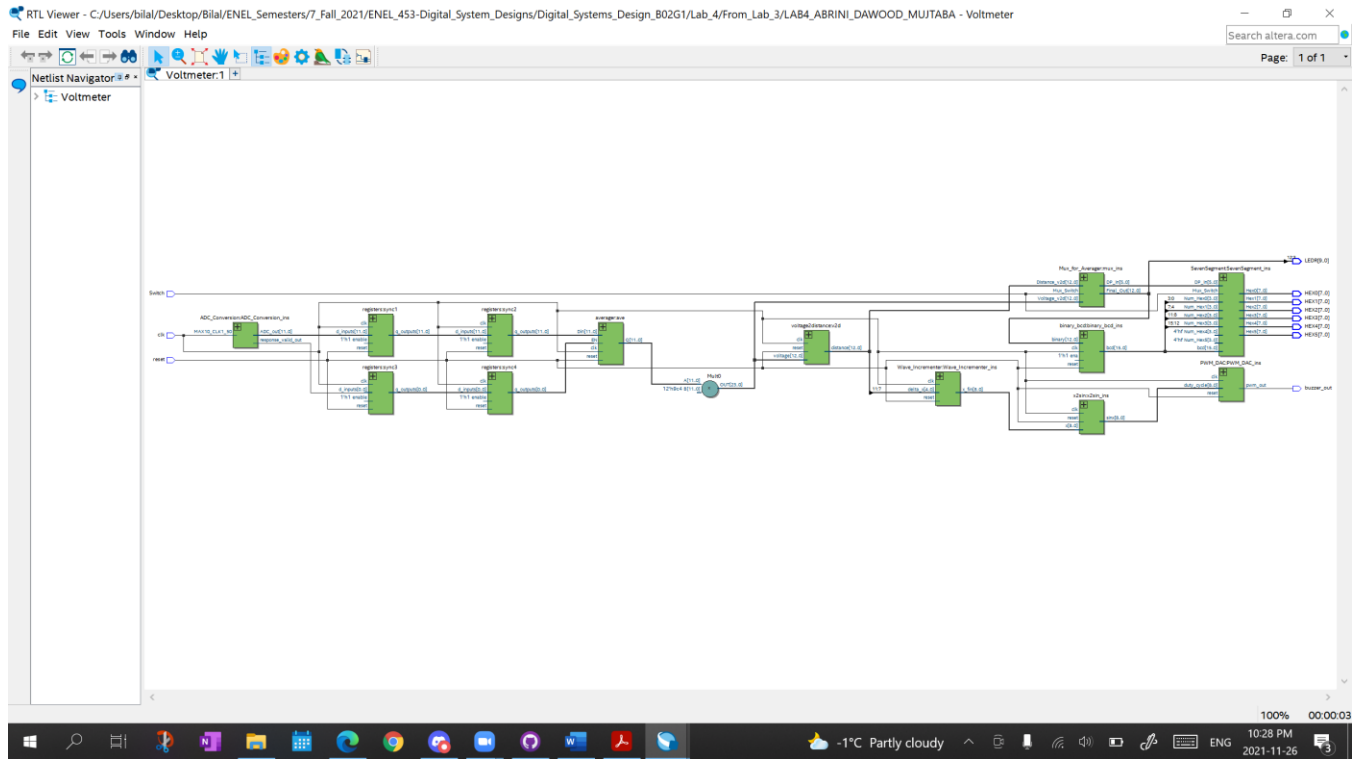
ENEL 453 LAB 4 – SUBMISSION

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Top level RTL Schematic:



Screenshot of timing analysis:

The first screenshot shows the 'Slow 1200mV 85C Model Fmax Summary' report. It contains a table with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	66.5 MHz	66.5 MHz	clk	
2	133.69 MHz	133.69 MHz	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]	

The second screenshot shows the 'Slow 1200mV OC Model Fmax Summary' report. It contains a table with the following data:

	Fmax	Restricted Fmax	Clock Name	Note
1	72.12 MHz	72.12 MHz	clk	
2	142.13 MHz	142.13 MHz	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]	

The third screenshot shows the 'Fast 1200mV OC Model Setup Summary' report. It contains a table with the following data:

	Clock	Slack	End Point TNS
1	clk	13.521	0.000
2	ADC_Conversion_ins[u0]altpll_sys[sd1]pll7[clk[0]	36.469	0.000

Screenshot of Waveform Simulation:

