Bilal Dawood

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Education

University of Calgary Calgary, AB

BSc in Electrical Engineering, Minor in Digital Engineering — GPA: 3.64 *Aug. 2019 – May 2024*

Relevant Coursework: Application Specific Processors and Accelerators, Industrial IoT, Advanced ML and NN

Experience

Digital Hardware Engineer (intern) May 2022 – Aug 2023

Ericsson Canada Inc *Ottawa, ON*

- Achieved 70% reduction in Thermal verification time by developing an automation tool using Python.
- Ensured accuracy by creating test cases and comparing recorded metrics manually with component datasheets.
- Showcased report writing and presentation skills by preparing user manual and presenting results to management.
- Ensured electrical functionality by verifying power rail integrity on high voltage radio boards using Power Tree and multimeter.
- Conducted board bring-up and verification by identifying and recording Flash SPI timing parameters using Oscilloscope.
- Confirmed data transfer compliance by identifying and recording Flash SPI interface timing parameters using Oscilloscope.
- Supported PCB design verification using Cadence Allegro by leveraging existing radio board schematics.
- Hands on experience with UART, JTAG, I2C and SPI with Ericsson radio boards.
- Power Rail Analysis using Power Tree and measuring continuity across capacitors to ensure no shorts were created.
- Leading research on high-frequency testing equipment, targeting optimal performance and value by comparing price with datasheet specifications and testing requirements.

Android SDK/NDK Full-Stack Developer (Intern) Feb 2023 – Aug 2023

Ericsson Canada Inc. *Ottawa, ON*

- Enhanced backend data management by 57% for application by creating 4 new classes and off-loading 80% of the data.
- Increased UI functionality by incorporating filters.
- Reduced page load times by 90% by optimizing app performance, showcasing expertise in software optimization.
- Collected and analyzed 5G performance metrics using Qualcomm Network Testing Device, contributing to app development.

Leadership Experience

Treasurer Aug 2020 – May 2022

IEEE UofC Student Branch Executive Council *Calgary, AB*

- Managed and maintained branch accounts for professional associations.
- Prepared and submitted Annual Budget reports and Financials.
- Developed financial strategies, ensured suitable funding for events, and advised on activity cost allocation.
- Presented data in a methodical format in front of other executive council members, demonstrating analytical thinking and proactive communication skills.

Electrical Team Lead Sept 2021 – Sept 2022

Team Zeus *Calgary, AB*

- Provided guidance to 5 members for completion of electrical wiring of Formula SAE electric car.
- Collaborated with other technical teams to integrate electrical systems into the vehicle.
- Assisted in designing and testing Battery Management System (BMS) and Electrical Control Unit (ECU).
- Applied practical experience in developing and testing Power Distribution Units (PDUs).

Projects

Automated Transit Enforcement | *Python, Git, Software Dev, Hardware Dev* Sept 2023 – May 2024

- Developed a comprehensive hardware block diagram to outline the integration and use of various components.
- Conducted research and selected hardware components based on literature review, electric ratings, and cost to select optimal components while ensuring functionality and compatability.
- Reduced power consumption by 36% by developing a proof-of-concept with RPi and sensors (LiDAR, GPS, camera)
- Reduced memory utilization and processing time by 800% by setting appropriate triggers through embedded designing
- Integrated hardware components with the software server, ensuring smooth data transfer and system operation.
- Conducted extensive testing to ensure system reliability and performance under various operational conditions.
- Regularly shared progress with Calgary Transit, explaining tehcnical details in easy to undestand manner.

Real-time Audio Filtering | *C, ARM Assembly, STM MCU, Embedded Systems* Jan 2024 – May 2024

- Designed and implemented embedded real-time audio filter on the STM32F411 using C and ARM Assembly.
- Reduced filter sampling rate by 28% and reduced program size by 13.6% by utilizing optimization techniques involving block processing and use of ARM Assembly.
- Implemented and compared various FIR filtering techniques (Circular Buffer, Block Processing).
- Compared performance (speed, memory usage, program size) and verified integrity of filter after implementation.
- Implemented Loop Unrolling and utilized architecture-specific SIMD instructions to meet audio timing requirements.
- Created Python notebook to verify integrity of signal after filtering.

2D Image Convolution | *C, Python, STM MCU, ARM Cortex-M4, DSP, Embedded Systems* Jan 2024 – May 2024

- Implemented various 2D Image filtering techniques using 3x3 kernels on STM32F411 using C.
- Loaded images to STM Microcontroller as binary file. Utilized convolution techniques to filter images.
- Paid close attention to data access and boundary handling for image convolution.
- Implemented and observed the affect of various 3x3 kernels (edge filter, gaussian blur, sharpening).
- Created Python notebook to view images by decrypting binary file.
- Demonstrated expertise in digital signal processing and embedded systems.

Hardware Accelerator (Pynq-Z2 FPGA) | *C, Xilinx Vitis HLS, FPGA, Python* Jan 2024 – May 2024

- Utilized AMD Xilinx Vitis High-Level-Synthesis (HLS) to build, synthesize and debug C code.
- Generated RTL designs and ensured proper resource utilization.
- Implemented hardware optimization techniques to improve performance of MAC operations on FPGA.
- Demonstrated proficiency with Loop Unrolling, Loop Fission and Pipelining optimization techniques on hardware.
- Conducted thorough testing and validation procedures using testbenches created in C as well as through C simulation and synthesis, to ensure functionality and performance of operations.
- Analyzed synthesis reports and utilized pragma directives to optimize loop latency, resource utilization and overall performance of hardware design.
- Contributed to the development of optimized hardware accelerators, enhancing processing efficiency and throughput for FPGA-based applications.
- Achieved 13%-time reduction verified by exporting IP and generating bit-files to flash bitstreams to FPGA via Python notebook.

SolarCam | *Embedded Systems, Solar Powered, C++* Jan 2022 – May 2022

- Developed an ESP32-microcontroller based solar powered security camera.
- Successfully sourced and integrated electrical components including solar panels, ESP32, PIR sensor, and camera module.
- Controlled GPIO pins using C++ to capture and save images.
- Designed a self-sustaining power system with solar charging, battery storage, and regulated voltage.
- Ensured adherence to relevant regulatory codes (ISO, CEC) for product quality, safety, and environmental considerations.

Deep learning Finger Digit Classifier GUI | *Python, Machine Learning, GUI, Data Visualization* Jan 2022 – May 2022

- Developed a finger digits classifier with fastai and a CNN, achieving a significant accuracy boost from 60% to 88%.
- Employed data augmentation techniques to enhance real-time finger count prediction accuracy.
- Proficiently managed image data and analyzed model performance for thorough evaluation and refinement.
- Created a user-friendly GUI application and utilized Python libraries effectively for streamlined development and enhanced collaboration.
- Utilized Git for version control, maintaining a clean and organized codebase.
- Employed Seaborn and Matplotlib for data visualization, enhancing the presentation of results.

Yagi-Uda Antenna Design | *Antenna Design, Signal Processing, Docuementation* March 2022 – May 2022

- Designed a Yagi-Uda antenna using copper wires and a split coaxial cable.
- Ensured optimal signal reception by achieving a power transfer of -20dB, indicating that 1% of power was reflected.
- Conducted experiments to measure the performance of the antenna under different conditions (materials, orientations).
- Used RTL-SDR USB radio devices and software to measure and analyze signal outputs.
- Identified and resolved issues during the design and testing phases of the antenna project, such as signal interference.
- Ensured precision in component measurements and soldering to achieve desired signal reception and circuit performance.
- Documented the design, methodology, results, and analysis of the projects in detailed reports.
- Tested the antenna with various materials between the transmitting and receiving antennas, demonstrating robustness and adaptability to different environmental conditions.
- Used RTL-SDR USB for receiving and demodulating audio signals, and measuring signal outputs under various conditions

AM Receiver System Desing | *Circuit Design and Analysis, Multisim, Simulation* Oct 2021 – Dec 2021

- Designed and implemented an AM receiver system.
- Developed active filter and base-band amplifier circuits.
- Used parametric sweeps and AC analysis to optimize circuit performance.

- Analyzed signals at different points in the AM receiver circuit to ensure proper reception and demodulation.
- Used simulation software (NI Multisim) to verify theoretical calculations and optimize circuit designs.
- Documented the design, methodology, results, and analysis of the projects in detailed reports.
- Utilized for DC and AC analysis, including tools like Multisim or similar simulation platforms for parametric sweeps and small-signal analysis.

Altera DE10-Lite Distance Sensor | *VHDL, Intel Quartus Prime, MODELSIM, FPGA* Sept 2021 – Dec 2021

- Implemented voltage-to-distance conversion in VHDL using Intel Quartus Prime.
- Design and implementation met timing requirements for digital signal processing.
- Created testbenches to conduct tests and simulate digital signals and switch gates to be verified using MODELSIM.
- Configured DE10 display for distance/voltage based on switch state.
- Demonstrated proficiency in FPGA programming, sensor integration, and VHDL, highlighting skills in hardware design and testing.
- Generated RTL schematic to view flow of bits.

Point Based Graphical Zoom | *MATLAB, Graphical User Interface, Image Processing* July 2021 – July 2021

- Used MATLAB to create a graphical point-based zoom function.
- The function generated a bounding box and produced a new figure based on any two points on a MATLAB-produced graph.

UnderPressure Posture Corrector | *C++, Embedded Systems, Agile, Product Development* Jan 2021 – May 2021

- Developed an Arduino-based posture corrector using an Arduino Nano, resistive strips, and a speaker.
- Applied voltage dividers and utilized C++ and Arduino IDE for embedded programming.
- Implemented Agile project management methodologies (sprint and scrum) for efficient development.
- Received awards for "Most Innovative Product," "Best Marketing," and "Best Use of Humor."

DFF Synchronous Sequential Circuit | *Simulation, Analysis, Digital logic Design* Nov 2020 – Dec 2020

- Implemented d-latches and d-flip-flops using Quartus for simulation and verification.
- Designed a synchronous detector circuit, creating state transition diagrams and K-maps to define behavior.
- Developed a clock divider to manage timing requirements within digital circuits.
- Utilized Intel Quartus Prime for designing, simulating and verifying digital circuits.
- Utilized K-maps to simplify logic desing.
- Ensured accurate operation of digital components, with the synchronous detector circuit correctly identifying the binary sequences
- Simplified logical expressions from K-maps to enhance circuit efficiency, demonstrating advanced problem-solving skills.

C++ Flight Management Program | *C++, File Handling, Algorithm, Software Development* June 2020 – July 2020

- Developed and implemented a Flight Management Program in C++, incorporating classes for Flight, Passenger, and Seat.
- Utilized file handling to read and process flight information from a text file, showcasing proficiency in data input/output operations.
- Implemented functionalities such as displaying seat maps, managing passenger information, adding/removing passengers, and saving data to enhance the program's usability.
- Applied the Selection Sort algorithm for efficient organization of passenger data based on seat locations, demonstrating algorithmic problem-solving skills.

Impact of Green Line LRT Research Project | *Research, Analysis, Presentation* July 2020 – Aug 2020

- Researched and wrote a report on the impact of the Green Line LRT and its stations on stakeholders.
- Analyzed stakeholders, including the public, residents near the station, taxpayers, and Calgary Transit employees.
- Considered financial restrictions and proposed solutions to potential problems.
- Gave a professional and technical presentation summarizing findings.

Calgary Weather Data Visualization | *Java, GUI, Data Visualization* Nov 2019 – Dec 2019

- Implemented a GUI and user-interactive program using Java-based Language Processing.
- Displayed daily average minimum and maximum temperature data for the last 30 years in Calgary.
- Enabled user flexibility in selecting data for specific months and displaying maximum or minimum temperatures.

Technical Skills

Languages: Java, Python, C/C++, MATLAB, JavaScript, HTML/CSS, Assembly (ARM, MIPS), Verilog
Frameworks: React, Node.js, Flask, FastAPI, Tensorflow
Developer Tools: Git, Gerrit, Linux, PuTTy, MS Azure, VS Code, PyCharm, Jira
Design and Simulation: Cadence Allegro, MODELSIM, NI Multisim, PS:SE, Xilinx Vivado, Intel Quartus Prime, SIMULINK
Hardware Tools: Oscilloscope, Spectrum Analyzer, Multimeter, Solder, Power Supplies, STM MCU, Pynq Z2 FPGA, PIC MCU
Libraries: Pandas, NumPy, Matplotlib, Seaborn, Tkinter, Keras, OpenCV, Pillow, Scikit-learn

Awards

Jason Lang Scholarship(2020, 2021, 2023), **Dean's List**(2020, 2021, 2024)