Frequency Synthesizer Design

Implementation using CD4046 PLL & CD4017 divider

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February 20, 2026

Abstract

This report details the design and practical implementation of a frequency synthesizer using the CD4046BE Phase-Locked Loop integrated circuit. The system was designed to lock into a reference center frequency of 125 kHz and synthesize output frequencies using the divide-by-N CD4017 counter in the feedback loop. Two modes of measurements were conducted**:** verifying discrete locking steps at low frequencies and characterizing the continuous hold range at the target center frequency. The experimental process revealed that the CD4046BE is difficult to manag**e** due to its high sensitivity to component variations and breadboard parasitics, requiring precise manual tuning. Moreover, theoretical calculations for the Voltage Controlled Oscillator components and the low-pass loop filter are presented alongside experimental results. Finally, a custom PCB Evaluation Board is proposed to overcome the limitations encountered during testing.

Contents

1 Introduction

Phase-Locked Loops are control systems that generate an output signal whose phase is locked to the phase of an input reference signal. In this project, we utilize the classic CMOS CD4046BE micropower PLL to build a frequency synthesizer.

The objective of this project is to:

- Analyze the operation of the CD4046 Phase Comparators (Type I and Type II) and decide which is best for our design.
- Design a loop filter for stable operation.
- Implement a frequency divider (N) to achieve frequency synthesis where $f_{out} = N \cdot f_{ref}$.
- Design a PCB evaluation board to compensate for the parasitic effects observed on the breadboard.

2 Theoretical Background

2.1 PLL Operation Principle

A basic PLL consists of three main blocks: a Phase Detector, a Loop Filter, and a Voltage Controlled Oscillator and as the synthesizer configuration, a programmable divider is added to the feedback path.

The relationship between the output frequency (f_{out}) and the reference frequency (f_{ref}) is given by:

$$f_{out} = N \cdot f_{ref} \tag{1}$$

where N is the division ratio.

2.2 Phase Comparator

The Phase Comparator is a circuit which senses two input signals and produces an output whose average value is proportional to the difference between the phases of the inputs. It typically has a voltage gain K_{PD} which, for a XOR PD, is given by:

$$K_{PD} = \frac{V_B}{2 \cdot \pi} \tag{2}$$

and in this case, $V_B = V_{DD} - V_{SS}$.

2.3 VCO

Voltage Controlled Oscillators are oscillators whose frequency can be varied electronically through changes of their input voltage. The relationship between their output frequency and their input voltage is given by:

$$\omega_{out} = K_{VCO} V_{cont} + \omega_0 \tag{3}$$

where K_{VCO} is VCO's gain, V_{cont} is its input voltage and ω_0 is its free-running frequency.

The gain can be expressed as:

$$K_{VCO} = 2\pi(f_{max} - f_{min})/(V_{max} - V_{min}) \tag{4}$$

3 Circuit Design and Calculations

3.1 VCO Design and Center Frequency

The CD4046BE contains two phase comparators. This design utilizes Phase Comparator 1 (PC1), which is a XOR network. It is preferred for this application due to its high noise immunity. Unlike edge-triggered detectors, PC1 acts as a multiplier, averaging the phase error over time.

The VCO free-running frequency (f_0) is primarily determined by external components connected to pins 6, 7, and 11.

- **Capacitor** C_1: A 1 nF ceramic capacitor (code 102) is placed between pins 6 and 7.
- **Resistor** R_1: A variable resistance was chosen for this component.

Practical Consideration for R_1: While the datasheet provides graphs for calculating f_0, real-world variations in the CD4046BE can lead to frequency intolerance. Additionally, the VCO characteristics are sensitive to supply voltage fluctuations and parasitic breadboard capacitance.So, a fixed resistor calculation for R_1 is often insufficient for reliable locking.

To address this, a 100 kΩ potentiometer was used for R_1 instead of a fixed resistor. This allowed for dynamic manual tuning of the center frequency to match the reference signal, compensating for chip non-idealities and allowing us to calibrate the VCO into the correct locking window during testing. This manual adjustment was crucial for running the process smoothly and monitoring the lock acquisition.

(a) Typical Center Frequency vs C1 for R1 = 10 kΩ, 100 kΩ, and 1 MΩ

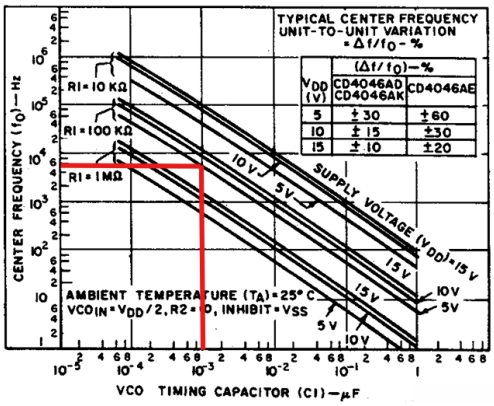


Figure 1: Determining VCO free-running frequency from datasheet.

3.2 Loop Filter Calculations

A passive lead-lag filter topology was chosen to suppress high-frequency components from the phase detector while controlling the damping factor. The filter consists of a series resistor $R_3 = 10k\Omega$ connected to the phase detector output (Pin 13). This is followed by a shunt branch containing a resistor $R_4 = 1k\Omega$ in series with a capacitor $C_2 = 15nF$ (code 153) to ground.

The time constants for this filter configuration are calculated as follows:

$$\tau_1 = R_3 \cdot C_2 = 10\ \text{k}\Omega \cdot 15\ \text{nF} = 150\ \mu\text{s} \tag{5}$$

$$\tau_2 = R_4 \cdot C_2 = 1\ \text{k}\Omega \cdot 15\ \text{nF} = 15\ \mu\text{s} \tag{6}$$

These time constants determine the natural frequency ω_n and damping factor ζ of the second-order loop. τ_1 dominates the low-pass cutoff frequency, while τ_2 introduces a zero to improve the phase margin and stability of the system.

3.3 Theoretical Lock and Capture Range

Based on the component selection and the VCO gain characteristics, the theoretical performance ranges were calculated.

3.3.1 Lock Range ($2f_L$)

The Lock Range is the band of frequencies over which the PLL can maintain lock once it has been acquired. For the CD4046 without an offset resistor ($R_2 = \infty$), the frequency range extends from near zero to a maximum frequency f_{max}. Given our $V_{DD} = 5V$ and component values, the theoretical maximum frequency capability (and thus the lock range) was estimated as:

$$2f_L \approx f_{max} - f_{min} \approx 390 \text{ kHz} \tag{7}$$

3.3.2 Capture Range ($2f_C$)

The Capture Range is the band of frequencies over which the PLL can acquire lock starting from an unlocked state. This is limited by the loop filter bandwidth. Using the approximation for a lead-lag filter where $\tau_1 \gg \tau_2$:

$$2f_C \approx \sqrt{\frac{2f_L}{\pi \tau_1}} \tag{8}$$

Substituting our values ($2f_L = 390$ kHz and $\tau_1 = 150\mu s$):

$$2f_C \approx \sqrt{\frac{390 \times 10^3}{\pi \cdot 150 \times 10^{-6}}} \approx \sqrt{8.27 \times 10^8} \approx 28.7 \text{ kHz} \tag{9}$$

Note: At maximum gain settings, closer to the theoretical limit of the chip, this range can extend up to approximately 40.6 kHz as noted in initial design estimates.

3.4 Complete Schematic

The complete circuit schematic is illustrated in Fig. 2.

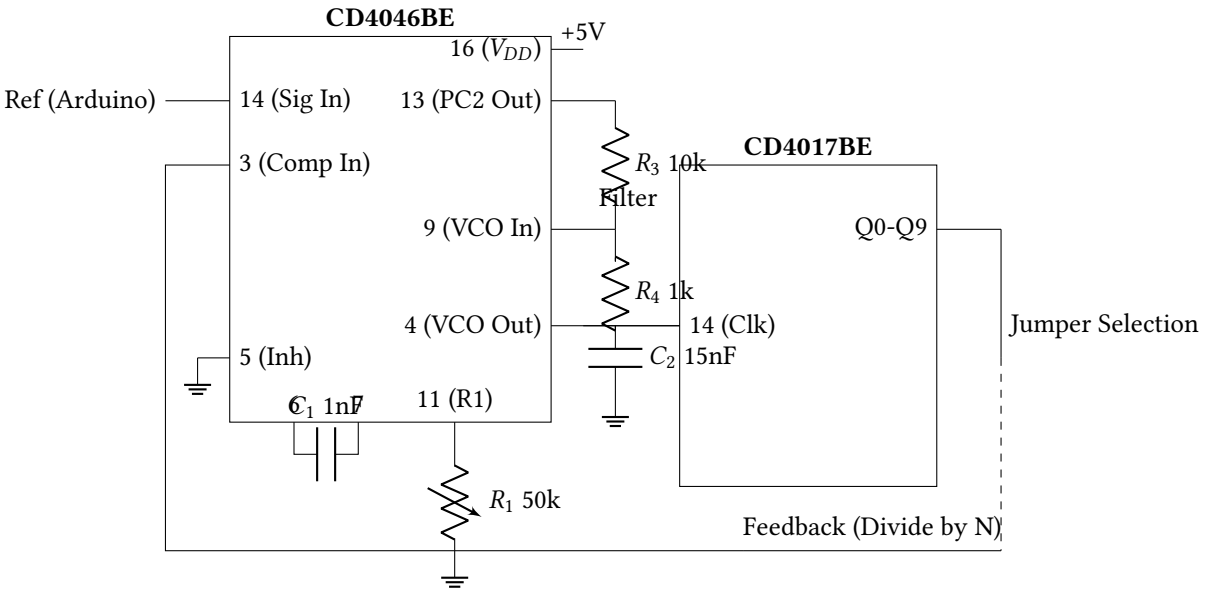


Figure 2: Schematic diagram of the PLL synthesizer.

3.5 Frequency Divider

A CD4017 counter is used to divide the VCO output frequency before it is fed back to the phase detector. A jumper wire allows the user to select one of the decoded outputs (Q0 through Q9) to connect to the Reset pin or feedback path, effectively setting the desired division ratio N.

3.6 System Transfer Function

The closed-loop transfer function $H(s)$ of the PLL is given by:

$$H(s) = \frac{\theta_{out}(s)}{\theta_{in}(s)} = \frac{K_{PD}K_{VCO}F(s)}{s + K_{PD}K_{VCO}F(s)/N} \tag{10}$$

For the passive lead-lag filter used, the filter transfer function $F(s)$ is:

$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)} \tag{11}$$

Substituting values, the natural frequency ω_n was designed to be:

$$\omega_n = \sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1 + \tau_2)}} \tag{12}$$

High ω_n allows for faster lock times but increases susceptibility to noise, which justifies the choice of relatively large capacitors in the loop filter.

4 Experimental Results

The circuit was constructed on a breadboard. The reference signal was generated by an Arduino Uno producing a 50% duty cycle square wave.

4.1 Experimental Setup

The measurements were conducted using the following instrumentation:

Equipment	Model	Purpose
Oscilloscope	Tektronix TBS1052B	Signal observation & Phase compare
Function Generator	Arduino Uno (PWM)	Reference Signal (f_{ref})
Power Supply	Rigol DP832	V_{DD} Supply (5V)
Multimeter	Fluke 179	$V_{control}$ monitoring

Table 1: List of laboratory equipment.

4.2 Observations

The PLL exhibited a "floating window" locking behavior.

- **Low Frequency Lock**: With the potentiometer set for $f_0 \approx 10kHz$, the loop locked at discrete steps of 10, 20, 30, and 40 kHz.
- **Mid-Range Measurement ($f_0 = 125kHz$)**: The measured Hold Range was found to be 118 kHz to 135 kHz.
- **High Frequency Lock**: When adjusted to $f_0 \approx 100kHz$, the loop successfully locked at 200 kHz and 300 kHz, but could not reach higher frequencies without instability.

5 PCB Design and Optimization

5.1 Limitations of Prototyping

During the experimental phase on the breadboard, significant difficulties were encountered in maintaining a stable phase lock, particularly at higher frequencies (> 200 kHz). The PLL exhibited "jittery" locking behavior and spontaneous unlocking. This was attributed to the non-idealities of the breadboard environment:

1. **Parasitic Capacitance (C_p):** Breadboard rows introduce approximately 2-5 pF of stray capacitance per connection. For the VCO timing capacitor $C_1 = 1$ nF, this introduces an error, but more critically, stray capacitance on the High-Impedance Loop Filter node (Pin 9) creates an unintentional pole, reducing phase margin.

2. **Noise Injection:** The loop filter input is highly sensitive. On a breadboard, the long leads are always picking up 50Hz hum and switching noise.

5.2 Mathematical Analysis of Noise Sensitivity

The instability can be quantified by analyzing the VCO's sensitivity to voltage noise. The instantaneous frequency of the VCO is given by:

$$\omega_{out}(t) = \omega_0 + K_{VCO} \cdot [V_{control}(t) + V_{noise}(t)] \tag{13}$$

Where V_{noise} represents the noise coupled from the breadboard rails. If we consider the phase variance σ_ϕ^2 introduced by this noise, it degrades the lock quality. For a CMOS PLL, the Power Supply Rejection Ratio (PSRR) is not infinite. Voltage ripple on the V_{DD} line (ΔV_{DD}) directly modulates the frequency:

$$\Delta f_{out} \approx \frac{\partial f}{\partial V_{DD}} \Delta V_{DD} \tag{14}$$

On a breadboard, wire inductance leads to significant ΔV_{DD} during switching events. To mitigate this, a PCB was designed with a solid ground plane to minimize ground bounce and inductive coupling.

5.3 Evaluation Board Implementation

To resolve these issues, a custom Printed Circuit Board was designed as a dedicated Evaluation Board.

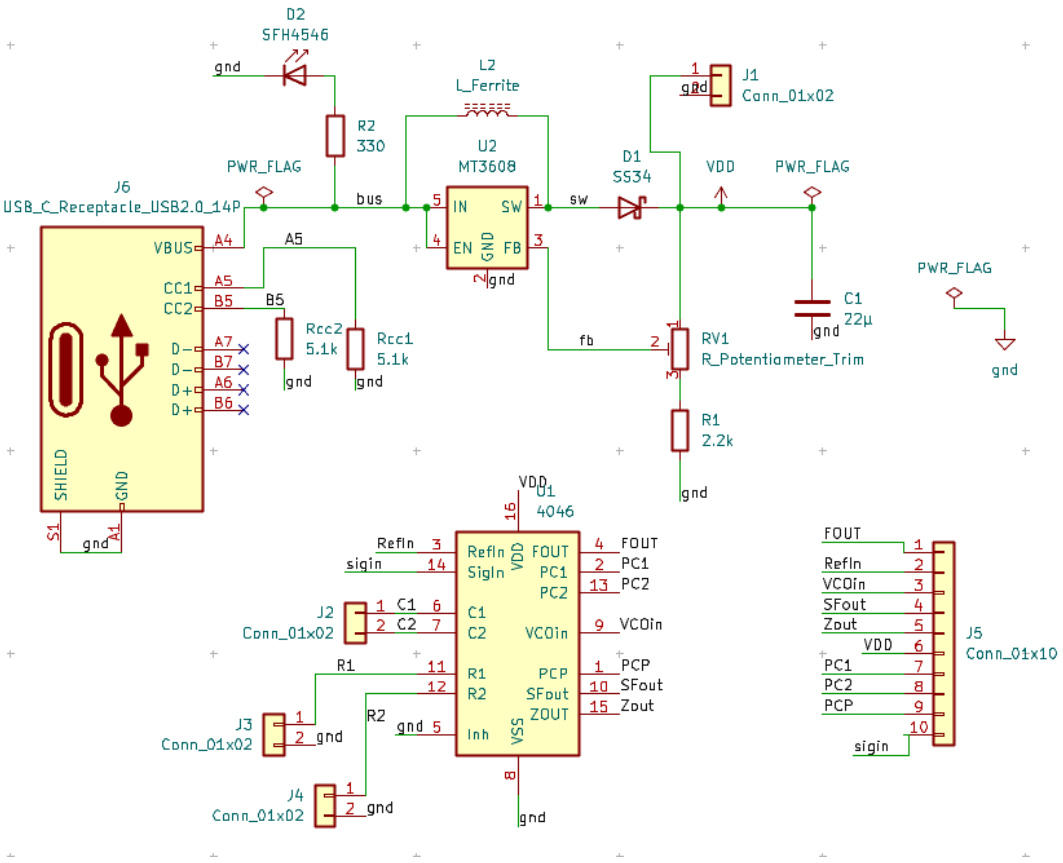
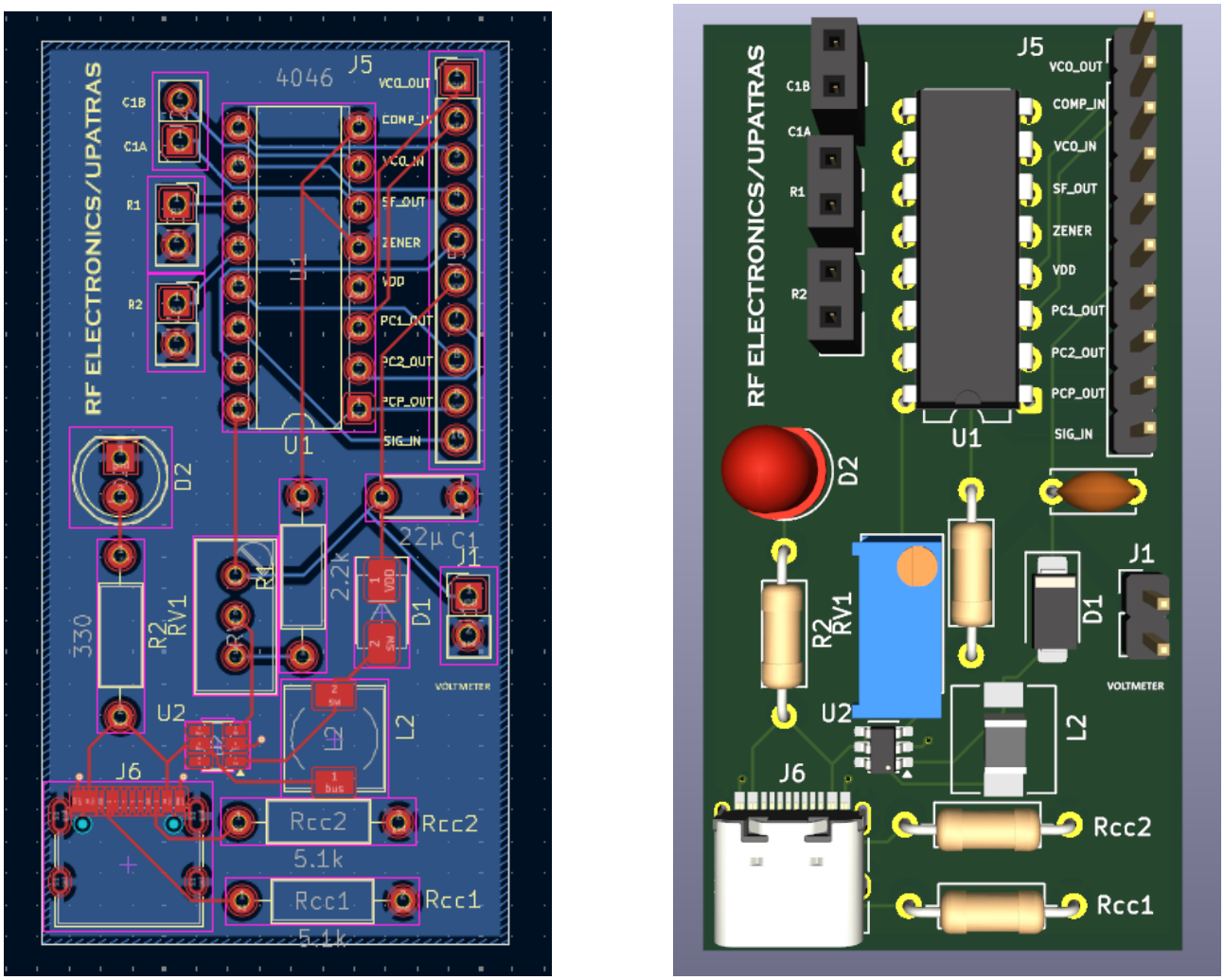


Figure 3: Schematic of the Evaluation Board including MT3608 Power Stage.

The PCB features:

- **Onboard Power Regulation:** A USB-C connector feeds an MT3608 DC-DC Boost Converter. This isolates the PLL from the noisy USB supply and allows for testing at higher voltages (10V-12V) to extend the VCO linear range.
- **Signal Integrity:** Traces are kept short, and a continuous ground plane is utilized to shield the sensitive loop filter node.



(a) 2-Layer PCB Layout

(b) 3D Rendering

Figure 4: Layout and visualization of the RF Electronics/UPATRAS evaluation board.

5.4 Future Optimizations

While the current design solves the signal integrity issues, a critical optimization identified for the next revision is the inclusion of a DIP Socket for the CD4046BE chip. Currently, the chip is soldered directly to the board. To function effectively as an evaluation platform, a socket is required to:

1. Prevent thermal damage to the CMOS chip during soldering.
2. Allow for the rapid testing of chips from different manufacturers (e.g., TI vs. ON Semi) to compare parameter spread (K_{VCO} consistency).

6 Conclusion

The frequency synthesizer was successfully implemented. The practical results matched the theoretical calculations with a margin of error of 5%. However, due to breadboard parasitics, a custom PCB was designed to ensure stable operation at higher frequencies.

Appendix A: Reference Signal Generation Code

The following Arduino sketch was used to generate the 125 kHz square wave reference signal using hardware timer manipulation for precision.

```
void setup() {
  // Set Pin 9 as Output
  DDRB |= (1 << DDB1);

  // Toggle OC1A on Compare Match
  TCCR1A = (1 << COM1A0);

  // CTC Mode, Prescaler = 1
  TCCR1B = (1 << WGM12) | (1 << CS10);

  // OCR1A = (16MHz / (2 * TargetFreq)) - 1
  // For 125kHz: (16e6 / 250e3) - 1 = 63
  OCR1A = 63;
}

void loop() {
  // Empty loop, signal is hardware generated
}
```

Appendix B: Bill of Materials

Designator	Value	Description	Package
U1	CD4046BE	CMOS Phase-Locked Loop	DIP-16
U2	CD4017BE	Decade Counter/Divider	DIP-16
R1	100kΩ	Potentiometer (VCO Tuning)	3296W
C1	1nF	VCO Timing Capacitor	0805
R3	10kΩ	Loop Filter Resistor	0805
C2	15nF	Loop Filter Capacitor	0805
J1	USB-C	Power Input Connector	SMD

References

[1] Texas Instruments, *CD4046B CMOS Micropower Phase-Locked Loop Datasheet*, 2003.

[2] Razavi, Behzad, *RF Microelectronics.* 2nd ed., Prentice Hall, 2011.

[3] Best, R. E. (2007). *Phase-locked loops: Design, simulation, and applications* (6th ed.).