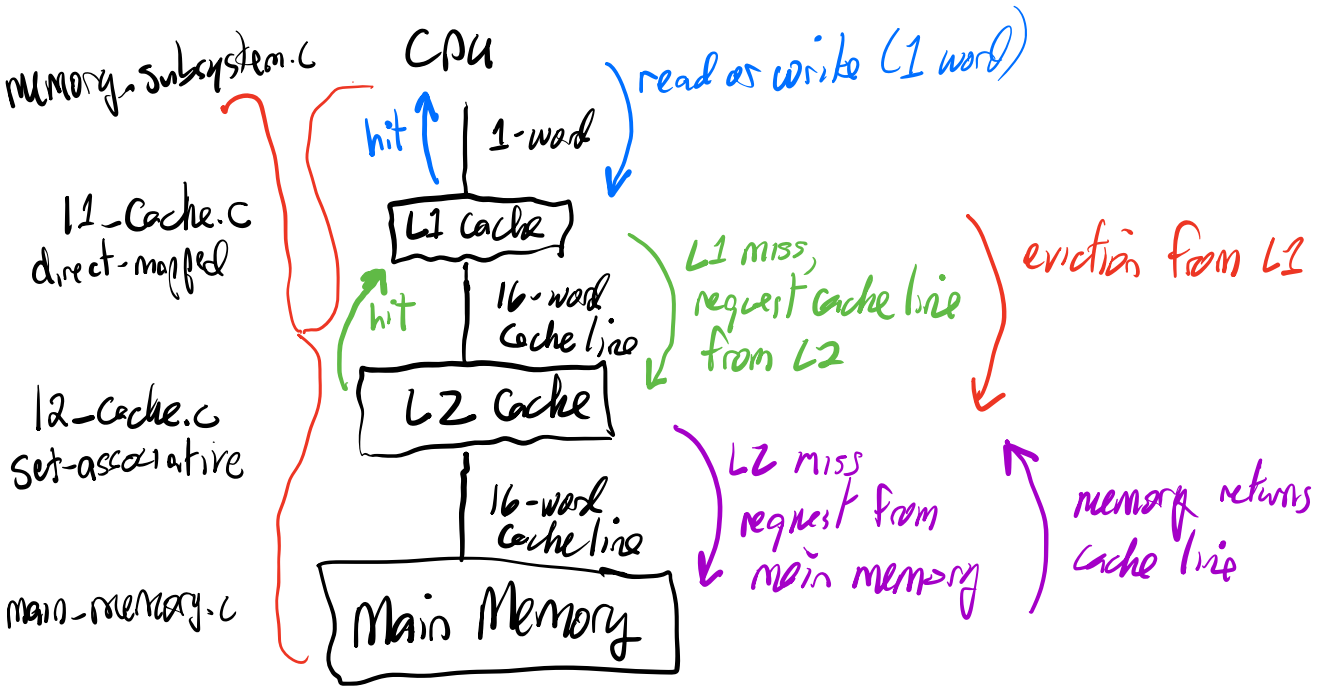
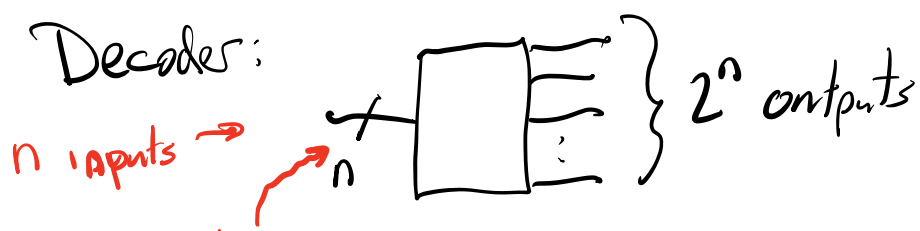
Cache Project

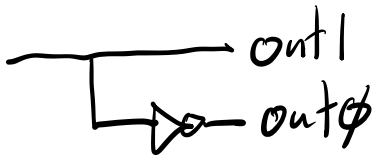


Back to digital logic:

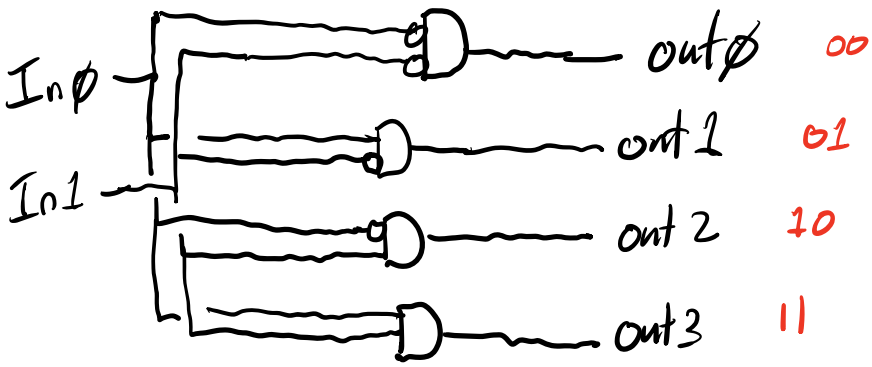
Decoder:



1 bit:



2 bit:



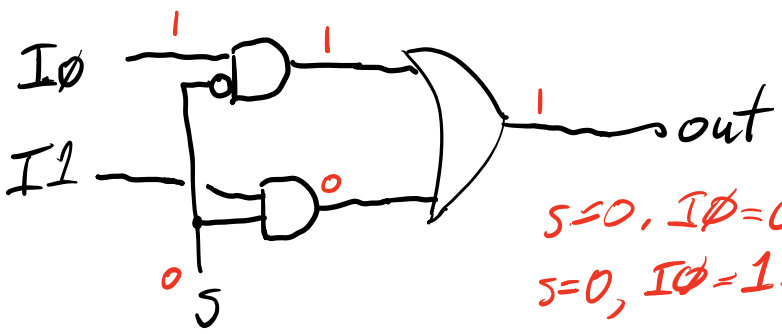
"Multiplexer" (multiplexor) "mux"

- selects one of the inputs to send to the output

The n-bit selector selects one of the 2^n inputs to send to the output.

If the value of the selector is i, then the output gets the value of input i.

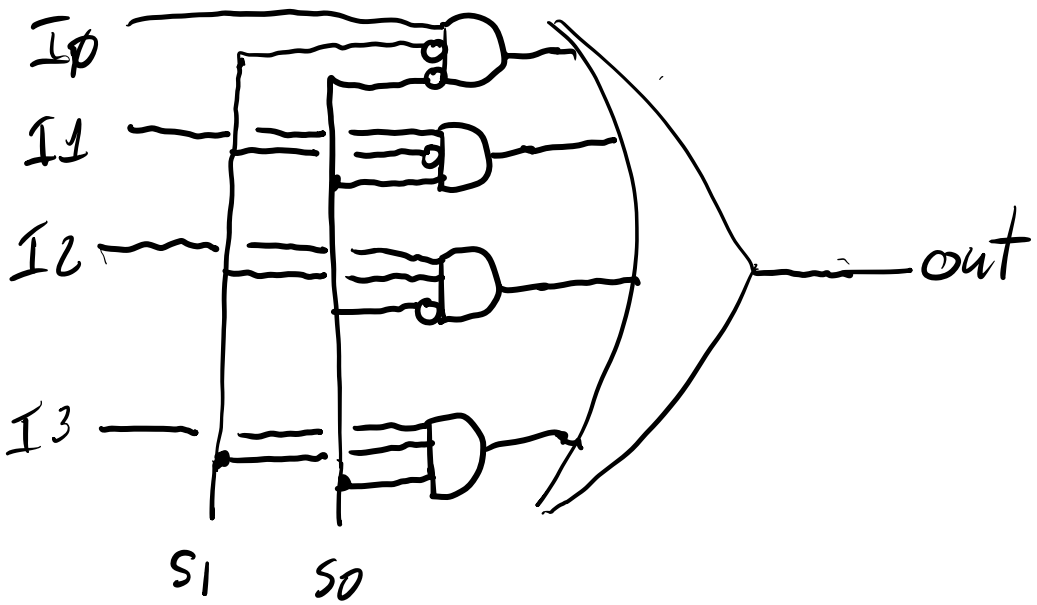
2-input mux (1 selector input)



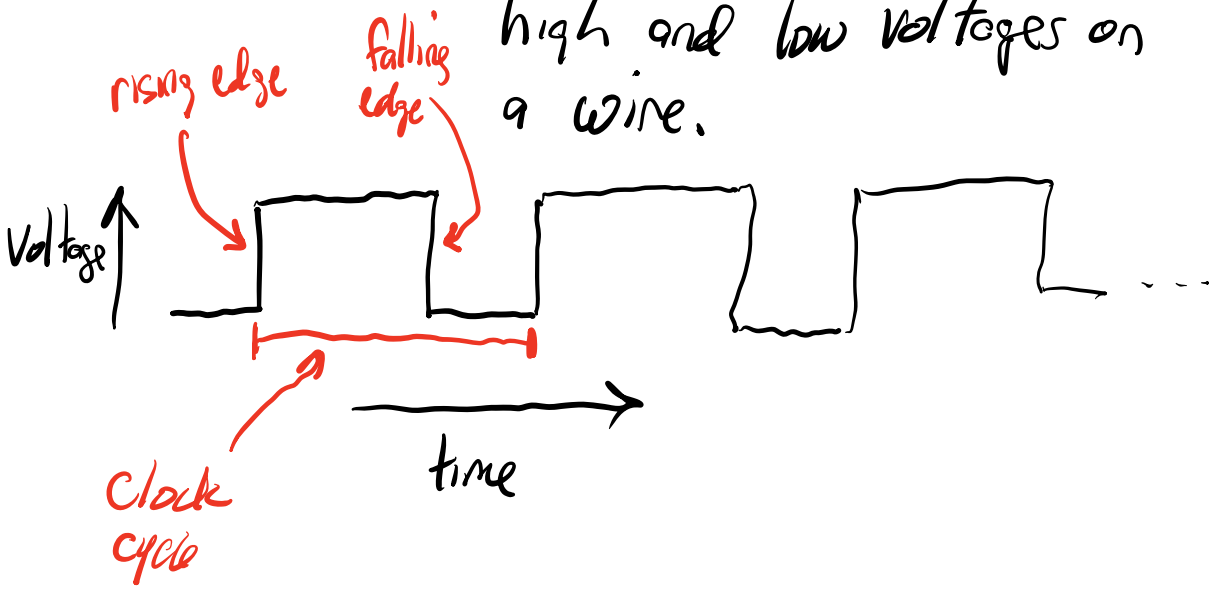
S=0, I0=0 ⇒ Out=0

S=0, I0=1 ⇒ out=1

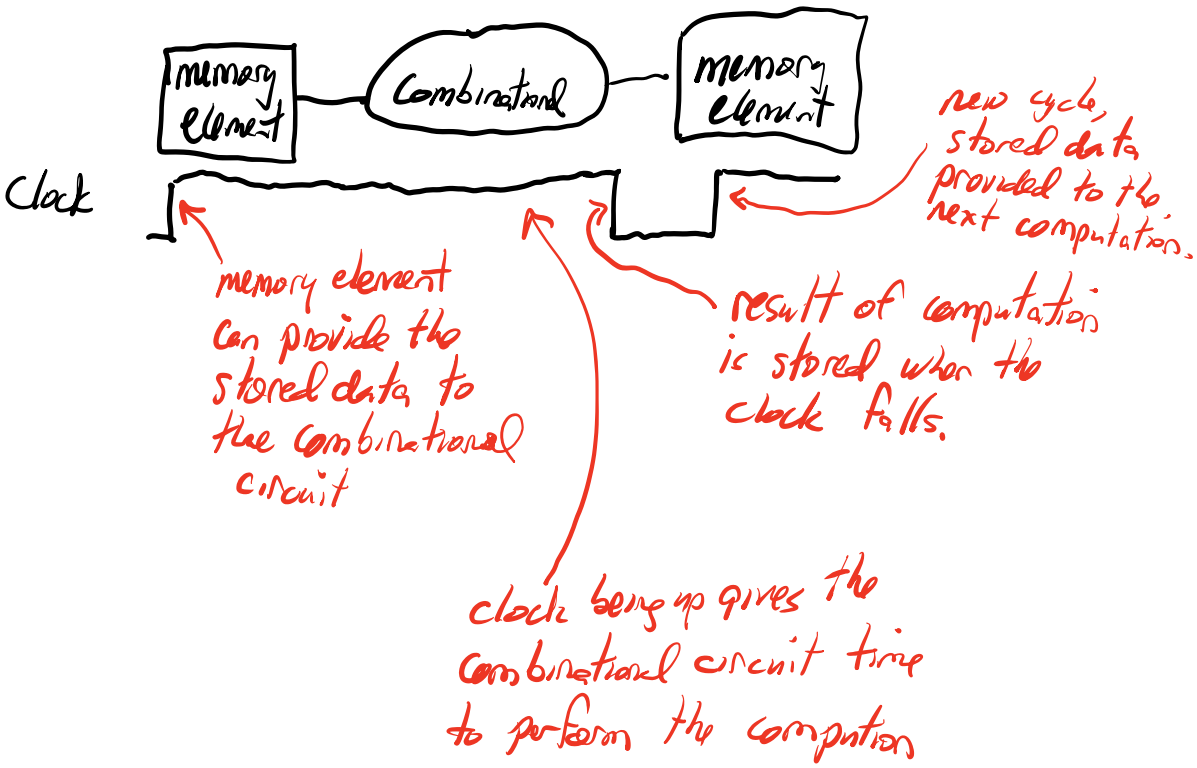
4-input mux (2 selector lines)



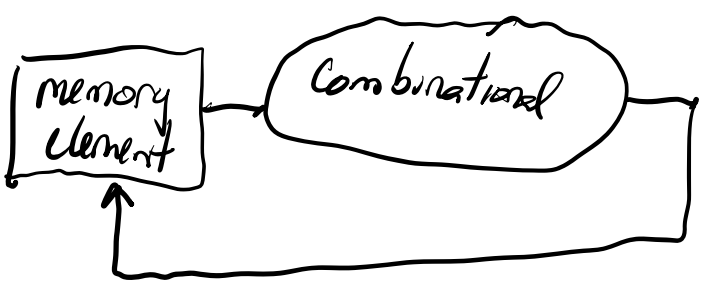
Clock - device that puts alternating high and low voltages on a wire.



A clock is used to synchronize actions in a circuit
- particularly the storing of data.



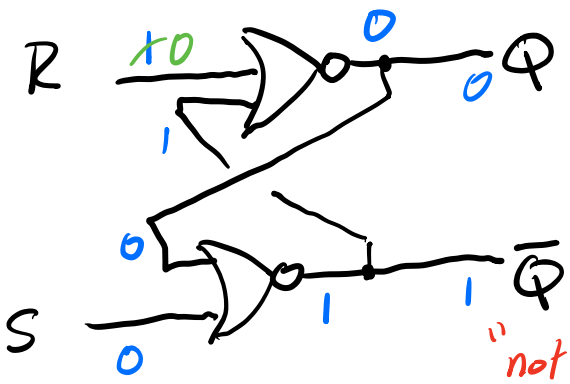
More realistically:



The clock prevents the overwriting of the memory element with the output of the combinational circuit until the computation has finished

Memory Elements (sequential circuits)

"unclocked latch" (aka S-R latch for "Set-Reset")



S=1, R=0 → Q=1, $\bar{Q}$=0

S=0, R=1 → Q=0, $\bar{Q}$=1

S=0, R=0 →

"not Q"

No change

① When Q was 1 and $\bar{Q}$ was 0
→ Q is still 1 and
$\bar{Q}$ is still 0.

② When Q was 0 and $\bar{Q}$ was 1
→ Q is still 0 and
$\bar{Q}$ is still 1.

S=1, R=1 → unstable state
- never used.

When S=0 and R=0, the latch outputs will remain the same
- i.e. their value immediately before S and R both became 0.