Shenzhen Leadtek Technology Co.,Ltd

Approval Sheet

■ **Preliminary specification**

☐ **Final specification**

Customer Name	**xxxxxx**
Product Description	**2.1inch 1200RGB*1200 TFT-LCD Module**
Version	**REV.0**
Supplier	LTK
Module Code	LTK021P69ND

Customer Approval		LTK Approval	
SIGNATURE/TITLE	**DATE**	**SIGNATURE/TITLE**	**DATE**
PREPARED BY		**PREPARED BY**	
_____/_____	_____	_____/_____	_____
REVIEWED BY		**REVIEWED BY**	
_____/_____	_____	_____/_____	_____
APPROVED BY (R&D)		**APPROVED BY (R&D)**	
_____/_____	_____	_____/_____	_____
APPROVED BY (QA)		**APPROVED BY (QA)**	
_____ _/_____	_____	_____ _/_____	_____

Product Specification

Product Name : 2.1" TFT-LCD Module

Model Name : LTK021P69ND

Description : 2.1" 1200RGB×1200 16.7M Color

PREPARED BY	CHECKED BY	APPROVALED BY

Shenzhen Leadtek Technology Co.,Ltd

Revision History

REV.	ECN NO.	DESCRIPTION OF CHANGES	DATE	PREPARED
REV.0	-	Initial Release	2016.11.16	LU Linlin

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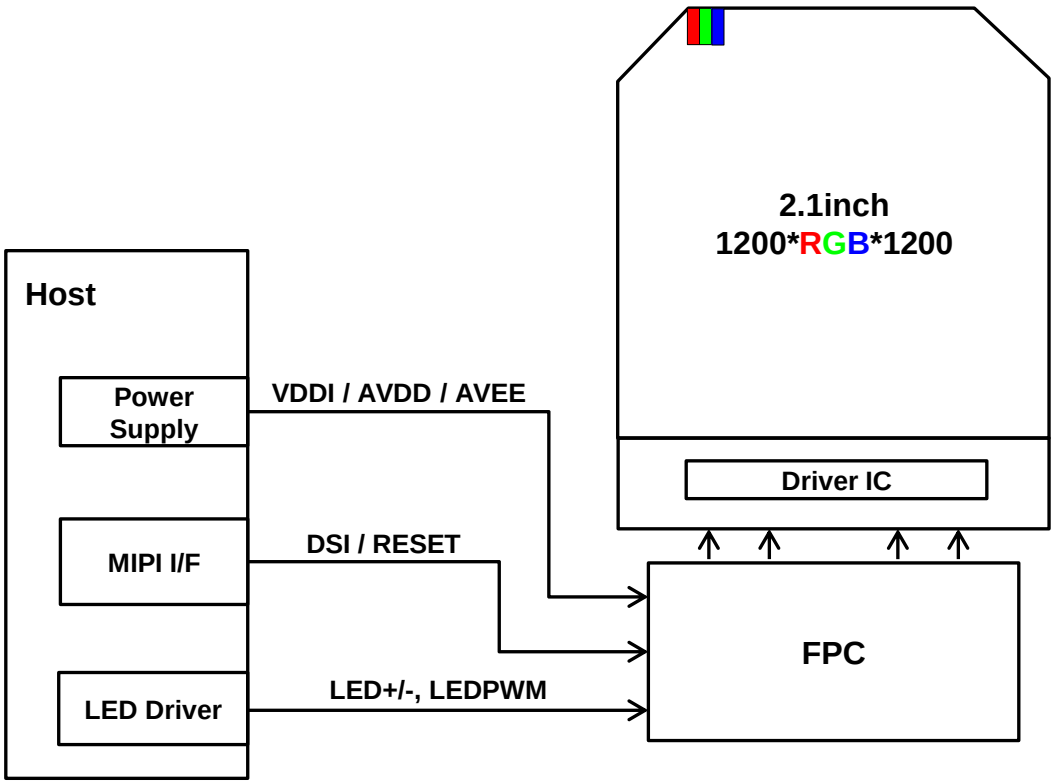
1.0 GENERAL DESCRIPTION

1.1 Introduction

The 2.1inch TFT-LCD Module is a Color Active Matrix TFT LCD panel using LTPS (Low Temperature Poly-silicon) TFT's (Thin Film Transistors) as an active switching devices. This module has a 2.1 inch diagonally measured active area with 1200*1200 resolutions (1200 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M colors. The TFT-LCD panel used for this module is adapted for a low reflection and higher color type.



1.2 Features

- High PPI
- Fast response time
- High frame ratio
- Irregular shape
- High luminance, low reflection and wide viewing angle
- RoHS、Halogen Free Compliant

1.3 Application

- Virtual Reality Device
- Augmented Reality Device

1.4 General Specification

< Table 1. General Specifications >

Parameter	Specification	Unit	Remark
Display method	Active matrix TFT		
Display mode	Transmission mode, Normally black		
Screen size	2.1 (53.46mm)	inch	diagonally
Number of pixels	1200(H) × 1200(V)	pixels	806 ppi
Active area	37.8(H) × 37.8(V)	mm	
Pixel pitch	10.5(H) × 31.5(V)	um	
Pixel arrangement	RGB stripe		
Display colors	16.7M	colors	8bit
NTSC Ratio	72%		
LCM Outline Dimension	41.0(H) × 44.4(V) × 2.36 (T)	mm	Note 1)
LCM Weight	7.55 ±1.0	gram	
Driver IC	NT35598		
Interface	MIPI DSI (Video Mode)		
Surface Treatment	Hardness ≥ 1H		w/ quarter-wave plate

Note:

1) Protection film is not included.

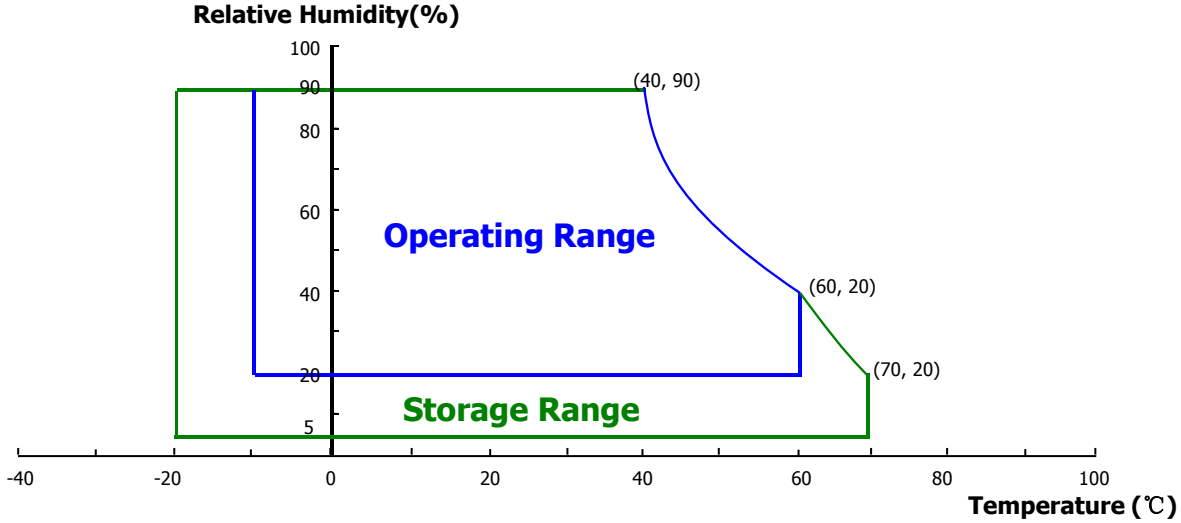
2.0 ABSOLUTE MAXIMUM RATINGS

< Table 2. Absolute Maximum Ratings> [Ta =25±2 ℃]

Items	Symbol	Rating	Unit	Remark
Logic voltage	VDDI	-0.3 to +5.5	V	
Positive Analog Power Supply Voltage	AVDD	-0.3 to +6.6	V	
Negative Analog Power Supply Voltage	AVEE	+0.3 to -6.6	V	
LED forward current	I_{LED}	10	mA	each LED
Storage temperature	T_{STG}	-20 to +70	℃	
Operation temperature	T_{OPR}	-10 to +60	℃	
Humidity (ambient temeprature=Ta)	Ta≤60℃, 90% RH Max.			

Note 1: If the module exceeds the absolute maximum ratings, it may be damaged permanently. Also, if the module operated with the absolute maximum ratings for a long time, its reliability may drop. It is not allowed for any of these ratings to be exceeded. Make sure all the design characte ristics are adequate before the panel is initialed.

Note 2: Temperature and relative humidity range are shown in the figure below.
Wet bulb temperature should be 39 ℃ max. and no condensation of water.



3.0 ELECTRICAL SPECIFICATIONS

3.1 TFT LCD Panel

< Table 3. LCD Panel Electrical Specifications > [Ta =25±2 ℃]

Items		Symbol	Min.	Typ.	Max.	Unit	Remark
Logic voltage		VDDI	1.65	1.8	3.6	V	Note 1
Positive Analog Power Supply Voltage		AVDD	4.5	5.5	6.0	V	
Negative Analog Power Supply Voltage		AVEE	-4.5	-5.5	-6.0	V	
Frame Ratio		FPS	-	90	120	Hz	
Input signal voltage	High level	V_{IH}	0.7×VDDI	-	VDDI	V	
	Low level	V_{IL}	VSSI	-	0.3×VDDI	V	
Output signal voltage	High level	V_{OH}	0.8×VDDI	-	VDDI		
	Low level	V_{OL}	VSSI	-	0.2×VDDI		
Current consumption		I_{VDDI}		24.0	28.0	mA	Note 2
		I_{AVDD}		7.0	9.0	mA	
		I_{AVEE}		7.0	9.0	mA	
Driver IC ESD		HBM	- 2	-	+2	kV	
		MM	-200	-	+200	V	

Note 1:
The value can be adjusted by software to optimize display quality.
The operation is guaranteed under the recommended operating conditions only. The operation is not guaranteed if a quick voltage change occurs during operation. To prevent noise, a bypass capacitor must be inserted into the line close to power pin. Please make sure all the design settings are used within this range before the panel is initialed.

Note 2:
Test pattern: All White Display

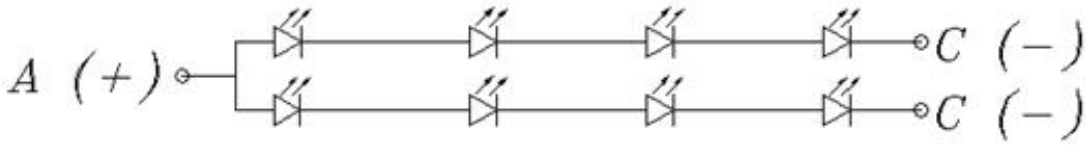
3.2 Back-light Unit

< Table 4. LED Driving Specifications > Ta=25+/-2°C

Items	Symbol	Min.	Typ.	Max.	Unit	Remark
Forward Current	If	-	10	20	mA	Note1
Forward Voltage	Vf	-	6	6.4	V	Note1
Power Consumption	P_{BL}	-	480	960	mW	Note2
LED Q'ty		8			ea	

Note 1: The driving condition is defined for each LED chip.
Note 2: The B/L power consumption is defined for the backlight module.
the schematic drawing of the backlight unit is as the figure.

Ref. Total power consumption(max) depends on LED current/LED driver efficiency, etc.



Back-Light Circuit

4.0 OPTICAL SPECIFICATION

4.1 Overview

The optical characteristics should be measured in a dark room (ambient luminance≦ 1 lux and temperature = 25±2℃) with the equipment of Konica Minolta CA-310 and CS-2000 and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0° . The center of the measuring spot on the display surface should stay fixed.

The operation should be under the recommended operating conditions.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Item		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle	Horizontal	θ_3	CR > 10	70	85	-	degree	Note 1
		θ_9		70	85	-		
	Vertical	θ_{12}		70	85	-		
		θ_6		70	85	-		
Color Gamut (NTSC)				65	72	-	%	
Contrast Ratio		CR	θ = 0°	300	500	-		Note 2
Luminance of White	Center	Y_w	θ = 0°	650	800	-	cd/m^2	Note 3
Luminance Uniformity	5 Points	ΔY5		80%	-	-		Note 4
Chromaticity (CIE 1931)	Red	Rx	θ = 0°	0.600	0.630	0.660		Note 5
		Ry		0.325	0.355	0.385		
	Green	Gx		0.300	0.330	0.360		
		Gy		0.595	0.625	0.655		
	Blue	Bx		0.120	0.150	0.180		
		By		0.045	0.075	0.105		
	White	Wx		0.260	0.290	0.320		
		Wy		0.285	0.315	0.345		
Response Time (G to G)		T	θ = 0°	-	-	8	ms	Note 6
Flicker				-	-	-30	db	Note 7
Cross Talk		CT	θ = 0°	-	-	2	%	Note 8

Note 1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (FIGURE 1).

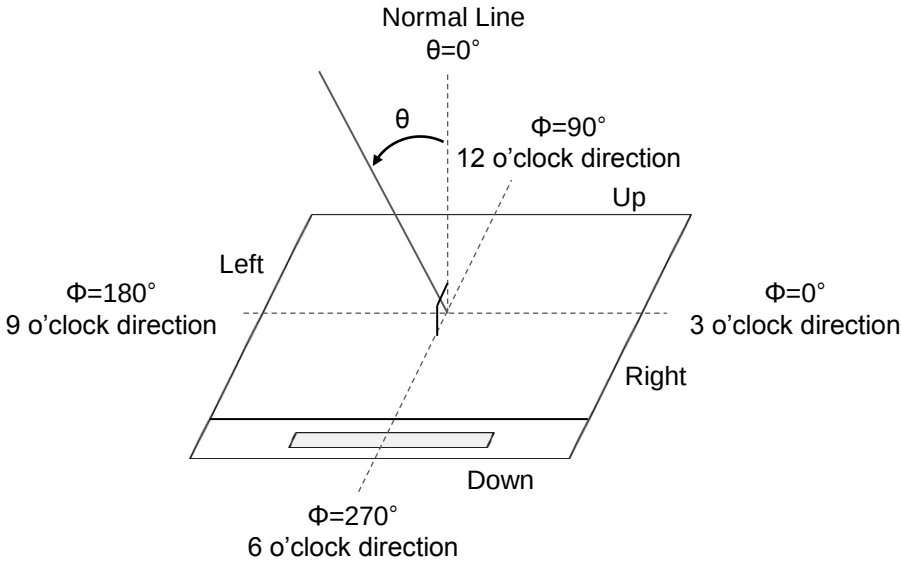


Fig.1 Viewing angle measurement setup

Note 2. Contrast ratio measurements shall be made at viewing angle of θ=0° and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state (FIGURE 1).
Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

Note 3. Luminance of white is defined as luminance values of the center point across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in FIGURE 2 for a total of the measurements per display. The luminance is measured by CA310 when the LED current is set at 10mA/ea.

Note 4. The White luminance uniformity is then expressed as:
ΔY = Minimum Luminance of 5 points / Maximum Luminance of 5points (FIGURE 3).

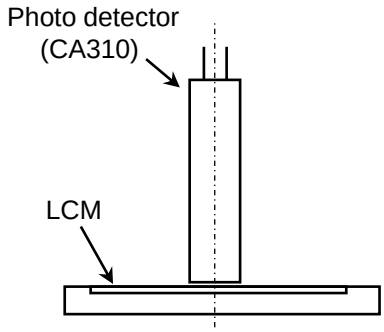


Fig.2 Luminance, uniformity & chromaticity measurement setup

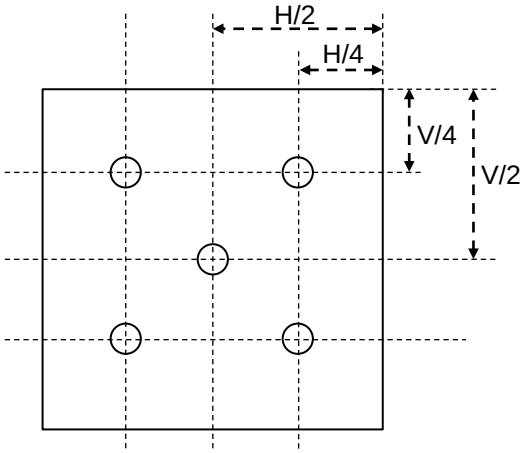


Fig.3 Luminance uniformity measurement setup

Note 5. The color chromaticity is measured with all pixels first in red, green, blue and white. Measurements should be made at the center of the panel.

Note 6. Definition of Response time.

The output signals of photo detector are measured when the input signals are switched between different display pattern (Gray-to-Gray).

The response time is defined as the time interval between the 10% and 90% of amplitudes (Fig.4)

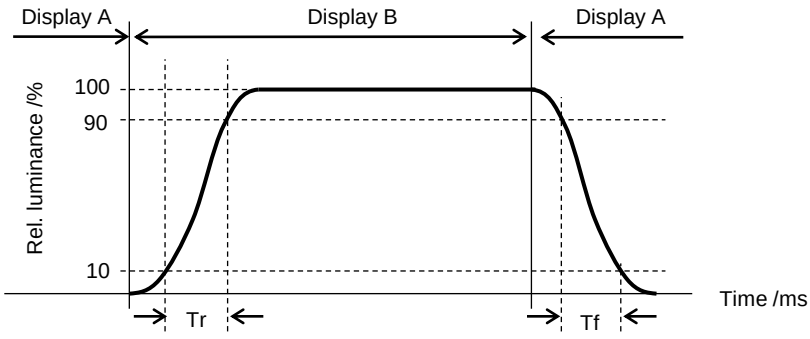


Fig.4 Response Time

Note 7. Flicker

Test equipment: CA310
Test pattern: column inversion (Fig.5)

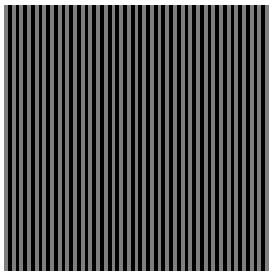


Fig.5 Flicker pattern

Note 8. Cross Talk

Test pattern: Fig.6

$$X - talk = maximum\left(\frac{Y1 - Y1'}{Y1}, \frac{Y2 - Y2'}{Y2}, \frac{Y3 - Y3'}{Y3}, \frac{Y4 - Y4'}{Y4}\right)$$

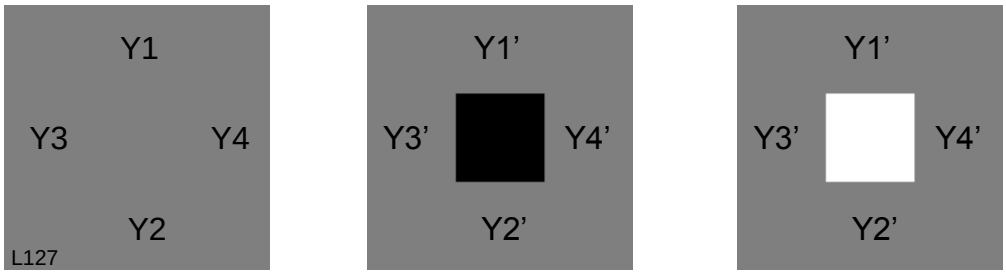


Fig.6 Cross-talk pattern

5.0 INTERFACE CONNECTION

The electronics interface connector is **AXE650124.**
The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

NO.	Symbol	Description	NO.	Symbol	Description
1	GND	Ground	26	GND	Ground
2	VDDI	Power Supply for Digital Circuits	27	LED-2	LED Backlight Negative Power Supply
3	GND	Ground	28	LED-1	LED Backlight Negative Power Supply
4	GND	Ground	29	GND	Ground
5	GND	Ground	30	LED+	LED Backlight Positive Power Supply
6	DSIB_D2_P	MIPI-DSI Data Lane	31	GND	Ground
7	DSIB_D2_N	MIPI-DSI Data Lane	32	DSIA_D3_N	MIPI-DSI Data Lane
8	GND	Ground	33	DSIA_D3_P	MIPI-DSI Data Lane
9	DSIB_CLK_P	MIPI-DSI Clock Lane	34	GND	Ground
10	DSIB_CLK_N	MIPI-DSI Clock Lane	35	DSIA_CLK_N	MIPI-DSI Clock Lane
11	GND	Ground	36	DSIA_CLK_P	MIPI-DSI Clock Lane
12	DSIB_D3_P	MIPI-DSI Data Lane	37	GND	Ground
13	DSIB_D3_N	MIPI-DSI Data Lane	38	DSIA_D2_N	MIPI-DSI Data Lane
14	GND	Ground	39	DSIA_D2_P	MIPI-DSI Data Lane
15	DSIA_D1_P	MIPI-DSI Data Lane	40	GND	Ground
16	DSIA_D1_N	MIPI-DSI Data Lane	41	DSIB_D0_N	MIPI-DSI Data Lane
17	GND	Ground	42	DSIB_D0_P	MIPI-DSI Data Lane
18	DSIA_D0_P	MIPI-DSI Data Lane	43	GND	Ground
19	DSIA_D0_N	MIPI-DSI Data Lane	44	DSIB_D1_N	MIPI-DSI Data Lane
20	GND	Ground	45	DSIB_D1_P	MIPI-DSI Data Lane
21	RESX	Global Reset signal	46	GND	Ground
22	TE	Tearing Effect	47	AVEE	Negative Power Supply
23	HSYNC	Line Synchronies	48	AVDD	Positive Power Supply
24	LEDPWM	LED Backlight Control PWM Output PIN	49	IM0	Interface type selection
25	GND	Ground	50	GND	Ground

Remark:
IM0: 1 port or 2 port selection pin.
When IM0 is connected to “low”, only port A is valid, and meanwhile, port B must be directly connected to “low”;
When IM0 is connected to “high”, port A and B are valid.

VDDI is defined as “H” level and GND is defined as “L” level.

6.0 Block Diagram

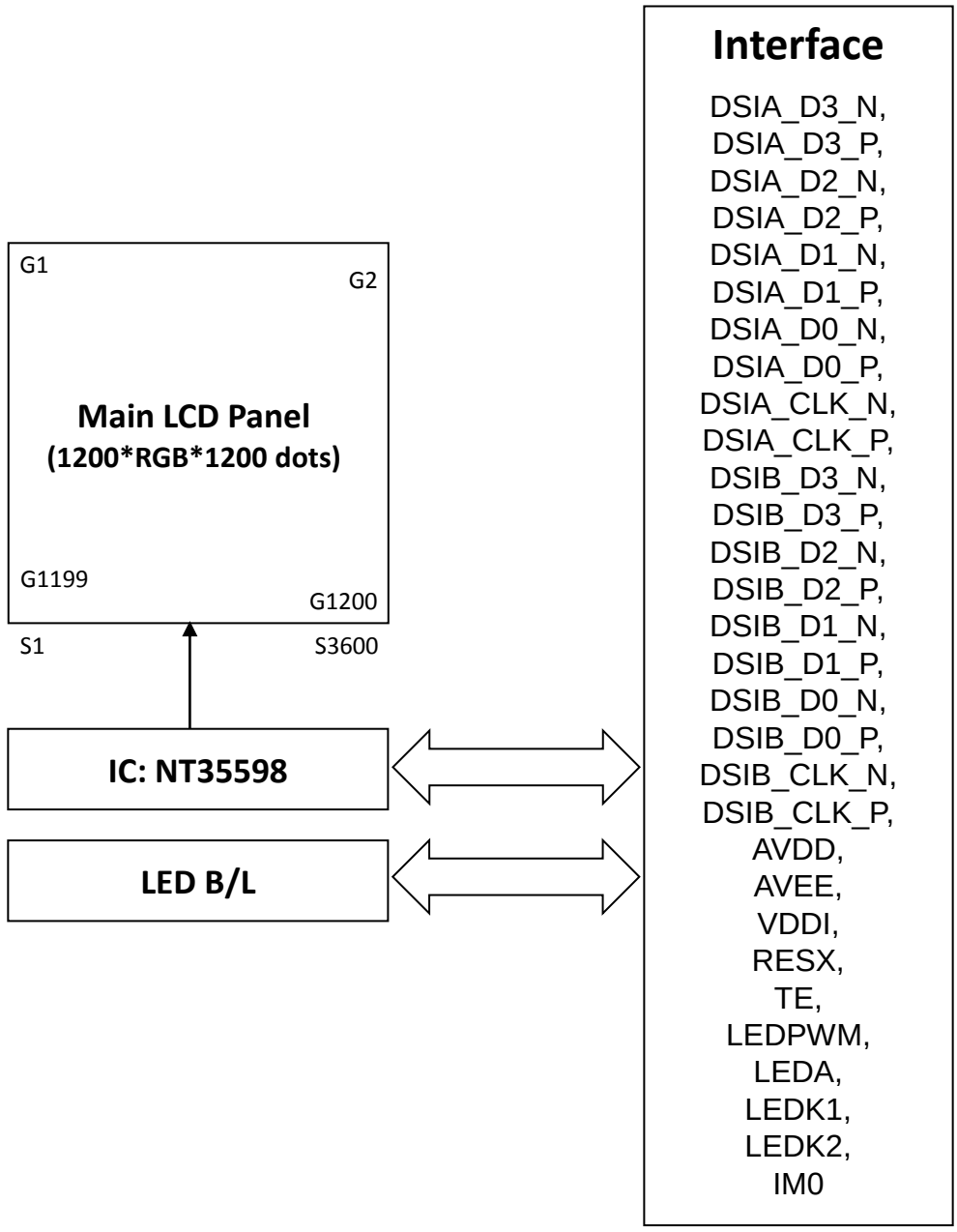


Figure 5. Block diagram

7.0 Timing Characteristics

7.1 Power On/Off Sequence

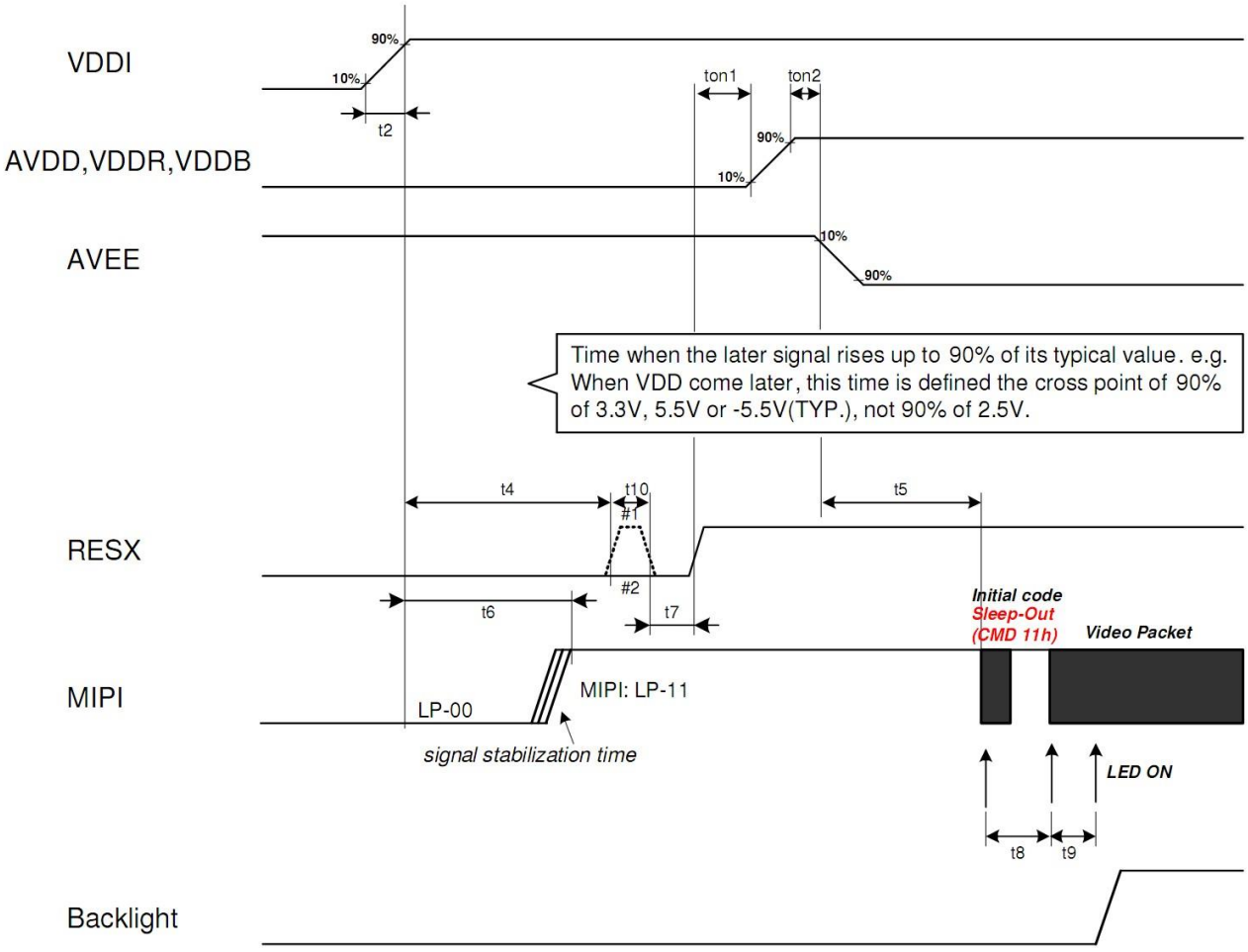
VDDI must be applied in advance of other Powers (AVDD/AVEE).
Analog powers (AVEE/AVDD) must be powered down in advance of VDDI or at the same time.
During power off, if LCD is in the Sleep Out mode, Analog Powers (AVDD/AVEE) and VDDI must be powered down minimum 120msec after RESX has been released.
During power off, if LCD is in the Sleep In mode, VDDI or Analog Powers (AVDD/AVEE) can be powered down minimum 0msec after RESX has been released.

Notes:
1. There will be no abnormal visible effects on the display panel during the Power On/Off Sequences.
2. There will be no abnormal visible effects on the display between end of Power On Sequence and before receiving Sleep Out command. Also between receiving Sleep In command and Power Off Sequence.

■ Power On Sequence

If RESX line is held High or unstable by the host during Power On, then a Hardware Reset must be applied after both VDD and VDDI have been applied – otherwise correct functionality is not guaranteed. There is no timing restriction upon this hardware reset.
If RESX line is held Low (and stable) by the host during Power On, then the RESX must be held low for minimum 10µsec after both VDD and VDDI have been applied.
The power on sequence for different power input modes are shown below figures.

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
ton1	5	-	-	ms	Schottky diode should add on VGLX-AVEE (3/4/5 power mode) VGLX-GND (2 power mode)
ton2	2	-	-	ms	
ton3	0	-	-	ms	
ton4	0	-	-	ms	
t2	-	-	150	us	
t4	10	-	-	ms	
t5	5	-	-	ms	
t6	0	-	t4	ms	
t7	10	-	-	us	
t8	120	-	-	ms	
t9	0	No limit	-	ms	
t10	5	-	-	ms	



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

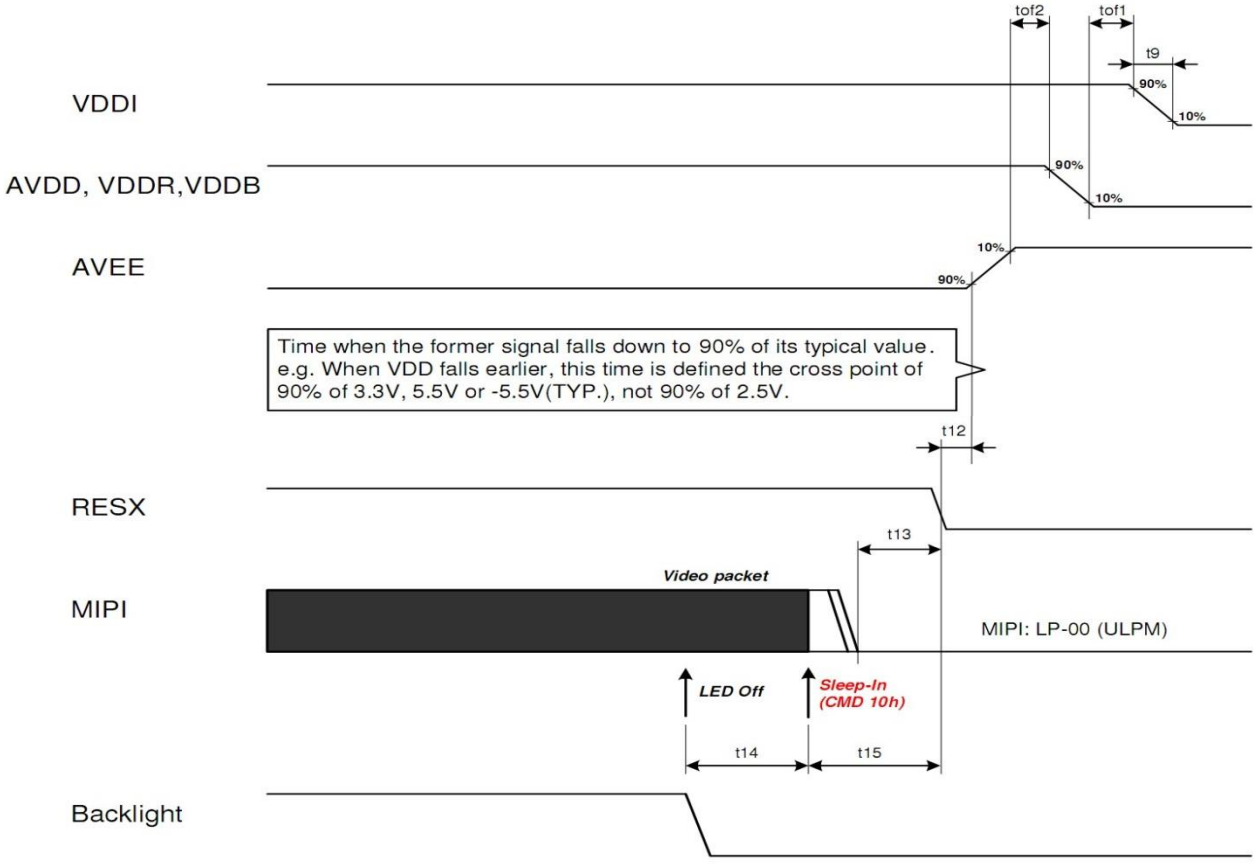
Note 2: This power-on sequence is based on adding Schottky diode on VGLX pin to ground .

Note 3: Reset signal H to L to H (#1) is better than only L to H (#2).

Note 4: If the MIPI signal can go to LP-11 before reset (low to high), the second low pulse doesn't need. The second low pulse is used to clear "False Control Error" if MIPI signal doesn't keep to LP-11 before reset.

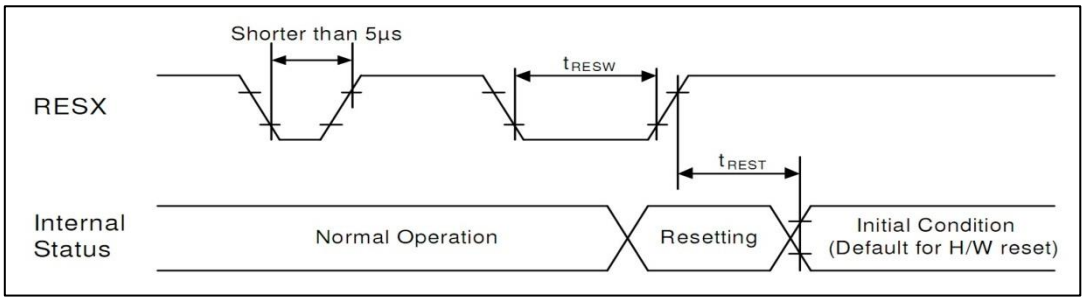
■ **Power Off Sequence**

Symbol	Value			Unit	Remark
	Min.	Typ.	Max.		
t9	-	No limit	-	us	
tof1	2	-	-	ms	
tof2	2	-	-	ms	Schottky diode for VGL-AVEE should be connected
tof3	0	-	-	ms	
tof4	0	-	-	ms	
t12	0	-	-	ms	
t13	0	-	-	ms	
t14	0	-	-	ms	
t15	100			ms	



Note 1: Unless otherwise specified, timings herein show cross point at 50% of signal/power level.

7.2 Reset Input Timing



(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	t_{RESW}	Reset "L"pulse width (Note 1)	10	-	-	us	
	t_{REST}	Reset complete time (Note 2)	-	-	5	ms	When reset applied during Sleep In Mode
			-	-	120	ms	When reset applied during Sleep Out Mode and Note 5

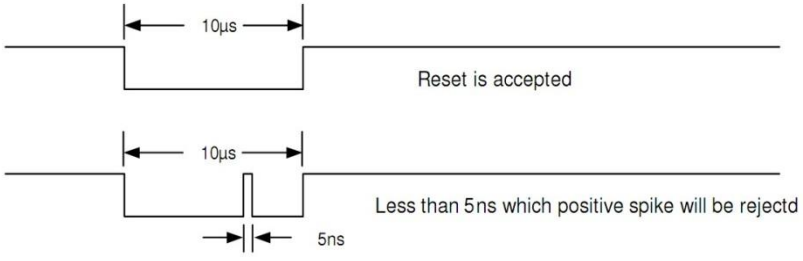
Note 1) Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below.

RESX Pulse	*Action*
Shorter than 5µs	*Reset Rejected*
Longer than 10µs	*Reset*
Between 5µs and 10µs	*Reset Start*

Note 2) During the resetting period, the display will be blanked (The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep Out –mode. The display remains the blank state in Sleep In–mode) and then return to Default condition for H/W reset.

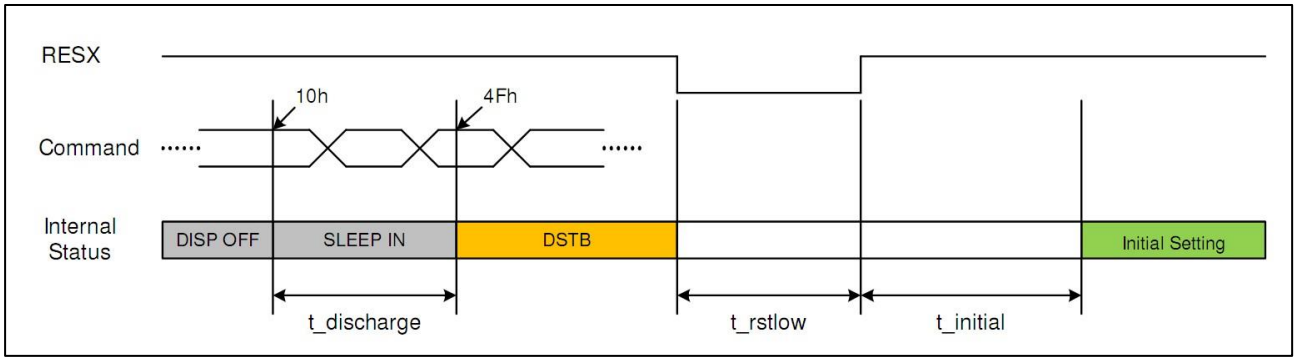
Note 3) During Reset Complete Time, values in OTP memory will be latched to internal register during this period. This loading is done every time when there is H/W reset complete time (t_{REST}) within 5ms after a rising edge of RESX.

Note 4) Spike Rejection also applies during a valid reset pulse as shown below:



Note 5) It is necessary to wait 5msec after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120msec

7.3 Deep Standby Mode Timing



(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
RESX	$t_{\_discharge}$	Sleep in into DSTB delay time	100	-	-	ms	
	$t_{\_rstlow}$	Reset low pulse	3	-	-	ms	
	$t_{\_initial}$	Reset high to initial setting delay time	120	-	-	ms	

7.4 MIPI Interface Characteristics

7.4.1 High Speed Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-CLK+/-	$2xUI_{INST}$	Double UI instantaneous	2	-	5	ns	4 Lane (Note 2)
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halfs ($UI = UI_{INSTA} = UI_{INSTB}$)	1	-	2.5	ns	4 Lane (Note 2)
DSI-Dn+/-	t_{DS}	Data to clock setup time	0.15xUI	-	-	ps	
DSI-Dn+/-	t_{DH}	Data to clock hold time	0.15xUI	-	-	ps	
DSI-CLK+/-	t_{DRTCLK}	Differential rise time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DRTDATA}$	Differential rise time for data	150	-	0.3xUI	ps	
DSI-CLK+/-	t_{DFTCLK}	Differential fall time for clock	150	-	0.3xUI	ps	
DSI-Dn+/-	$t_{DFTDATA}$	Differential fall time for data	150	-	0.3xUI	ms	

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Maximum total bit rate is 4Gbps for 24-bit data format, 3Gbps for 18-bit data format and 2.67Gbps for 16-bit data format for both two DSI ports (4x2 lanes) application which support to 1600RGBx 2560 resolution.

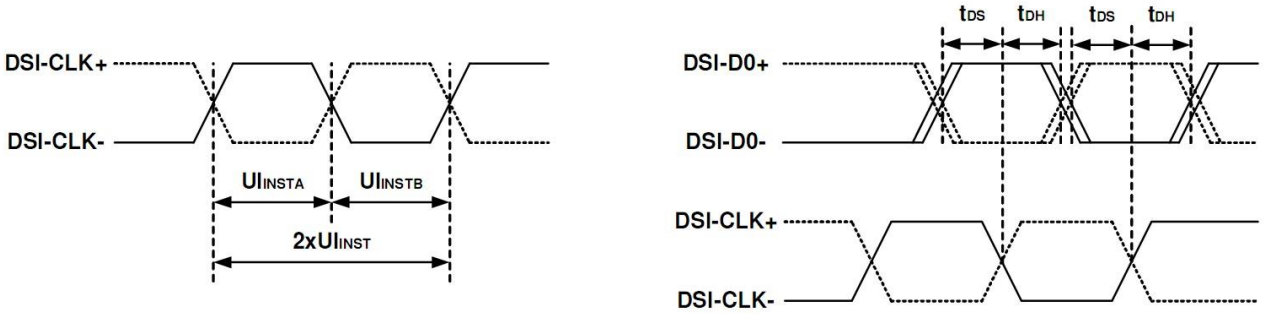


Fig.7.4.1 DSI clock channel timing

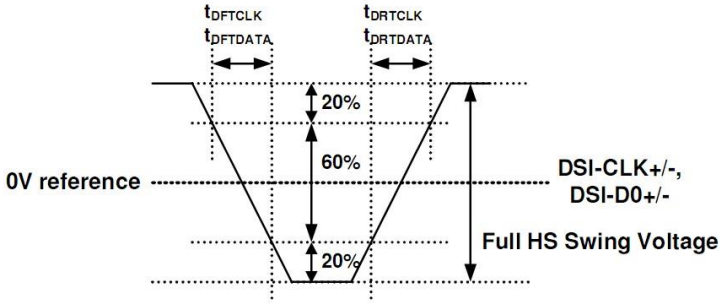


Fig.7.4.2 Rising and fall time on clock and data channel

7.4.2 Low Speed Mode

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP-11 periods MPU Display Module	50	-	75	ns	Input
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP-11 periods Display Module MPU	50	-	75	ns	Output
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T_{LPXD}	-	$2xT_{LPXD}$	ns	Output
DSI-D0+/-	$T_{TA-GETD}$	Time to drive LP-00 by display module	$5xT_{LPXD}$	-	-	ns	Input
DSI-D0+/-	T_{TA-GOD}	Time to drive LP-00 after turnaround request - MPU	$4xT_{LPXD}$	-	-	ns	Output

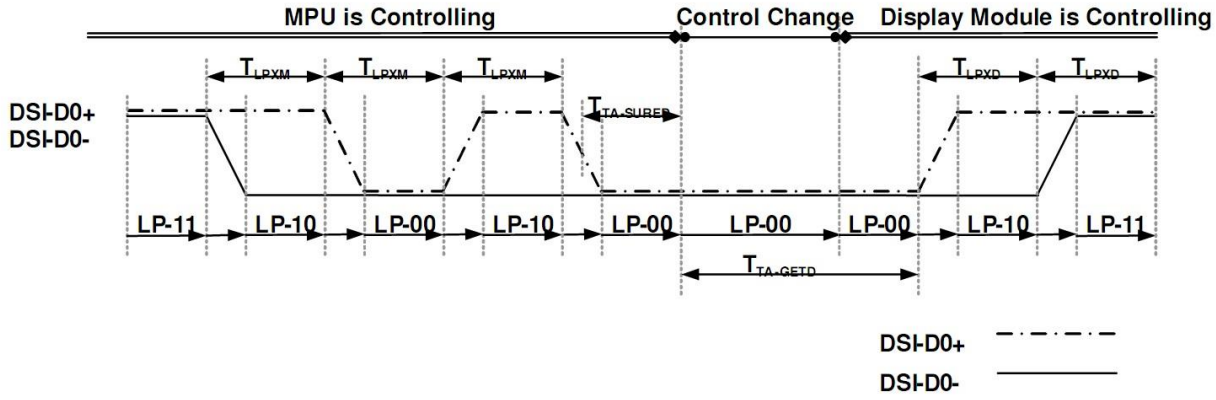


Fig.7.4.3 Bus Turnaround (BTA) from MPU to display module Timing

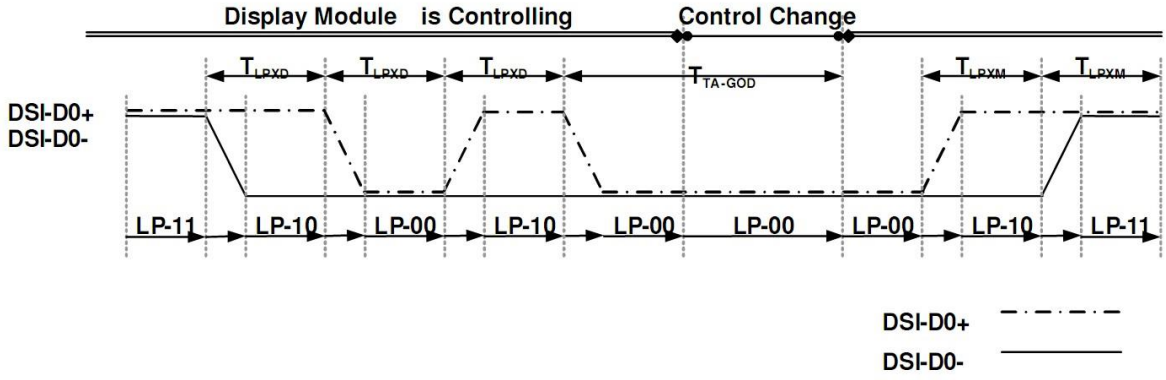


Fig.7.4.4 Bus Turnaround (BTA) from display module to MPU Timing

7.4.3 DSI Bursts

(VSS=VSSI=DVSS=0V, VDDI=1.65V to 3.6V, VDD=2.5V to 3.6V,Ta = -30 to 70°C)

Signal	Symbol	Parameter	MIN	TYP	MAX	Unit	Description
Low Power Mode to High Speed Mode Timing							
DSI-Dn+/-	T_{LPX}	Length of any low power state period	50	-	-	ns	Input
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	40+4xUI	-	85+6xUI	ns	Input
DSI-Dn+/-	$T_{HS-TERM-EN}$	Time to enable data receiver line termination measured from when Dn crosses V_{ILMAX}	-	-	35+4xUI	ns	Input
High Speed Mode to Low Power Mode Timing							
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at display module to ignore transition period of EoT	40	-	55+4xUI	ns	Input
DSI-Dn+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to drive flipped differential state after last payload data bit of a HS transmission burst	60+4xUI	-	-	ns	Input
High Speed Mode to/from Low Power Mode Timing							
DSI-CLK+/-	$T_{CLK-POS}$	Time that the MPU shall continue sending HS clock after the last associated data lane has transition to LP mode	60+52xUI	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to drive HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns	Input
DSI-CLK+/-	$T_{HS-EXIT}$	Time to drive LP-11 after HS burst	100	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to drive LP-00 to prepare for HS transmission	38	-	95	ns	Input
DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time-out at clock lane display module to enable HS transmission	-	-	38	ns	Input
DSI-CLK+/-	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	Minimum lead HS-0 drive period before starting clock	300	-	-	ns	Input
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated data lane beginning the transition from LP to HS mode	8xUI	-	-	ns	Input

Note 1) Dn = D0, D1, D2 and D3.

Note 2) Two HS transmission can be sent with a break as short as THS-EXIT from each other in continuous clock mode. In discontinuous mode, the break is longer which account TCLK-POS, TCLK-TRAIL and THS-EXIT, before activity in clock and data lanes again.

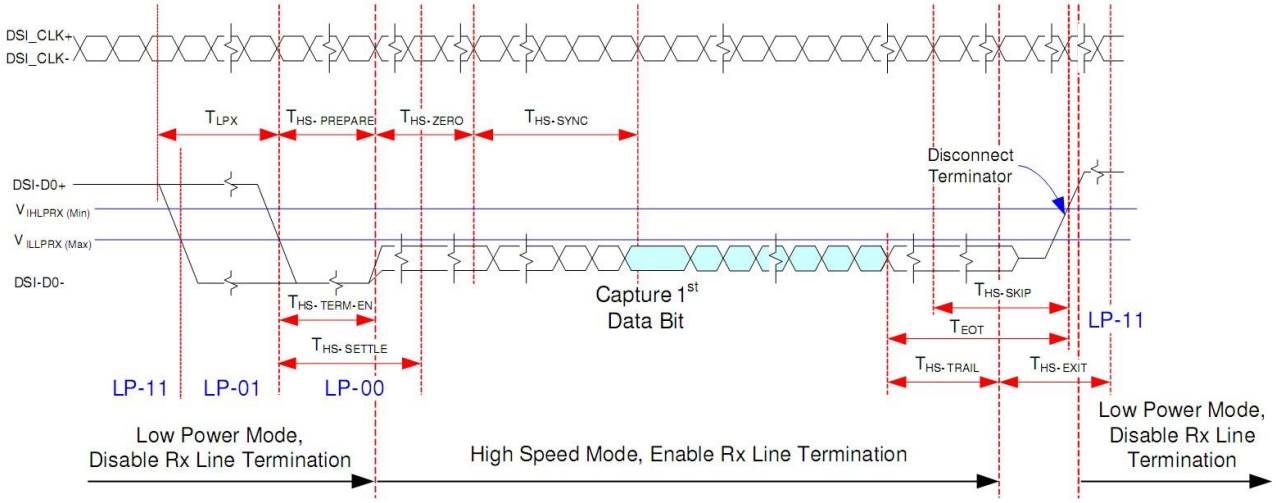


Fig.7.4.5 Data lanes-Low Power Mode to/from High Speed Mode Timing

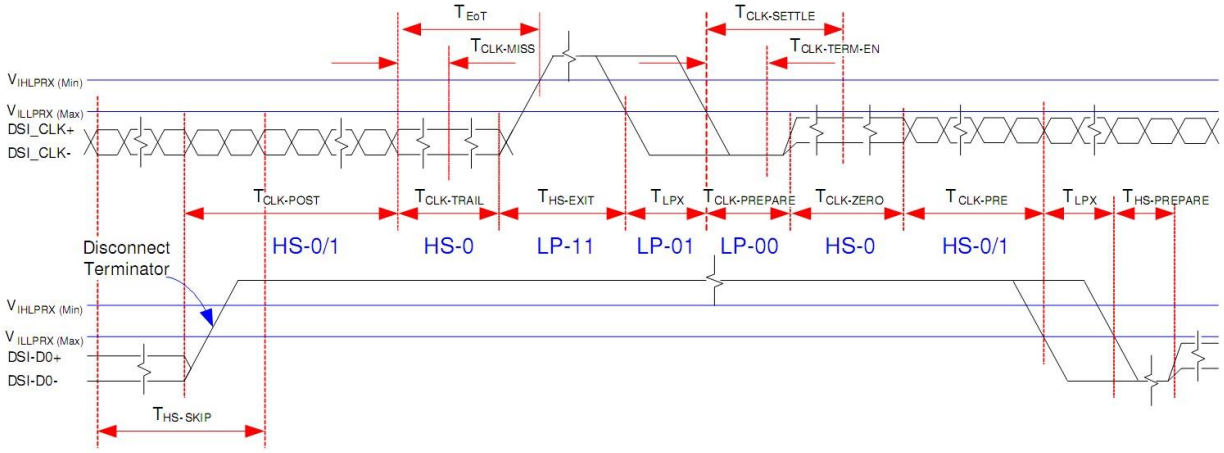
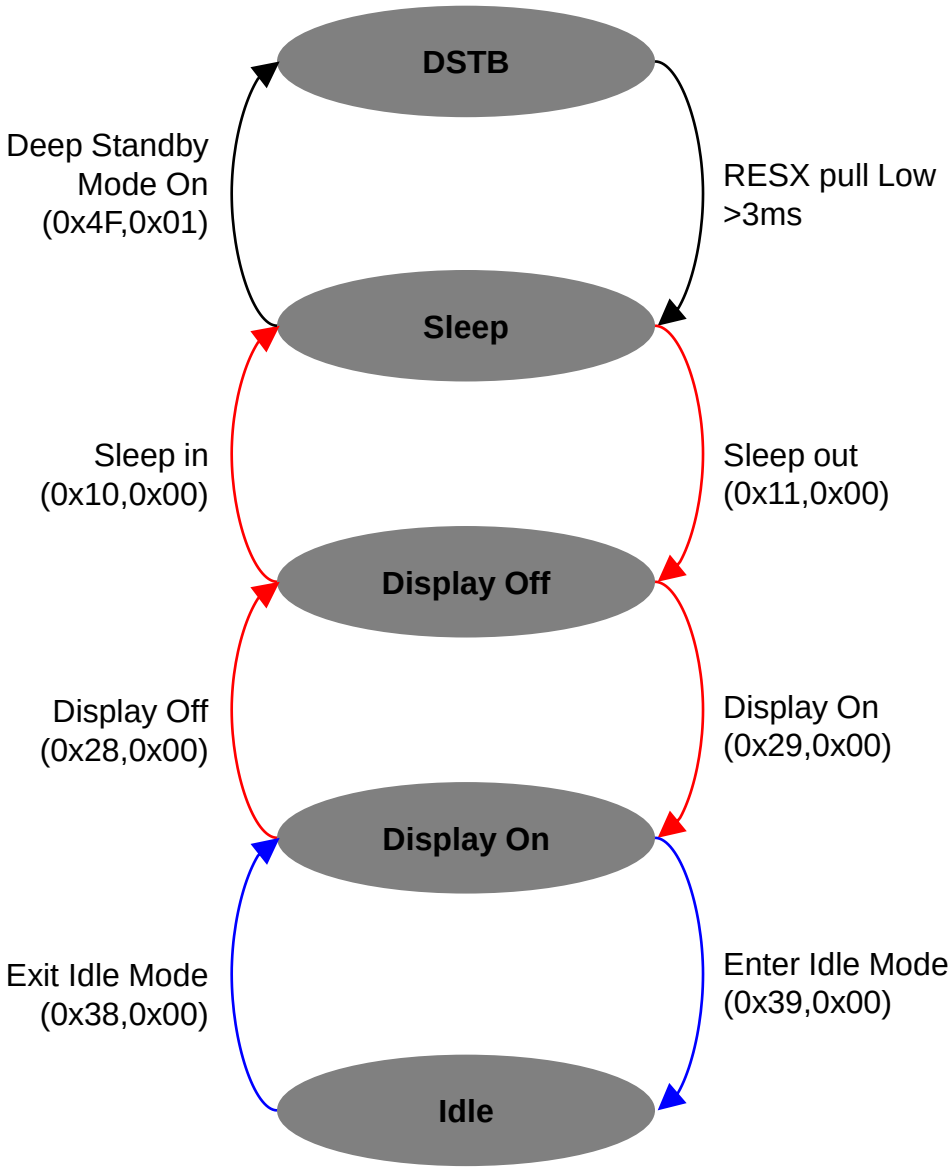


Fig.7.4.6 Clock lanes-High Speed Mode to/from Low Power Mode Timing

7.5 Operating Sequence (for reference only)

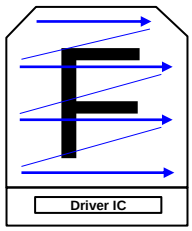
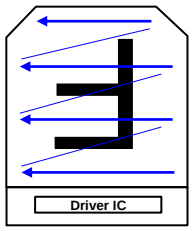


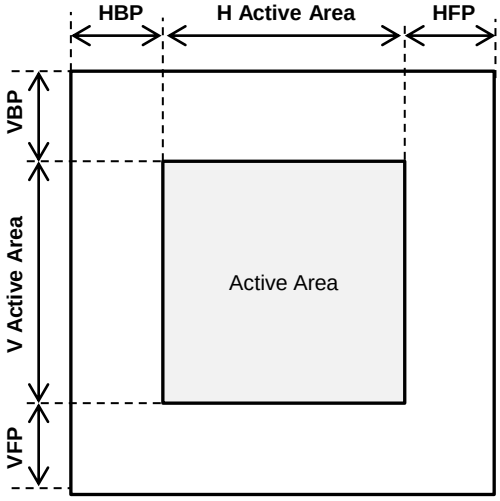
7.6 Initial Code Setting

☐ Speed & Porch Setting (for reference only)

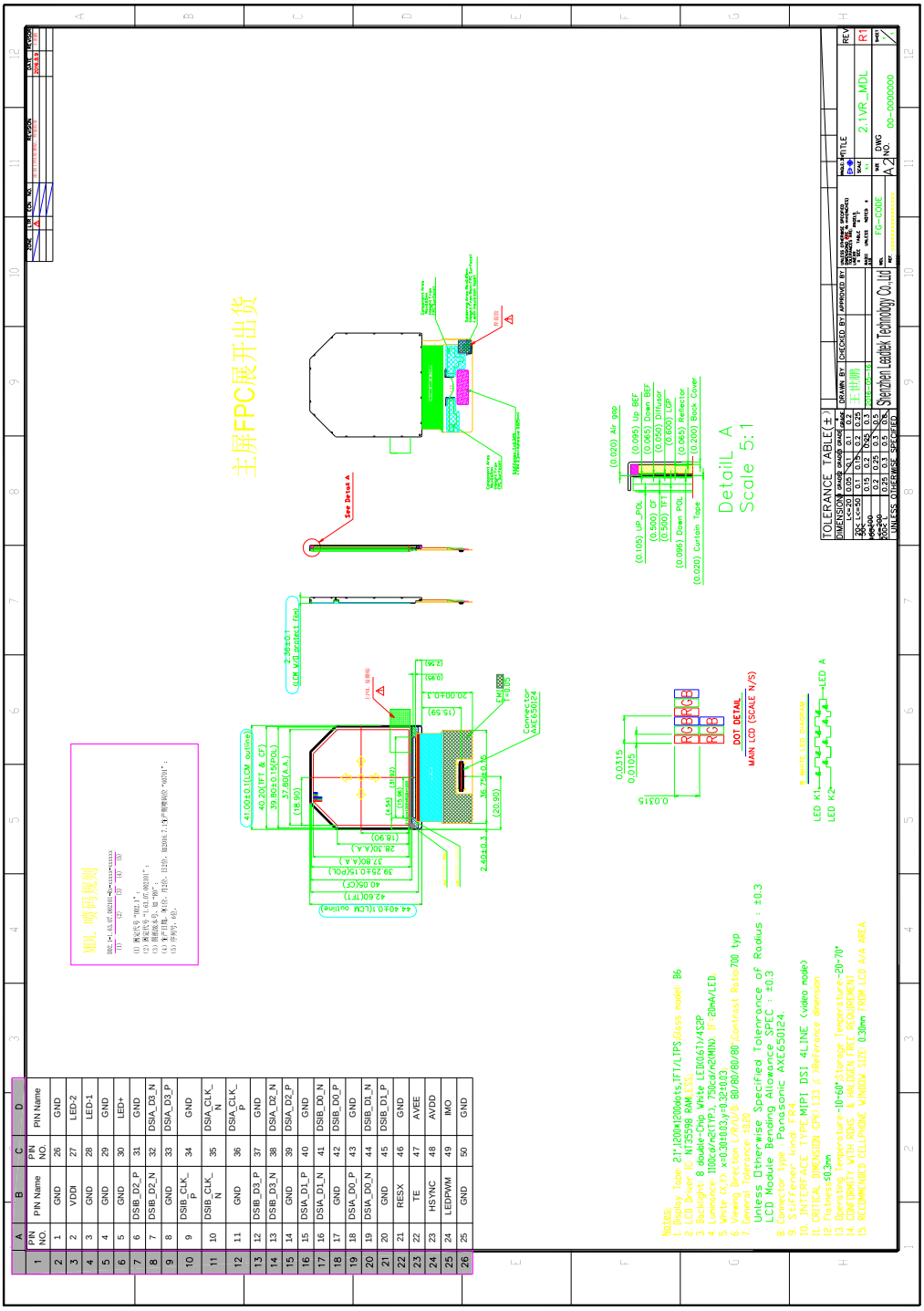
Item			Symbol	Min.	Typ.	Max.	Unit
Speed	Frame Rate		-	-	90	120	Hz
	Line Time		-	-	9.02	-	us
	Dot CLK		-	-	146	-	MHz
	MIPI Speed		-	-	878	-	Mbps
Porch	Horizontal	Horizontal total time	Htotal	-	1320	-	dot
		Horizontal Active time	Hactive		1200		dot
		Horizontal Pulse Width	Hsync	-	-	-	dot
		Horizontal Back Porch	HBP	-	60	-	dot
		Horizontal Front Porch	HFP	-	60	-	dot
	Vertical	Vertical Total	Vtotal	-	1232	-	line
		Vertical Active	Vactive		1200		line
		Vertical Pulse Width	Vsync	-	-	-	line
		Vertical Back Porch	VBP	-	16	-	line
		Vertical Front Porch	VFP	-	16	-	line
Lane				-	4	8	Lane

☐ Display Scan Direction

	Data Direction	B1h
正向 扫描		01h
反向 扫描		07h



8.0 MECHANICAL CHARACTERISTICS



P/N NO.	B P/N Name	C P/N NO.	D P/N Name
1	GND	26	GND
2	VDDI	27	LED-2
3	GND	28	LED-1
4	GND	29	GND
5	GND	30	LED+
6	DSIB_D2_P	31	GND
7	DSIB_D2_N	32	DSIA_D3_N
8	GND	33	DSIA_D3_P
9	DSIB_CLK_P	34	GND
10	DSIB_CLK_N	35	DSIA_CLK_N
11	GND	36	DSIA_CLK_P
12	DSIB_D3_P	37	GND
13	DSIB_D3_N	38	DSIA_D2_N
14	GND	39	DSIA_D2_P
15	DSIA_D1_P	40	GND
16	DSIA_D1_N	41	DSIB_D0_N
17	GND	42	DSIB_D0_P
18	DSIA_D0_P	43	GND
19	DSIA_D0_N	44	DSIB_D1_N
20	GND	45	DSIB_D1_P
21	RESX	46	GND
22	TE	47	AVEE
23	HSYNC	48	AVDD
24	LEDPWM	49	IMO
25	GND	50	GND
26			

9.0 RELIABILITY TEST

The Reliability test items and its conditions are shown in below.

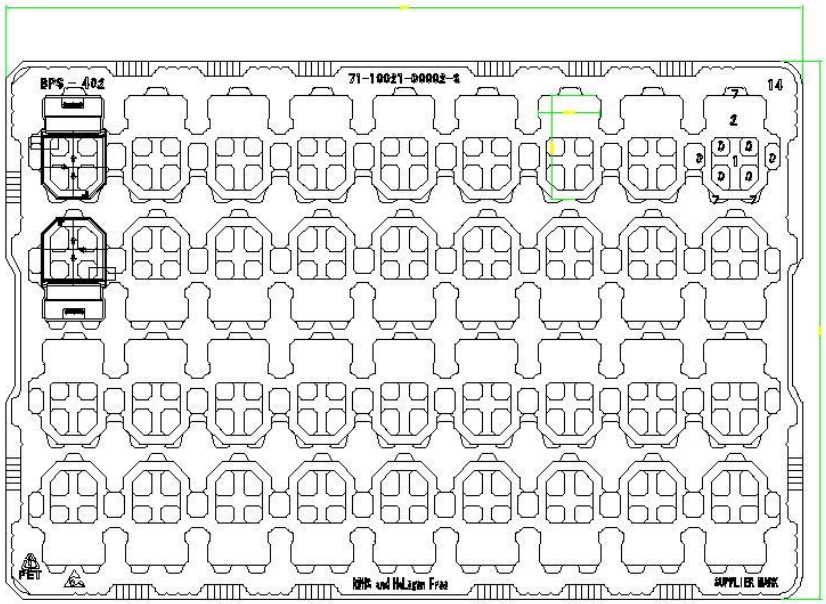
<Table 7. Reliability Test Conditions>

No.	Test Items	Conditions
1	High temperature storage	Ta = 70 ℃, 48 hrs
2	Low temperature storage	Ta = -20℃, 48 hrs
3	High temperature & high humidity operation test	Ta = 60 ℃, 90%RH, 48hrs
4	High temperature operation	Ta = 60 ℃, 48 hrs
5	Low temperature operation	Ta = -10 ℃, 48 hrs

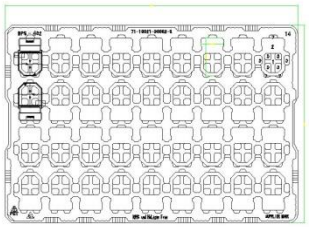
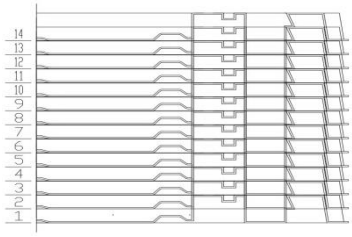
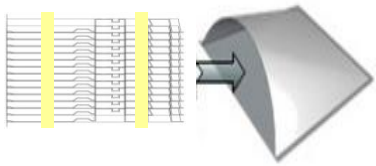
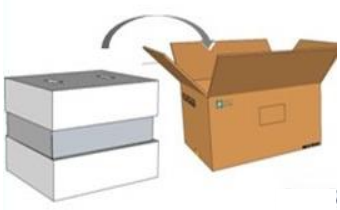
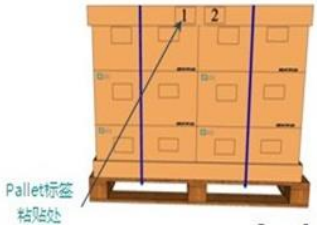
10.0 PACKING INFORMATION

10.1 Packing Description

No.	Description	Quantity	Size (mm)
1	LCM per Box	936 pcs	
2	LCM per Tray	36 pcs	
3	PET Tray	28 ea (2ea empty)	507(L) × 343(W)
4	Antistatic Air Bubble Bag	2 ea	700(L) × 510(W)
5	Pulp Molding Pad	2 ea	629(L) × 465(W)
6	Out Box	1 ea	545(L)×380(W)×270(H)
7	Belt tape	56.5 cm	
8	Distribution label	1 ea	



10.2 Packing Procedure

将LCM放入Tray中 36 pcs LCM /Tray	将盛装LCM的Tray码叠13层，然后加放1个空Tray做盖子（每个Tray之间需互转180°）。 468pcs LCM /13Tray	将捆绑后的Tray放入一个气泡袋
 **Step 1**	 **Step 2**	 **Step 3**
每2个打包后的气泡袋叠放在一起，然后上下各扣一个纸浆垫，并放入Box	采用“H”型封箱方式，对Box进行封箱，并在Box的Mark处粘贴外箱标签， 936pcs LCM/Box	按“田”字型码拍 12 Box/Pallet
 **Step 4**	 **Step 5**	 **Step 6**
套上dual cover 和 paper corner，并用打包带打包		
 **Step 7**		

11.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose Power, DSI signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc., Please pack the module not to be broken.
- We recommend to use the original shipping packages.