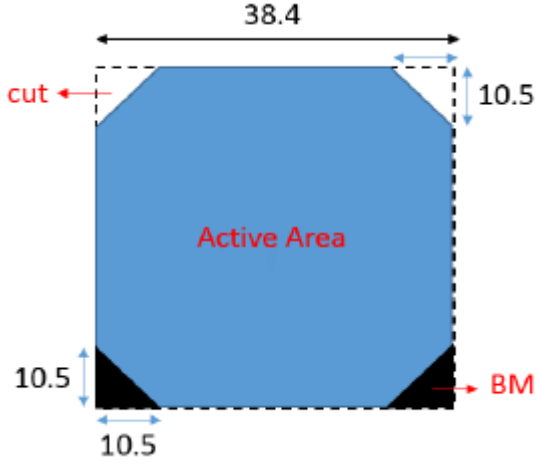
BOE 2.1” 1600 General Spec

	2.1”
Resolution	1600*1600 1058PPI(RGB Stripe)
Active Area (H*V mm)	38.4*38.4
Response Time (ms)	5.5ms MAX (G to G 10%-90%)
Frame Rate (Hz)	90Hz
Brightness (nits)	500nits 20% BL Duty
Contrast Ratio (typical)	700:1
Color Gamut (NTSC)	70%
Module Outline (mm)	41.2(H)*45.3(V)*1.8(T)
BLU Power (mW 20% Duty)	468
Driver IC	R63455



BOE 2.1” 1600 General Spec

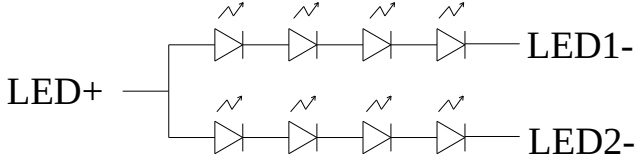
Connector:145863050024829+					
NO.	**Symbol**	**Description**	**NO.**	**Symbol**	**Description**
1	GND	Ground	**2**	NC	No Connection
3	PNSLV	Main port select	**4**	VSP	Positive power
5	BLUPWM	BLU duty control	**6**	NC	No Connection
7	TE	TE signal output	**8**	VSN	Negative power
9	RESET	DDIC reset signal	**10**	GND	Ground
11	GND	Ground	**12**	DSIB_D3_P	MIPI-DSI-Data lane
13	DSIB_D0_P	MIPI-DSI-Data lane	**14**	DSIB_D3_N	MIPI-DSI-Data lane
15	DSIB_D0_N	MIPI-DSI-Data lane	**16**	GND	Ground
17	GND	Ground	**18**	DSIB_CLK_P	MIPI-DSI-Clock lane
19	DSIB_D1_P	MIPI-DSI-Data lane	**20**	DSIB_CLK_N	MIPI-DSI-Clock lane
21	DSIB_D1_N	MIPI-DSI-Data lane	**22**	GND	Ground
23	GND	Ground	**24**	DSIB_D2_P	MIPI-DSI-Data lane
25	DSIA_D2_N	MIPI-DSI-Data lane	**26**	DSIB_D2_N	MIPI-DSI-Data lane
27	DSIA_D2_P	MIPI-DSI-Data lane	**28**	GND	Ground
29	GND	Ground	**30**	DSIA_D1_N	MIPI-DSI-Data lane
31	DSIA_CLK_N	MIPI-DSI-Clock lane	**32**	DSIA_D1_P	MIPI-DSI-Data lane
33	DSIA_CLK_P	MIPI-DSI-Clock lane	**34**	GND	Ground
35	GND	Ground	**36**	DSIA_D0_N	MIPI-DSI-Data lane
37	DSIA_D3_N	MIPI-DSI-Data lane	**38**	DSIA_D0_P	MIPI-DSI-Data lane
39	DSIA_D3_P	MIPI-DSI-Data lane	**40**	GND	Ground
41	GND	Ground	**42**	NC	No Connection
43	ID0	ID Pin(low : 0)	**44**	LED+	LED Positive power
45	ID1	ID Pin (high : 1)	**46**	NC	No Connection
47	IOVCC1	Power for digital circuit	**48**	LED1-	LED Negative power
49	IOVCC2	Power for digital circuit	**50**	LED2-	LED Negative power

TFT LCD Panel

Items	Symbol	Min.	Typ.	Max.	Unit
Logic voltage	VDDI	-	1.8	-	V
Positive Analog Power Supply Voltage	VSP	-	6.0	-	V
Negative Analog Power Supply Voltage	VSN	-	-6.0	-	V

Backlight (20% duty)

Item	Symbol	Min.	Typ.	Max.	Unit
Forward Voltage	VBL	-	6.5	-	V
Forward Current	IBL	-	45	-	mA
Power Consumption	PBL	-	468	-	mW
LED Quantity	8 (2 in1)				ea



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14. Power Supply On/Off Timing Specification

R63455 can be operated by supplying the VSP and VSN power supplies directly.

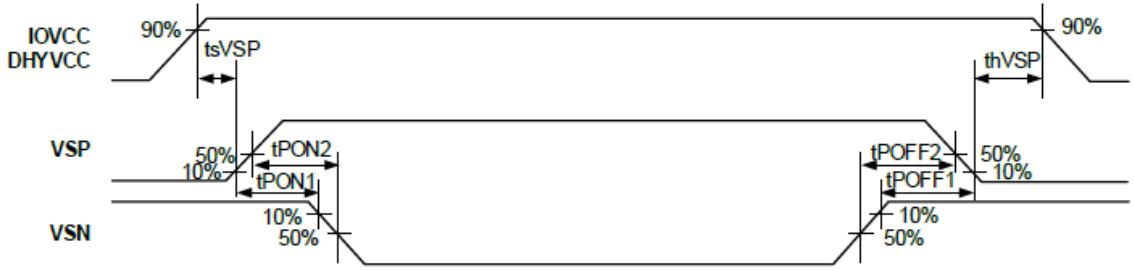

Figure 8. Power supply on/off timing

Table 23. Power supply timing specifications

Item	Symbol	Unit	Test Condition	Minimum	Maximum
VSP-VSN delay time (10% to 10%)	tPON1	µs	Power on	0	–
VSP-VSN delay time (50% to 50%)	tPON2	µs	Power on	0	–
System power on to VSP ON time	tsVSP	ms	Power on	1	–
VSN-VSP delay time (10% to 10%)	tPOFF1	µs	Power off	0	–
VSN-VSP delay time (50% to 50%)	tPOFF2	µs	Power off	0	–
VSP OFF to system power OFF time	thVSP	µs	Power off	0	–

Note: For more information, see section 18.6 (Reset Timing Characteristics) in this document.

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Reset timing at power supply on

Table 34. Reset timing characteristics

Item	Symbol	Unit	Test Condition	Minimum	Typical	Maximum
Reset low-level width1	tRW1	µs	Power supply on	3000	–	–
Reset low-level width2	tRW2	µs	Operation	1000	–	–
Reset low-level width3	tRW5	ms	Power supply off	25	–	
Reset to MIPI command	tRT1	ms	Sleep in	20	–	–
Noise reject width	tRESNR	µs	–	–	–	1

Figure 14. Reset reject pulse width

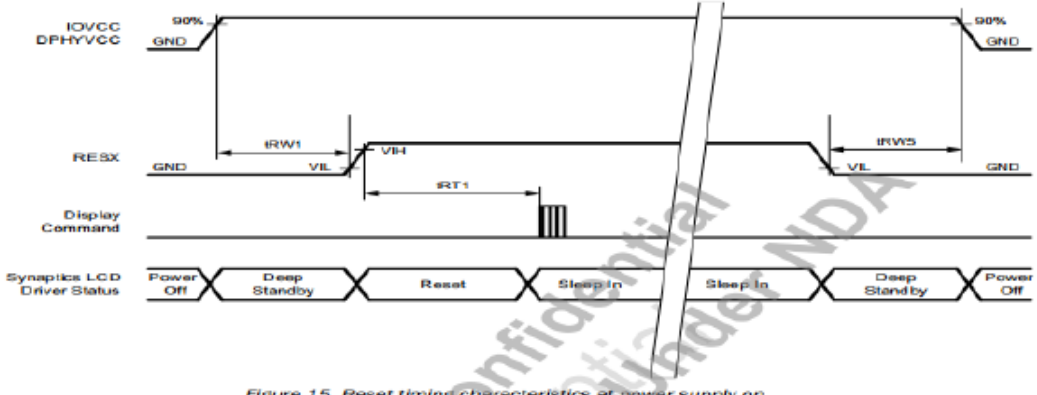

Figure 15. Reset timing characteristics at power supply on

Reset timing in sleep in/out

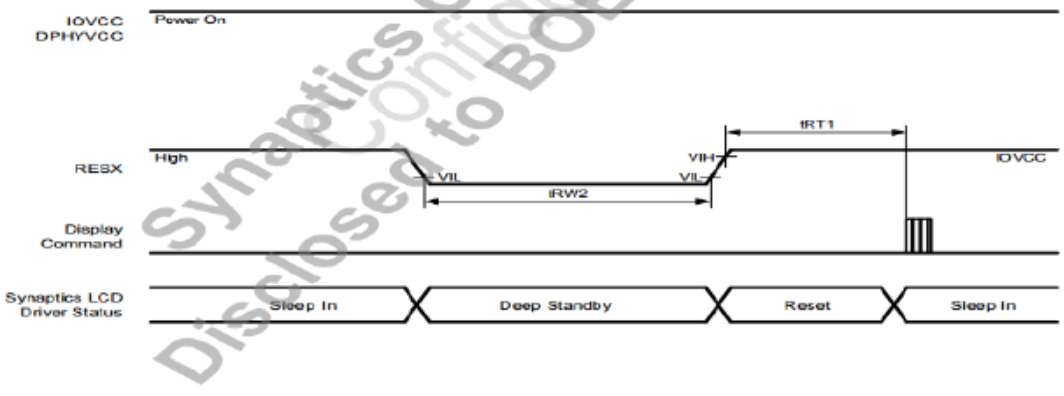

Figure 16. Reset timing in Sleep In

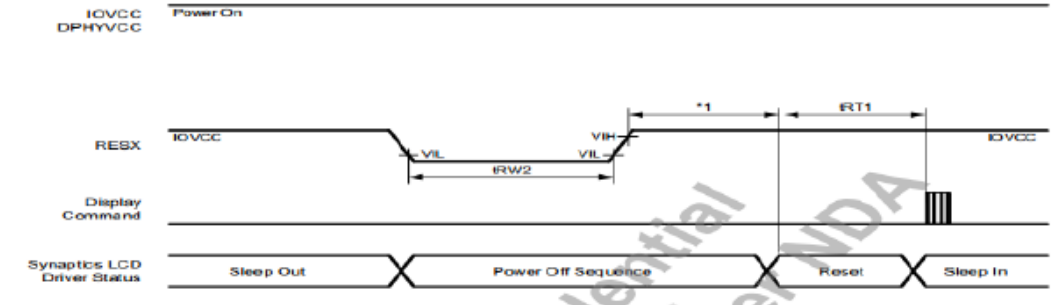

Figure 17. Reset timing in Sleep Out