ECEN452: ULTRA HIGH FREQUENCY TECHNIQUE

LAB05

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TASK 1: Design of a TRL Calibration Kit

BACKGROUND:

TRL Calibration technique is accurate by measuring a single reflection term and two transmission terms and all these values are used to determine the 12 error terms. It is generally known that TRL Calibration is more accurate than SOLT Calibration that uses well-defined short, open, and load.

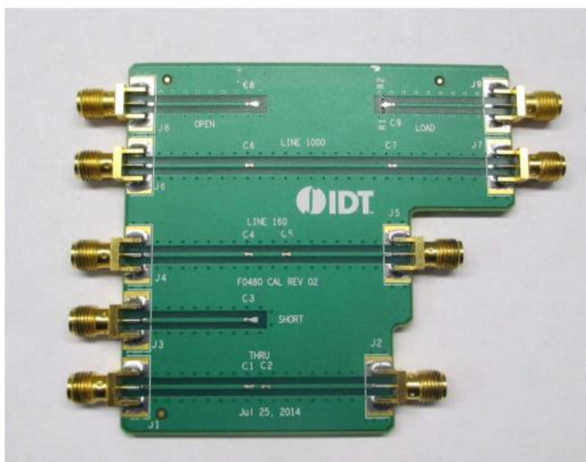


Figure 1. TRL Calibration Kit used for F0480

INGREDIENTS:

FR4 has the following features:

$\varepsilon_r = 4.1$

$\mathrm{Tan}\delta = 0.01$

Thickness = 61 mil = 1.5748 mm

$Z_0 = 50\ \Omega$

Distance from the reference plane = 15mm

$1\mathrm{GHz} \leq f \leq 5\mathrm{GHz}$

Calculate the required physical width of the microstrip line

First calculate A and B given by

$$A = \frac{Z_0}{60}\sqrt{\frac{\epsilon_r + 1}{2}} + \frac{\epsilon_r - 1}{\epsilon_r + 1}\left(0.23 + \frac{0.11}{\epsilon_r}\right)$$

$$B = \frac{377\pi}{2Z_0\sqrt{\epsilon_r}}.$$

A = 1.486838527

B = 5.849238024

My first guess is that $\frac{W}{d} < 2$

$$\frac{W}{d} = \begin{cases} \dfrac{8e^A}{e^{2A} - 2} & \text{for } W/d < 2 \\ \dfrac{2}{\pi}\left[B - 1 - \ln(2B - 1) + \dfrac{\epsilon_r - 1}{2\epsilon_r}\left\{\ln(B - 1) + 0.39 - \dfrac{0.61}{\epsilon_r}\right\}\right] & \text{for } W/d > 2, \end{cases} \tag{3.197}$$

The ratio came out to be

$$\frac{W}{d} = 2.014647836 > 2$$

Thus it should be greater than 2

So again the ratio came out to be

$$\frac{W}{d} = 2.01630280 > 2$$

Which satisfies the condition

Therefore, with the given thickness d = 1.5748mm

W = 3.175273653 mm

Calculate the design frequency of calibration kit

$$f_o = \frac{f_L + f_H}{2} = 3 \text{ GHz}$$

Also known as the center frequency

Calculate the effective dielectric constant

$$\epsilon_e = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2} \frac{1}{\sqrt{1 + 12d/W}}.$$

Using the ratio we obtained from above

$$\varepsilon_e = 3.137885623$$

Using (2) and (3), calculate the physical length [mm] for a quarter wavelength section of transmission line

$$v_p = \frac{c}{\sqrt{\epsilon_e}},$$

$$\beta = k_0 \sqrt{\epsilon_e},$$

The phase velocity is calculated

$$\upsilon_P = 169{,}239{,}664.3 \left[\frac{m}{s}\right]$$

Where the speed of light is 299,792,458 m/s

(1) When frequency is 5 GHz (Max)

$$\lambda_{f\_max} = 0.0338479329 \text{ m}$$

Therefore the quarter wave section is 8.461983214 mm

(2) When frequency is 1 GHz (Min)

$$\lambda_{f\_min} = 0.1692396643 \text{ m}$$

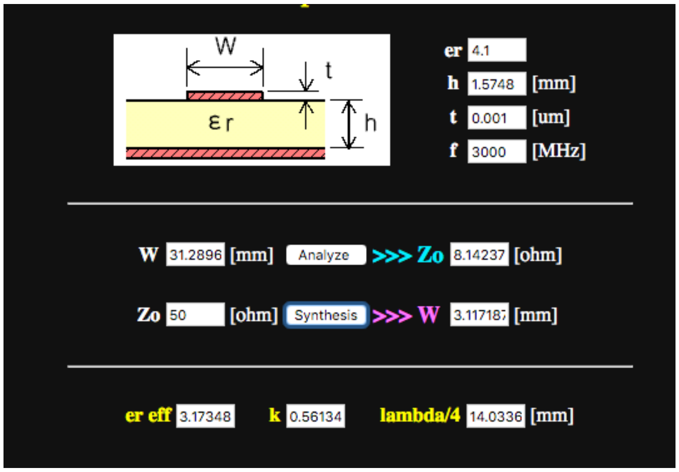
Therefore the quarter wave section is 42.30991608 mm

(3) When frequency is 3 GHz (the design frequency)

$$\lambda_{f\_design} = 0.0564132214 \text{ m}$$

Therefore the quarter wave section is 14.10330535 mm

Microstrip line calculator:



The results I calculated show fairly good harmony with those from the online microstrip line calculator.

HFSS DEGISN:

LINE:

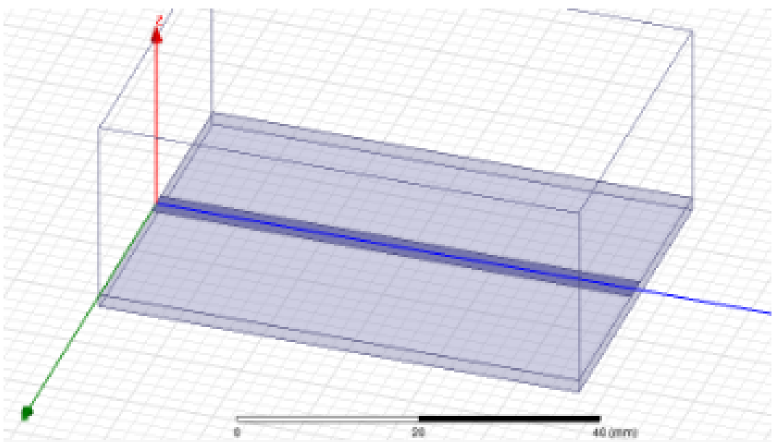
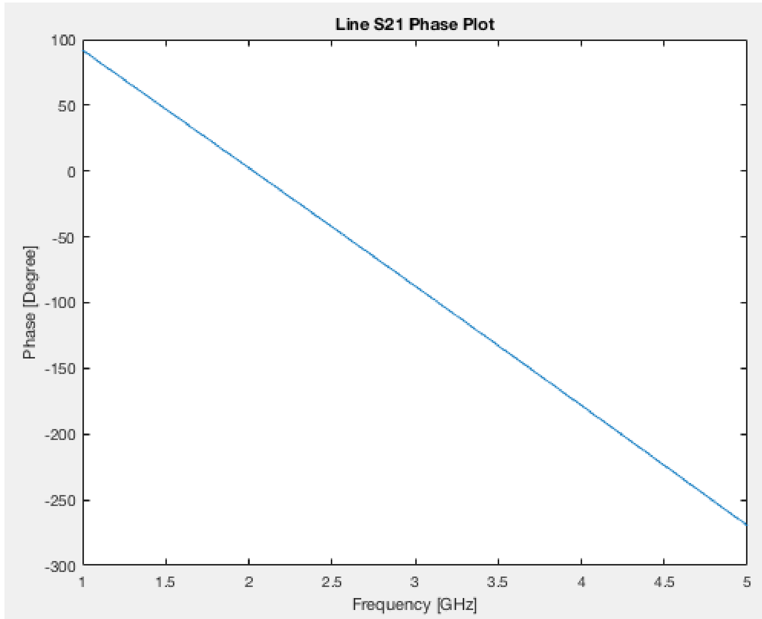


Figure. Line Design



Figure

REFLECT:

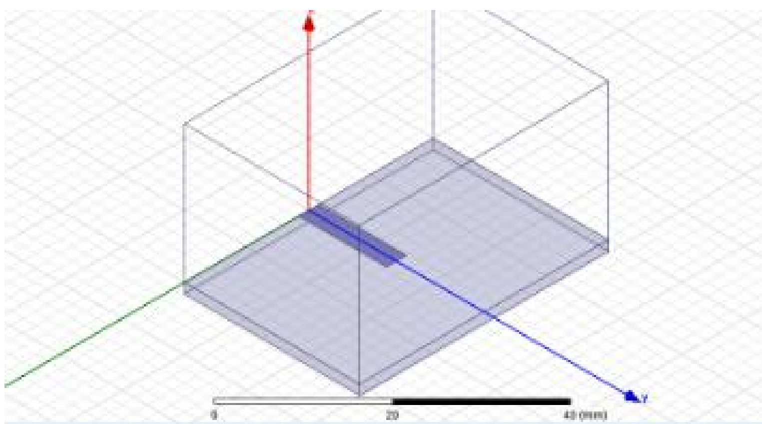
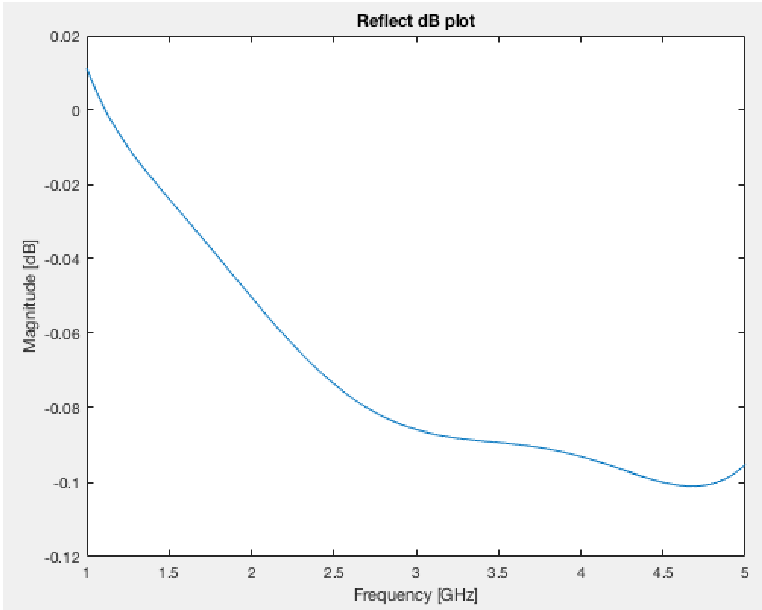


Figure. Reflect Design

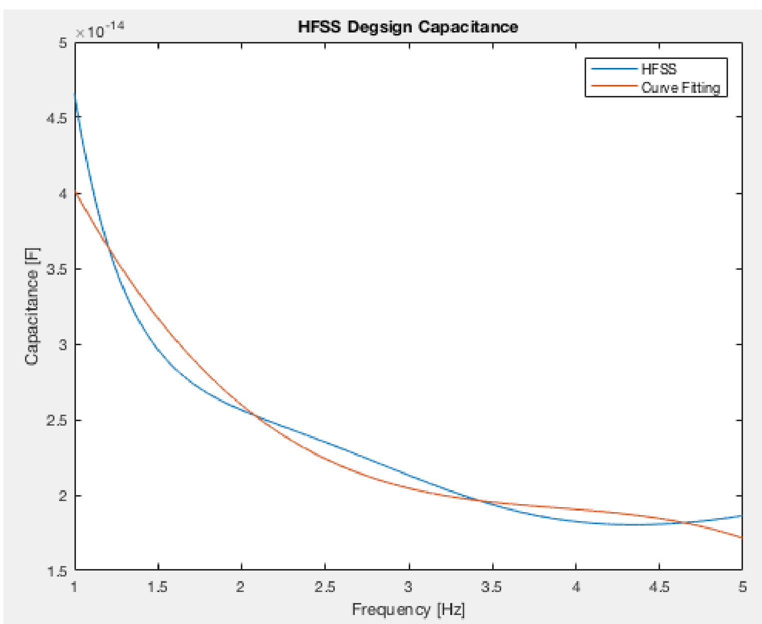


Figure

It’s really hard to tell there’s a variation in this plot but I just attached it anyway.

$$Im(Z) = \frac{1}{j\omega C}$$

$$C = \frac{1}{j\omega \cdot Im(Z)} = \frac{-j}{2\pi(3GHz) \cdot Im(Z)}$$



Figure

In MATLAB, I used ‘polyfit’ and ‘polyval’ functions for curve fitting since my computer has a little problem with running Python.

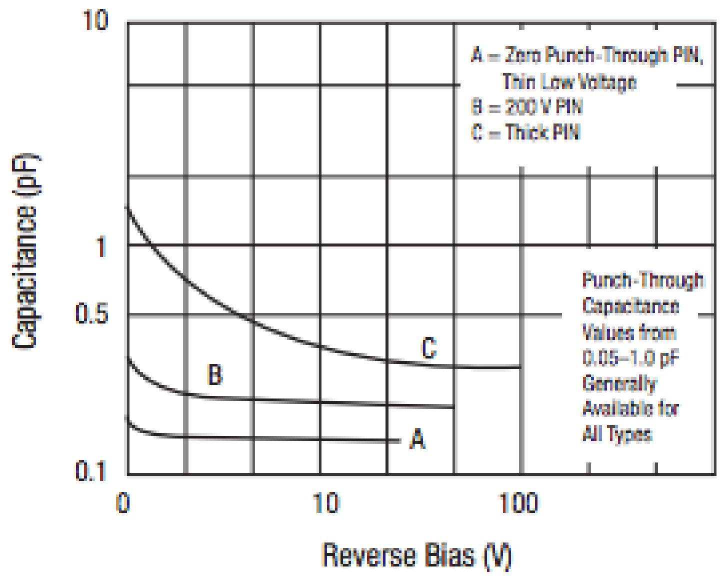


Figure 3. Typical Capacitance

Figure. Skyworks PIN Diode Capacitance Case

Note that this plot is with respect to Reverse Bias Voltage. This is absolutely good plot since our parasitic capacitor in PIN diode will be varied with frequency.

THRU:

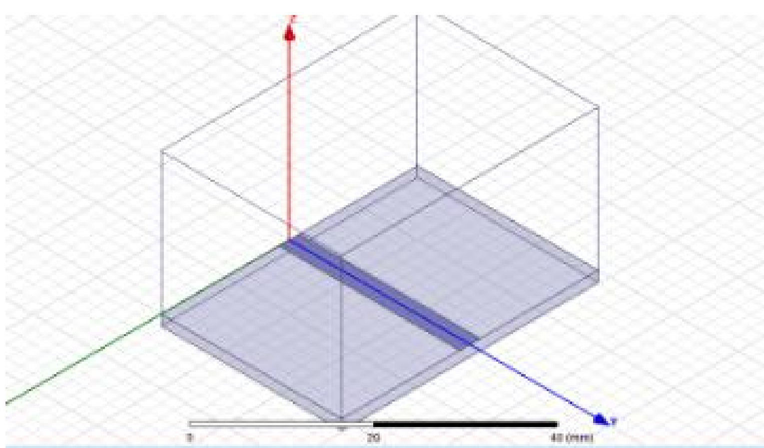
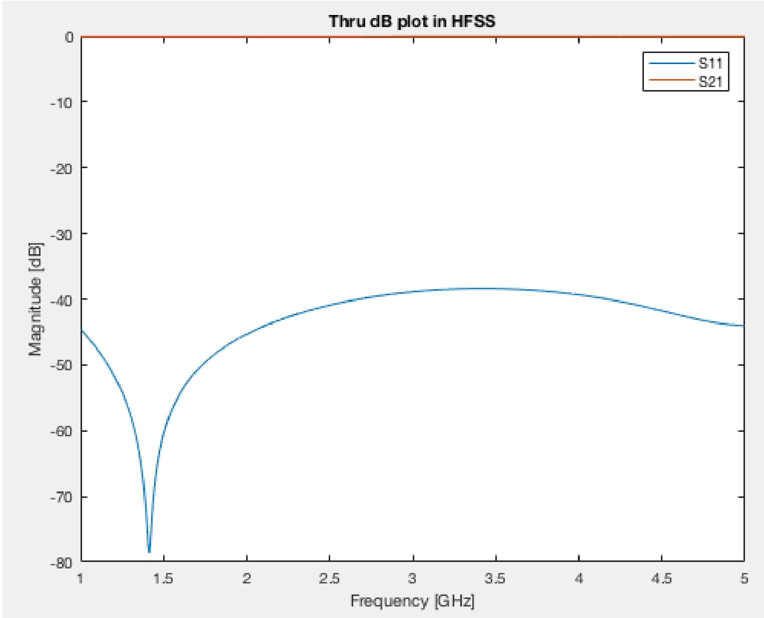
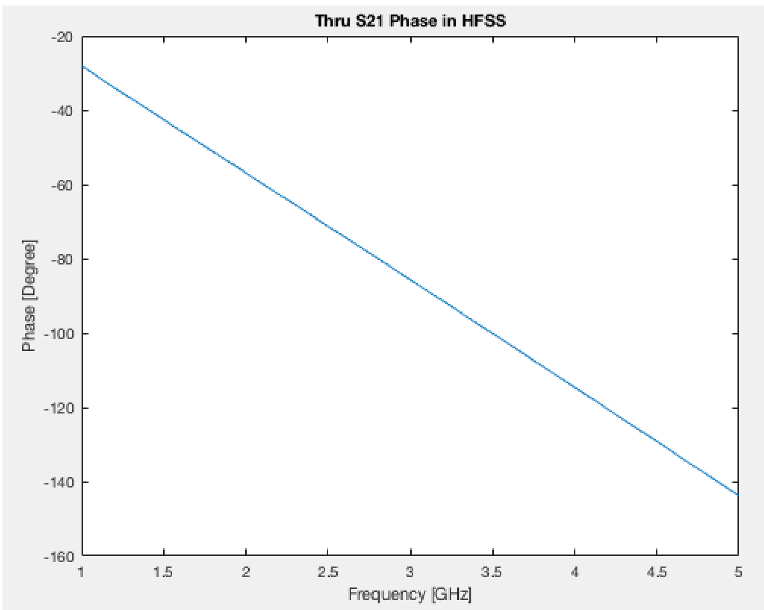


Figure. Thru Design



Figure



Figure

Task2: Design of an RF PIN diode series switch

INGREDIENTS:

Dielectric Constant (relative) = 4.1

The design frequency = 2.5GHz

Reference impedance = 50 ohm

Thickness of substrate = 62mil = 1.5748 mm

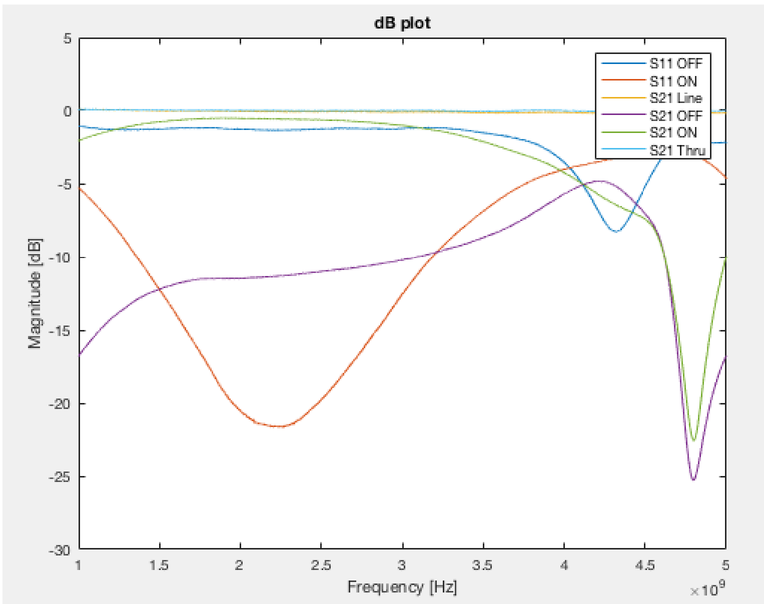
CALCULATION:

Width of 50 ohm microstrip line = 3.16 mm

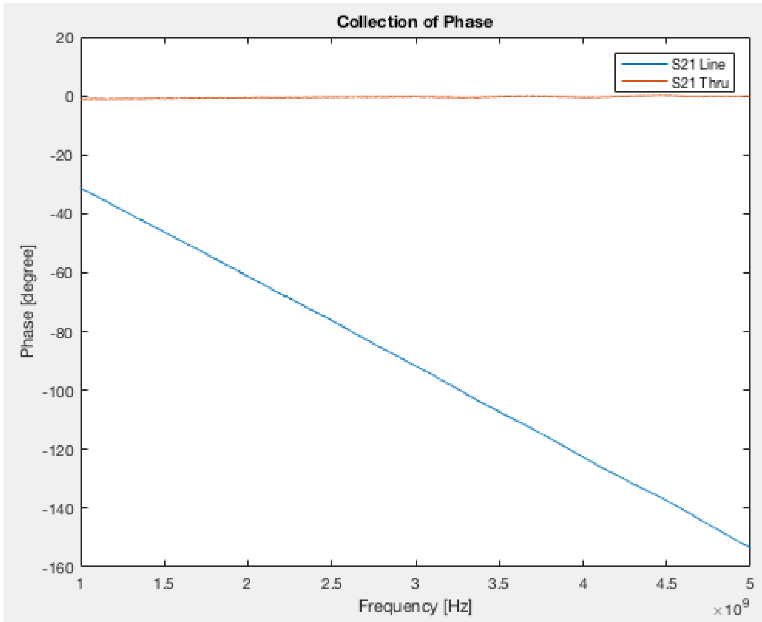
Quarter wave length line = 17.674 mm

Width of 100 ohm microstrip line = 0.747 mm

LAB MEASUREMENT:



Figure



Figure

We see for Line case, there is no phase difference between port 1 and 2 whereas there is for Thru case. It seems there is about 120 Degree phase difference with respect to Frequency. In practice, frequency sweep means changing in capacitance of the diode which is altered by varying bias voltage applied to the diode.

HFSS DESIGN:

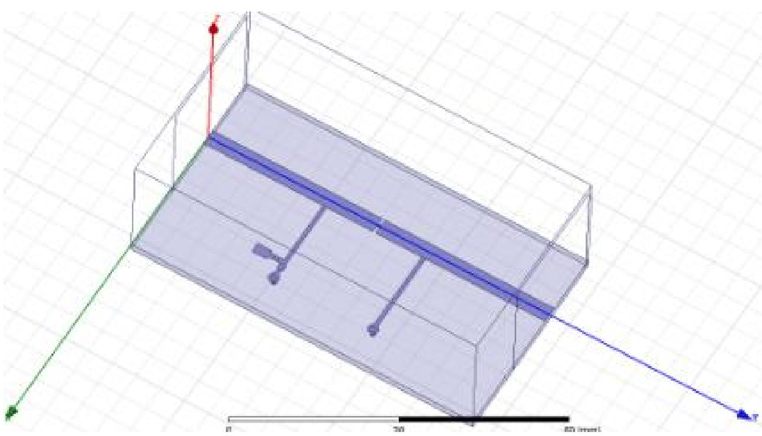


Figure. PIN Diode Design

This design uses the above calculation.

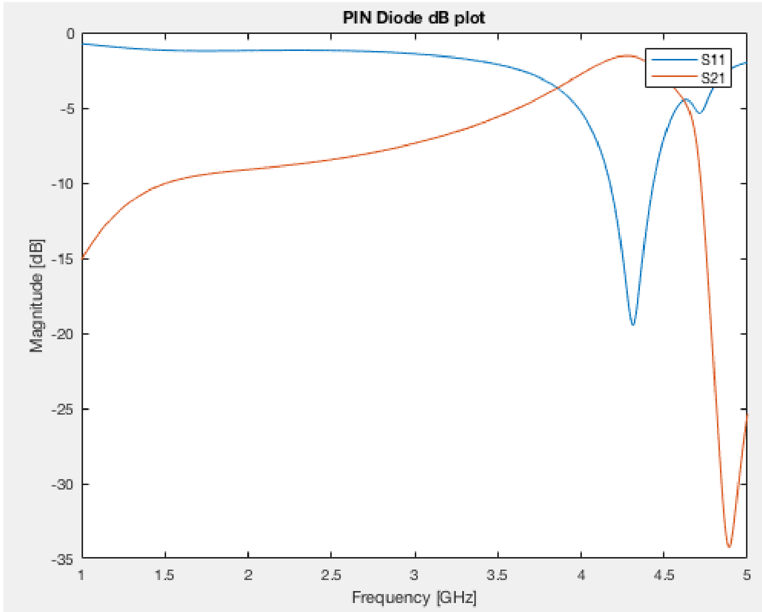

PIN Diode dB plot
S11
S21
Magnitude [dB]
Frequency [GHz]
0
-5
-10
-15
-20
-25
-30
-35
1
1.5
2
2.5
3
3.5
4
4.5
5

Figure. HFSS