ECE 4094

Project A

(SDR for Sounding Rocket Telemetry)

Progress Report

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Objectives

- To design and construct a Software Defined Radio platform (SDR) per the specifications outlined in the *Design Specification*
- Simulate the expected performance of the system, as part of the design phase
- Verify the operation of the constructed system against what was expected from simulation of the design
- By writing appropriate software, interface the SDR with the existing ecosystem of SDR software
- Learn a lot about RF engineering, produce a useful SDR and an interesting report/presentation!

Progress to Date

The majority of Semester 1 2020 has been spent gaining familiarity with the required concepts needed to be able to design a radio receiver and then searching for appropriate parts (appropriate in terms of cost and capability).

Selection of Major Components and Architecture:

A range of suitable RF hardware and ADCs has been reviewed, and an architecture has been developed around the following parts:

- BGU7045 (LNA)
- MSi001 (tuner)
- MAX11131 (ADC)
- FX2LP (microcontroller used as a USB 2.0 bridge; makes it easy to send samples from the ADC over USB)

Relevant Background Study:

I have gained some familiarity with concepts related to RF I haven't encountered before, including:

- Receiver architectures
    - Multistage superheterodyne and choice of intermediate frequencies
    - Single stage down to Low-IF or zero-IF
    - Direct digital down conversion
- Mixing (for up conversion and down conversion)
- Image rejection
    - Techniques for achieving it
    - How it is tested/measured
- Non-linearities (in amplifiers)
    - Intermodulation distortion (IMD)
    - 1dB compression point
    - Third order intercept point (OIP3, IIP3)
- Calculating noise figure, intermodulation products and gain through a chain of components
- Impedance matching
    - Smith charts
    - Controlled impedance traces
- Balanced and unbalanced signals
- Characterisation of phase noise

Study on PCB Design Techniques:

I have researched PCB design for RF and analogue electronics, and compiled some guidelines:

- Use a four-layer PCB, with a stack-up like so:
    1. Signals (RF, particularly)
    2. Uninterrupted ground plane
    3. Uninterrupted power plane
    4. Other signals
- Keep RF signals on the same layer
- Route RF signals first, then digital signals, then power
- Keep high speed digital signals away from RF
- Baluns and filters can be found as small SMD components
- Try to use the most integrated components possible
- Use a trace impedance calculator (provided by most PCB manufacturing houses) to figure out the dimensions of the RF traces
- Provide decoupling on all digital chips (usually per the manufacturer's recommendations).

Research on Existing Software Which May be Suitable:

The libmirisdr and libmirisdr-4 drivers, which are open source and contain code to control the Mirics MSi001, have been looked into, and the registers they manipulate to control the MSi001 appear to correspond very well to the MSi001 datasheet. This means the control commands from these drivers should be easy to pass through the FX2LP to the tuners. However, the return path--the bulk data transfer from the ADC(s)--has not been looked into yet. It is unknown yet how much of the rest of the open source driver will be reusable, especially given this SDR will have four tuners and will use different ADC and USB hardware to the target of the libmirisdr drivers.

Work to be Completed

Table 1: Work to be Completed, Time Estimates and Dependencies

Task	**Time Estimate**	**Dependencies**
1. Complete the selection of parts: Some components need to be investigated further to determine suitable parts, including: • Crystals/oscillators required for the RF/ADC/digital circuits • Passive supporting circuitry around all the other components. Most of this will be sourced from reference designs, however a reference design hasn't been found for the MSi001 tuner yet.	15 hours Specifying suitable oscillators/crystals and simple components such as voltage regulators, decoupling capacitors, resistors, etc. should not be too time-consuming. However, figuring out the specifications for the RF passives and sourcing them is expected to be more difficult, as this is not something I have done before.	None
2. Characterise the design: I have yet to apply these RF concepts to analyse the design so that its characteristics can be theoretically calculated. It would be good to know the final performance of the design on a few points: • Sensitivity • Noise floor • Gain • Susceptibility to IMD from nearby high-power signals (e.g. FM stations) • Phase noise • Frequency drift and offset • I/Q phase error Some of these can be derived from the datasheet of the tuner, however others will need a bit of analysis and simulation. Once the component choice has been verified at this level, PCB layout can be started.	10 hours to work through a rough back-of-the-envelope calculation in a few operating regions/conditions. 20 hours of additional work to develop a Simulink model using the RF toolbox, which will allow more complex and thorough analysis.	Partial dependency on Task 1 because a frequency reference needs to be selected in order to approximate phase noise and frequency drift.

3. Design the PCB A large part of this will involve searching for reference designs for the MSi001 tuner. This will help a lot. If such designs can't be found, then studying reference designs for other tuners will be helpful.	40 hours	Depends on Tasks 1 and 2
4. Order and assemble PCB and components	2 to 4 weeks for manufacturing and shipping. 4 weeks lead time on the Mirics MSi001 tuners. I am allowing this time as these have to be sourced from less reputable suppliers. 2 weeks lead time on all other components. 2 weeks lead time on the PCB	Depends on Task 3 However, the MSi001 tuners should be ordered immediately upon smooth completion of Task 2, because they have the most uncertain lead time, yet are almost guaranteed to be utilised in the final design.
5. Write firmware to run on the FX2LP to handle: • Bulk transfer of ADC samples over USB • Passing of control signals/data (from the driver) received over USB to the tuners The firmware on the FX2LP will be simple because it acts only as a bridge, with most of the complexity shifted onto the driver running on the host computer.	30 hours This firmware will not be complex, acting only as a bridge, however it will require programming an unfamiliar chip with an unfamiliar toolchain, hence the large allotted time. Some research into the USB specification is also expected.	Depends on Task 4 to be able to perform final integration and testing. However, large portions of this task have no dependencies, as I already have a development board for this chip available.
6. Adapt the libmirisdr-4 driver so that it presents this SDR correctly to the existing ecosystem of SDR software as four independently tuneable radios.	50 hours This task is expected to be the most complex part of the software, so a lot of time has been allotted.	Runs in parallel to Task 5 Similar to Task 5, enough is already known, and adequate hardware is on hand, to begin on large portions of this task.
7. Verify the performance of the SDR via lab testing and compare results with the theoretical design specifications.	10 hours of lab time with test equipment 6 hours to analyse the data and compare it	Depends on all previous tasks
8. Presentation and reporting • Compile the final report. • Produce a presentation poster.	30 hours	None; this task is completed throughout the design process.

Proposed Gantt Chart of Work to be Completed

The project schedule will rely in large part on the winter break period, after semester one exams, for a timely completion. It is expected that during the break this project will receive undivided attention, hence why Tasks 2 and 3 appear shorter than would be assumed with the average 8 hours a week that I have found to be achievable during semester, which is quite limiting. Tasks 5 and 6 are also expected to have work begin on them during the winter break period, as they have components which can be completed independently.

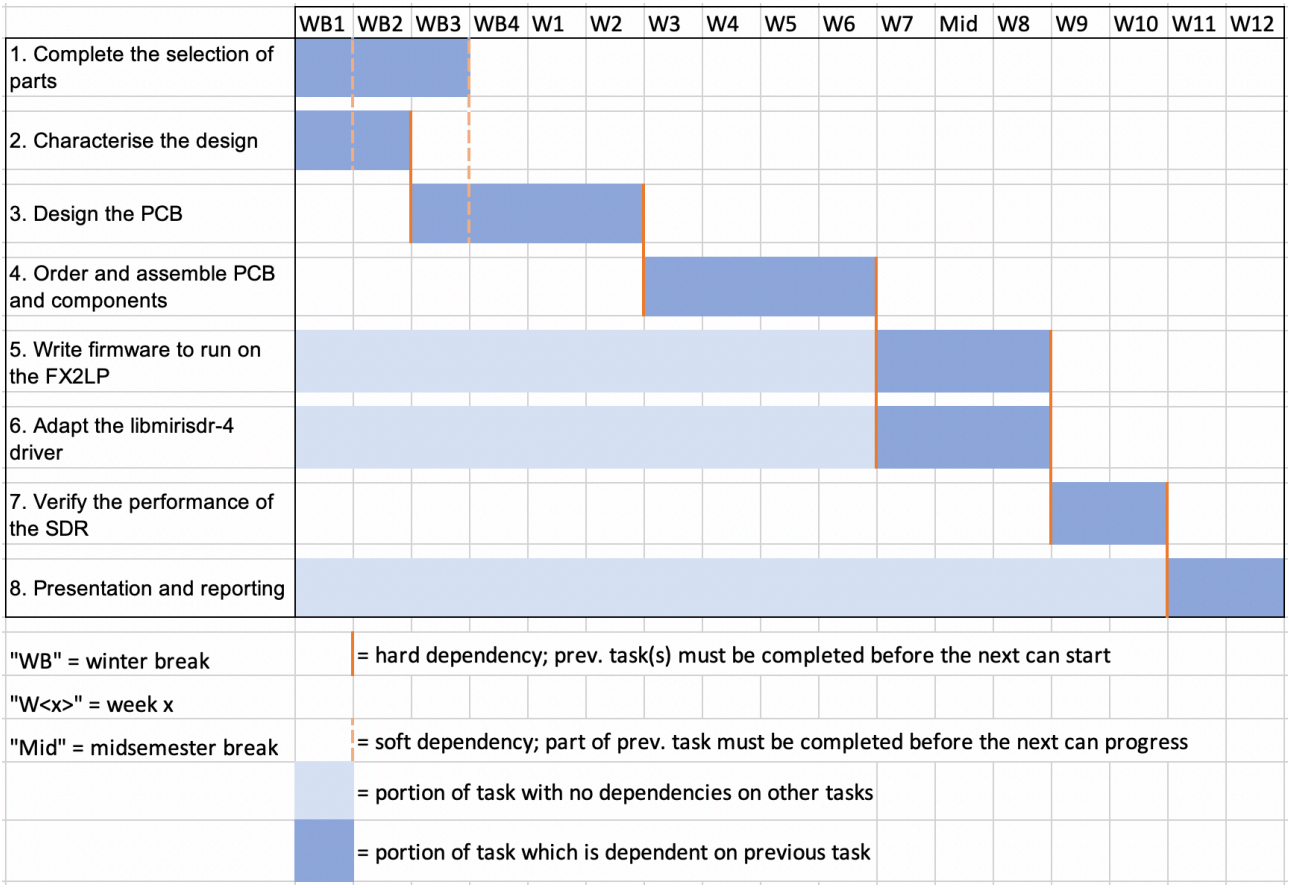

Figure 1: Proposed Gantt Chart of Work to be Completed (Project Timeline)