



北京郵電大學

BEIJING UNIVERSITY OF POSTS AND TELECOMMUNICATIONS



Computer Organization and Architecture

期中考试题讲解

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判断题1

- Many computer manufacturers(计算机厂家) offer a family of computer models, all with the same organization but with differences in architecture. F
相同的架构，不同的组织形式
- Clock speed plays a decisive role in computer performance. F
时钟频率不是决定性的，还有很多因素影响
- In general, the more devices attached to the bus, the greater the bus length and hence the less the propagation delay(传播延迟).F
总线上设备越多，冲突越多，传播延迟越大
- Asynchronous (异步) timing means occurrence of one event(事件的发生) on a bus follows and depends on occurrence of a previous event(前一个事件). T
异步时钟下，事件依赖于上一个事件
- In direct access(直接存取) method, each addressable location in memory has a unique(唯一), physically wired-in(固定) addressing mechanism. The time to access a given location is independent of(不依赖于) the sequence of prior accesses and is constant. F
直接存取的代表硬盘，需要寻道



判断题2

- In a non-volatile(非易失) memory, information once recorded remains without deterioration(衰减) until deliberately(故意) changed and no electrical power is needed to retain information. T
非易失性存储器，不容易丢失，除非破坏
- The main memory(主存) is the only form of Internal memory(内存) for the computer system. F
内部存储器还包括cache, 寄存器
- When the processor detects an interrupt, hardware poll(硬件轮询) branches to an interrupt-service routine whose job is to poll each I/O module to determine which module caused(引起) the interrupt. F
中断设备的判断由CPU来完成，而不是中断处理程序
- When a DMA module takes control(控制) of a bus, and while it retains(保持) control of the bus, the processor will pause(暂停) for each bus cycle stolen by the DMA module. T
周期窃取
- It is necessary for all of the pages(页) of a process(进程) to be in main memory while the process is executing. F
不需要，可以通过换页方式加载



选择题1

- 1. The key idea of von Neumann(冯.诺依曼) computer development is often devoted to the _____. (C)

- A. quickly computing speed
- B. capable of storing both data and instructions
- C. stored-program concept
- D. operating on binary data

冯诺依曼计算机的典型特点就是存储程序的概念。

- 2. The era of computer development is often divided by the _____. (C)

- A. program language
- B. computing speed
- C. electronic components used in it
- D. computer architecture

计算机中，第一代是真空管，第二代是晶体管，第三代是集成电路。是以他们采用的电子元件来划分的。



选择题2

- 3. For _____ method, access is done by using a combination(结合) of moving to general memory area followed by sequential access to reach the desired data item. (B)
 - A. sequential access(顺序访问)
 - B. Direct access(直接访问)
 - C. Random access(随机访问)
 - D. Associative access(相联访问)

直接访问是先顺序到区域，然后再访问数据，典型的代表是硬盘。

- 4. Examples of architectural attributes(体系结构属性) for the computer include the instruction set, _____, I/O mechanisms, and _____. (B, D)
 - A. memory technology
 - B. the number of bits used to represent various data types
 - C. interfaces
 - D. techniques for addressing memory
 - E. control signals

计算机中体系架构的属性包括指令集、数据的表示方法，IO机制以及寻址方式



选择题3

- 5. _____ specifies(指定) the data in memory to be written from or read into the CPU. (B)
 - A. IR
 - B. MBR
 - C. MAR
 - D. PC

IR: 指令寄存器， MBR: 存储器缓冲寄存器， MAR: 存储器地址寄存器 PC: 程序计数器

- 6. _____ are not the characteristics(特性) of a computer family(系列机). (D)
 - A. Similar or identical(类似或同样的) instruction set
 - B. Similar or identical operating system
 - C. Increasing number of I/O ports
 - D. Similar in the organization
 - E. Increasing memory size

系列机具有相似指令集，相似的操作系统，端口和内存可以扩展。但组织可以不同，采用更先进的技术来提高计算机的性能。



选择题4

- 7. Although there are many different bus designs, on any bus the lines can be classified into three functional groups _____, _____, and control lines. (C, E)

- A. External
- B. System
- C. Data
- D. Internal
- E. Address

总线一般分为数据总线、地址总线和控制总线

- 8. _____, the processor checks(检查) to see if any interrupts are pending(悬而未决): If no interrupt, proceed with the next instruction. (D)

- A. At the any time of instruction cycle
- B. At the beginning of instruction cycle
- C. At the middle of instruction cycle
- D. At the end of instruction cycle

中断的检测是在指令执行完成之后进行的。



选择题5

- 9. In the _____ mode, the I/O module and main memory exchange data directly, without processor involvement. (D)
 - A. Programmed I/O
 - B. Interrupt-driven I/O
 - C. I/O channel
 - D. Direct memory access (DMA)

DMA交换数据时，CPU基本不需要参与，只需要在前后进行处理。
- 10. The refresh of dynamic RAM is preformed by _____ as a refreshing unit. (C)
 - A. Memory unit
 - B. Byte
 - C. Row
 - D. Block

RAM的刷新是按行进行的。



选择题6

- 11. The width(宽度) of data bus impacts(影响) _____. (C)
 - A. the word length of machine
 - B. system capacity
 - C. system performance
 - D. memory bandwidth

地址总线的宽度决定了系统容量，数据总线的宽度决定了系统性能，控制总线的宽度决定了系统复杂性。



简答题1

- Briefly describe the cache replacement strategy (策略)

Cache替换策略和映射方式有关。

对于直接映射，不需要替换策略，直接替换。

对于相联映射，可以采用先进先出、最近使用原则、最多使用原则、随机原则进行替换。



简答题2

- Briefly describe the capacity (容量) expansion method of memory

内存容量扩展包括两种方式：

1. 使内存变深。增加芯片，扩展内存地址空间，可以容纳更多的存储单元。
2. 使内存变宽。增加芯片，使每个寻址单元的数据分布在多个芯片上，扩展每次读取内存的数据的宽度。

一般是两者相结合。



简答题3

- What does clock stealing in DMA mean?

时钟窃取指的是DMA在需要使用总线的时候，如果CPU也需要使用总线，此时系统让CPU挂起一个时钟周期，让DMA完成数据传输。DMA完成后，CPU再使用总线。



简答题4

- Briefly describe the core meaning of Amdahl's law (阿姆达定律)

阿姆达定律指出，程序的并行性对多核处理器的加速比具有很大影响。如果程序的并行性不高，那么即使采用多核，也不能充分发挥多核的优势。

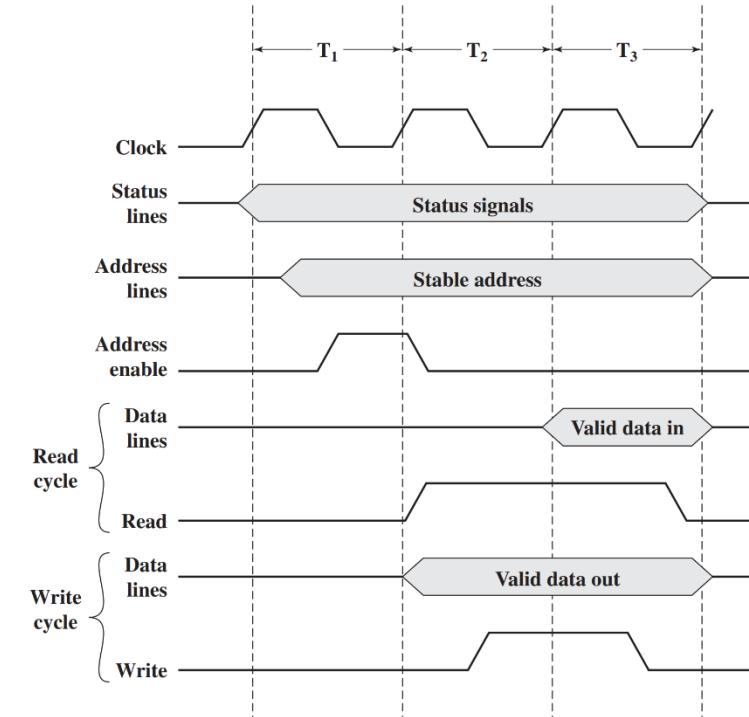
$$\text{Speedup} = \frac{\text{time to execute program on a single processor}}{\text{time to execute program on } N \text{ parallel processors}} = \frac{T(1-f) + Tf}{T(1-f) + \frac{Tf}{N}} = \frac{1}{(1-f) + \frac{f}{N}}$$

IV 图形解释

- Please describe synchronous(同步) read operations according to the giving diagram.

同步的读操作过程如下：

- 在第一个时钟周期内，总线状态信号有效，主设备发出地址信号，并将地址信号放在总线上，且信号稳定；
- 第二个时钟周期内，主设备发出读命令，从设备做出发送数据的准备；
- 第三个时钟周期内，从设备将有效数据放在数据总线上，主设备从数据总线上读出所需数据。完成读操作。





V

- Consider a 32-bit microprocessor, with a 32-bit external data bus, driven by a 4-MHz input clock. Assume that this microprocessor has a bus cycle whose minimum duration equals four input clock cycles. What is the maximum data transfer rate across the bus that this microprocessor can sustain, in bytes/s?
 1. 时钟周期= $1/4\text{MHz}=250\text{ns}$
 2. 总线周期=4个时钟周期= $1\mu\text{s}$
 3. 32位总线，在一个总线周期传完4个字节，所以，每个字节传送需要 250ns
 4. 传输速率= $1\text{byte}/250\text{ns}$ 换算后传输速率为 4MBps

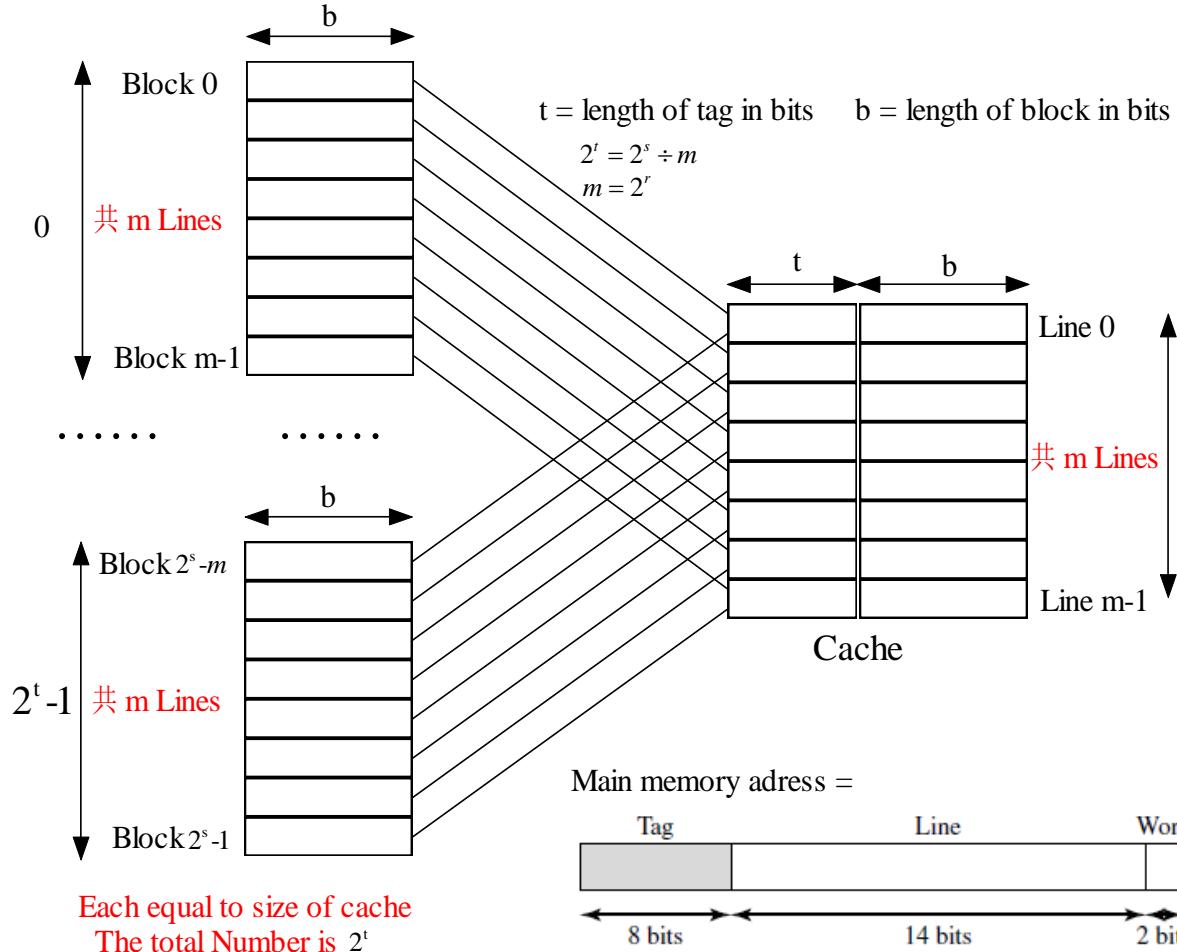


VI

- Consider a machine with a byte addressable main memory of 2^{24} bytes and block size of 8 bytes.
- 1) Assume that a direct mapped(直接映射) cache consisting of 1K lines is used with this machine.
- a. How is a 24-bit memory address divided into the tag, line number, and byte number? (2 marks) Please give the analysis and fill the results in the following table.

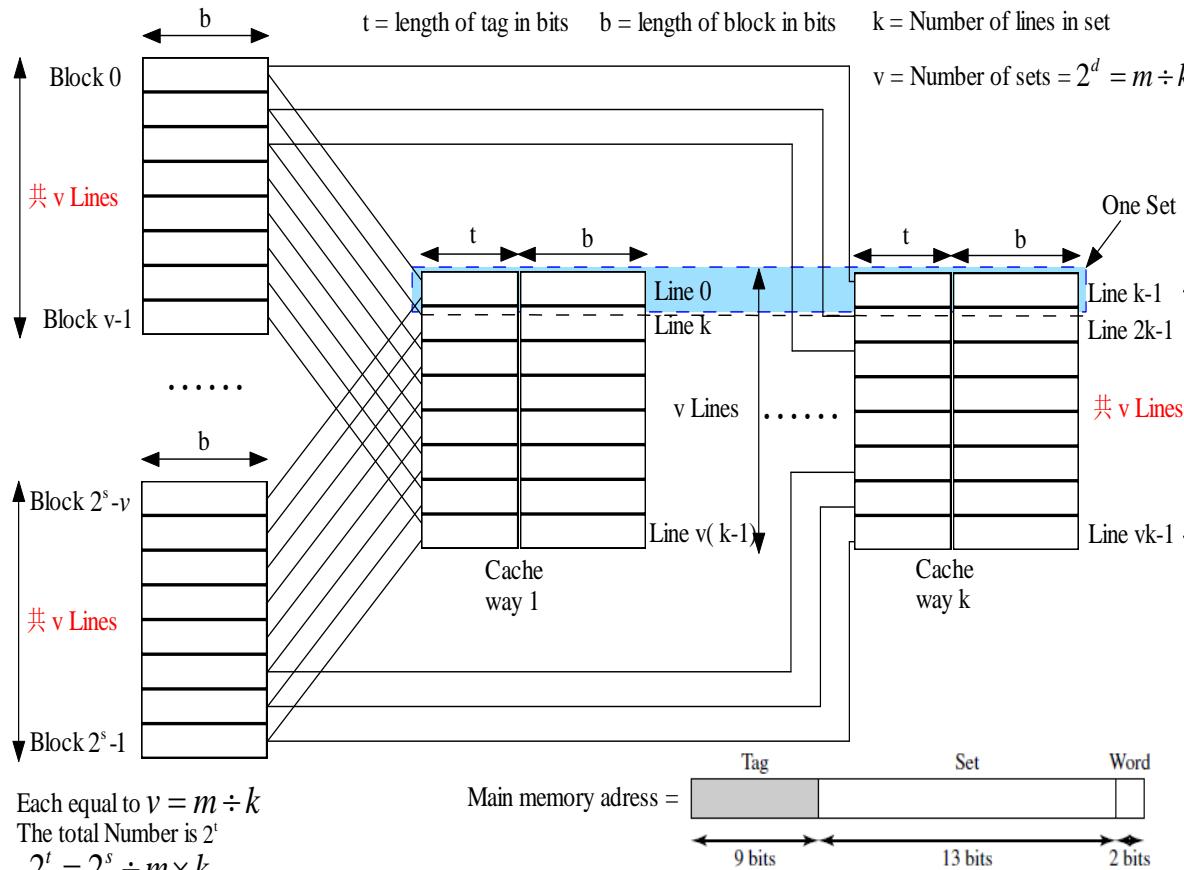
Tag	<u>Line</u> (or Slot)	Word ↳
↖	↖	↖

Direct mapping



- 内存中的块从头开始，按照cache的行数进行分组，每组都有m块
- 每一组都按照顺序映射到cache的行
- 内存中的一个块只能映射到cache中的唯一一行
- Cache中的一行对应内存中的 2^t 块

Set associative mapping



- cache采用 v 组 k 路组关联映射方法。每一路有 v 行
- 主存从 $0 \sim v-1$ 块映射到cache的所有 k 路的 v 行
- $v \sim 2v-1$ 块同样映射到cache的所有 k 路的 v 行，如此类推
- 内存中的每一个块都对应cache中的组中的 k 行



VI

- a. How is a 24-bit memory address divided into the tag, line number, and byte number? (2 marks) Please give the analysis and fill the results in the following table.

Tag	<u>Line</u> (or Slot)	Word
↔	↔	↔

11

10

3

1. 主存容量是 2^{24} , 可寻址范围 2^{24} , 所以 $S + W = 24$
2. 块的大小为8 byte, $8 = 2^3$, 所以 $W = 3$
3. 块数 = $2^{24}/2^3 = 2^{21}$, 所以 $S=21$
4. Cache的总行数=1K= 2^{10} , 所以行数为10
5. 标记位为: $21-10=11$



VI

- b. Into what line would bytes with each of the following addresses be stored? (4 marks)

0011 0001 0111 0011 1011 1100

1100 0011 1100 0101 1111 0100

1101 1111 0011 1001 0101 1110

- Please give the analysis and fill the results in the following table.

Address ↴	Line stored in Hex(十六进制) ↴
0011 0001 0111 0011 1011 1100 ↴	10 0111 0111=277H ↴
1100 0011 1100 0101 1111 0100 ↴	00 1011 1110=0BEH ↴
1101 1111 0011 1001 0101 1110 ↴	11 0010 1011=32BH ↴



VI

- 2) Assume that four-way set-associative cache is used with this machine and the number of sets is $4*1K$. How is a 24-bit memory address divided into tag, set number, and byte number? (2 marks)
 - Please give the analysis and fill the results in the following table.

Tag	Set	Word
↙	↙	↙
9	12	3

1. Cache的组数= $4*1K=2^{12}$, 所以cache组数所占bit位为12
2. 标记位为: $21-12=9$



VII

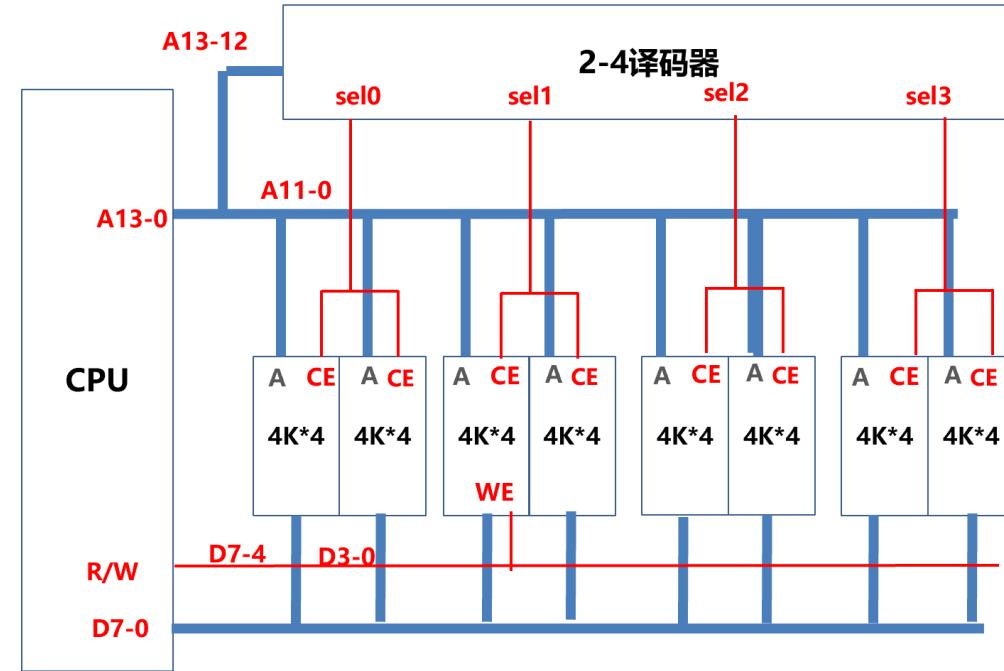
One memory system is built with RAM. Suppose we have memory chips(存储器芯片) as: $4K \times 4$ RAM. Range of RAM is from 0000H to 3FFFH, the rest is reserved. The control signal of RAM is CS#(Chip Select, 片选), The CPU has 16 address lines: A15~A0, 8 data lines: D7~D0. Signal R/W# use for controlling the read/write and MREQ# use for accessing control(访问控制):

1. How many RAM chips are needed?
2. Map each RAM chip with the starting and ending addresses.
3. Draw the decoding circuits(译码电路) for each chip and the connection circuits to the CPU.
4. Please give the total time needed for the refreshes the entire memory(刷新全部内存) (the read cycle is 0.5us).



- 1. RAM地址位0000H to 3FFFH, 也就是
 - 0000 0000 0000 0000~0011 1111 1111 1111
 - 总共14位, 所以内存寻址空间为 $2^{14}=16K$ 。内存有8位数据线, 所以存储单位为byte。
 - 芯片为4K*4bit, 所以总共需要8块。
- 2. 芯片地址。8个芯片分为4组, 每组为总线提供8位数据。
 - RAM1~2: 00 0000 0000 0000~00 1111 1111 1111
 - RAM3~4: 01 0000 0000 0000~01 1111 1111 1111
 - RAM5~6: 10 0000 0000 0000~10 1111 1111 1111
 - RAM7~8: 11 0000 0000 0000~11 1111 1111 1111

- 3. 内存组织图



- 4 刷新时间。4K行，需要 $4K \times 0.5\mu s = 2ms$ 。



VIII

- Consider a single-platter disk with the following parameters:
rotation speed: 3600 rpm; number of tracks on one side of platter: 30,000; number of sectors per track: 600; seek time: 1ms for every hundred tracks traversed. Let the disk receive a request to access a random sector on a random track and assume the disk head starts at track 0.
 - a. What is the average seek time?
 - b. What is the average rotational latency?
 - c. What is the transfer time for a sector?
 - d. What is the total average time to satisfy a request?



VIII

- a. 寻道时间: $29,999/2 = 14999.5 \text{ tracks}$

$$14999.5 / 100 = 149.995 \text{ ms}$$

- b. 旋转延迟: $60 * 1000 / 3600 = 16.666 \text{ ms}$ (磁道访问时间)

$$16.666 / 2 = 8.333 \text{ ms}$$

- c. 扇区传送时间: $16.666 \text{ ms} / 600 = 0.0277 \text{ ms}$

- d. 平均响应时间: $149.995 + 8.333 + 0.0277 = 158 \text{ ms}$



VIII

- Transfer time - T 传送时间T
 - $T = b/rN$
 - b = number of bytes to be transferred 需要传送的字节数
 - N = number of bytes on a track 一个磁道上的字节总数
 - r = rotation speed, in revolutions per second 旋转速度
- The total average access time (including transfer time) 总的平均访问时间，包括传输时间
 - $T_a = T_s + 1/2r + b/rN$ 总的时间=寻道时间+平均旋转延时+传送时间
 - T_s = seek time 寻道时间
 - $1/2r$ is the average Rotational latency 平均旋转延时



VIII

问题：如何组织文件的存储，使得访问时间最短？



VIII

- If the data is stored on the disk completely randomly 如果数据在磁盘上完全随机
 - The read of each sector requires seek time + rotation delay + transmission 每个扇区的读取都需要寻道时间+旋转延迟+传输时间
 - Most of the time is spent in seek track and sector, which is very time-consuming 大部分时间都耗在寻道+寻扇区，非常耗时
- Therefore, data is generally stored in adjacent tracks and sectors in sequence 数据一般都顺序存放在相邻的磁道和扇区
 - Only one seek time and several sector seeking times are required 只需要一次寻道时间和若干次寻扇区的时间
 - How data is organized is important 数据的组织方式很重要！！



- Suppose the page table for the process currently executing on the processor looks like the following. All numbers are decimal, everything is numbered starting from zero, and all addresses are memory byte addresses. The page size is 1024 bytes.

Virtual page number	Valid bit	Reference bit	Modify bit	Page frame number
0	1	1	0	4
1	1	1	1	7
2	0	0	0	—
3	1	0	0	2
4	0	0	0	—
5	1	0	1	0

What physical address, if any, would each of the following virtual addresses correspond to? (Do not try to handle any page faults, if any.)

- 1034
- 3144
- 3899



- $1034 = 1024 + 10$, 映射到页帧7, $7 * 1024 + 10 = 7178$
- $3144 = 3 * 1024 + 72$, 映射到页帧2, $2 * 1024 + 72 = 2120$
- $3899 = 3 * 1024 + 827$, 映射到页帧2, $2 * 1024 + 827 = 2875$

Virtual page number	Valid bit	Reference bit	Modify bit	Page frame number
0	1	1	0	4
1	1	1	1	7
2	0	0	0	—
3	1	0	0	2
4	0	0	0	—
5	1	0	1	0



谢谢大家!

