北京邮电大学 2019 ——2020 学年第 2 学期

《计算机组织与结构》期末考试试题

一． Short Answer Question: (50 marks, 5 for each)

1. What are the main functions of a computer(计算机的主要功能)?
2. What are the main components(组件)of any general-purpose computer?
3. Briefly explain the two basic approaches used to minimize register-memory operations(减少寄存器存储器操作) on RISC machines.
4. What are the typical elements of a machine instruction(机器指令的典型元素是什么)?
5. List and briefly define the registers essential to an instruction execution (列出并简要定义一条指令执行所必需的寄存器) .
6. What basic tasks does a control unit perform(控制单元执行哪些基本任务)?
7. Give a typical list of the inputs and outputs(输入输出列表) of a control unit.
8. What are the differences between the hardwired implementation(硬布线实现方式) and the microprogrammed implementation(微程序实现方式) of a control unit?
9. What is a stored program computer(存储程序式计算机)?
10. From the point of view of computer security, analyze the possible problems of stored program computer (请从计算机安全的角度，分析存储程序式计算机可能带来什么问题)?

四．Analyzing and Calculating(分析与计算) (50 marks)

11. (6 marks)Consider a microprocessor as shown in Figure 1, which has a read synchronous bus timing with an 8-bit external data bus, driven by an 8-MHz processor clock.

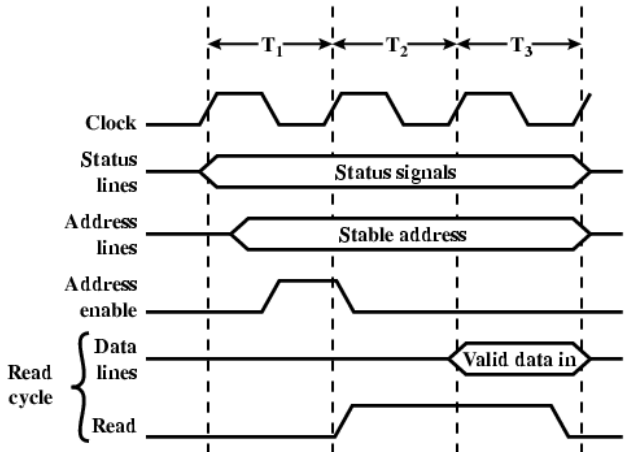

Figure 1

1) What is the maximum data transfer rate(最大数据传输率) in Bytes/s? (2 marks)

2) To increase its performance, would it be better to make its external data bus 16 bits? What is the maximum data transfer rate in Bytes/s now? (2 marks)

3) To increase its performance, would it be better to double the external clock frequency supplied to the microprocessor? What is the maximum data transfer rate in Bytes/s now? (2 marks)

12. (6 marks)For the hexadecimal main memory addresses 222222,777777,DDDDDD, show the following information, in hexadecimal format:

1) Tag, Line, and Word values for a direct-mapped cache, using the format of Figure 2.

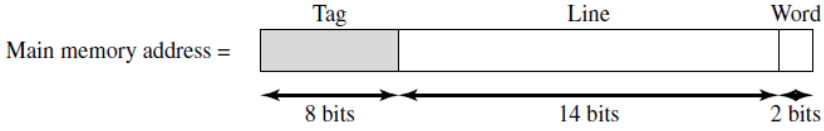

Figure 2

2) Tag and Word values for an associative cache, using the format of Figure 3.

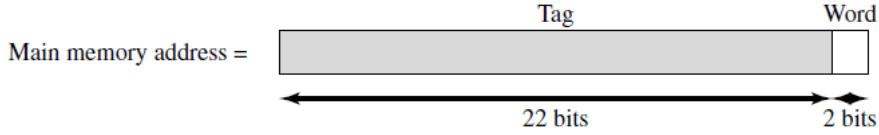

Figure 3

3) Tag, Set, and Word values for a two-way set-associative cache, using the format of Figure 4.

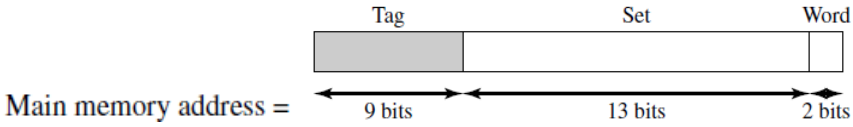

Figure 4

Please write your answers on the answer sheet in the form of Table 1.

Table 1

Address	222222	777777	DDDDDD
1) Tag/Line/Word	/ /	/ /	/ /
2) Tag /Word	/	/	/
3) Tag/Set/Word	/ /	/ /	/ /

13. (6 marks)For the 8-bit word 01111001, the check bits (Hamming Code) are stored with it in memory. Suppose when the word is read from memory, the check bits are calculated to be 1001. Please answer following questions.
    1) What is the true check bits stored with the 8-bit word 01111001？ (3 marks)
    2) What is the data word that was read from memory? (3 marks)

14. (6 marks)Consider a single-platter disk with the following parameters: rotation speed: 3600 rpm; number of tracks on one side of platter: 15,000; number of sectors per track: 600; seek time: one ms for every hundred tracks traversed. Let the disk receive a request to access a random sector on a random track and assume the disk head starts at track 0. Suppose the average seek time is 75 ms.
    1) What is the average rotational latency? (2 marks)
    2) What is the transfer time for a sector? (2 marks)
    3) What is the total average time to satisfy a request? (2 marks)

15. (6 marks)A DMA module is transferring characters to memory using cycle stealing, from a device transmitting at 8000 bps (bits/s). The processor is fetching instructions at the rate of 1 million instructions per second (1 MIPS).
    1) Please explain what the cycle stealing is. (2 marks)
    2) How much will the processor be slowed down due to the DMA activity? (4 marks)

16. (6 marks)Express the following numbers in IEEE 32-bit floating-point format:

1) $(386)_{10}$ 2) $(0.01)_{10}$ 3) $(-0.01)_{10}$

17. (6 marks)A non-pipelined processor has a clock rate of 5 GHz and an average CPI (cycles per instruction) of 6. An upgrade to the processor introduces a six-stage pipeline. However, due to internal pipeline delays, such as latch delay, the clock rate of the new processor has to be reduced to 4 GHz.

1) What is the speedup(加速比) achieved in the new processor for a parallelizable program (可并行程序) of 1 million instructions? (2 marks)

2) What are the MIPS rates for the non-pipelined processor and the pipelined processor? (4 marks)

18. (6 marks)Consider the following assembly language program:

I1: Add R1, 1 /R1 ← (R1) + 1/

I2: Load R2, (R1) /R2 ← Memory (R1)/

I3: Sub R3, 1 /R3 ← (R3) -1/

I4: Move R1, R4 /R1 ← (R4)/

I5: Load R5, (R1) /R5 ← Memory (R1)/

This program includes WAW(写后写), RAW(写后读), and WAR(读后写) dependencies. Show these.

19. (2 marks)An address field in an instruction contains decimal value 15. Where is the corresponding operand located for the direct addressing?