MANIPAL UNIVESITY JAIPUR
School of Computing & IT
IV Semester B. Tech End Semester Examination **MAY 2017**
CS1403 Microprocessors & Microcontrollers
QUESTION PAPER
OPEN BOOK EXAMINATION

Duration: 3hrs **Max Marks: 80**

Note: Answer any **FIVE** full questions & Numbers in [ ] indicates marks.
You are allowed to bring **at most 3 units of bound reference**.
Any missing or misprinted data may be assumed suitably.
All the programs must be readable and properly commented.

Q1. a. What is the advantage of 8086 CPU register for temporary data storage over using a memory location. [2]

b. If the 8086 execution unit calculates an effective address of 15B6H and DS contains 7000H, what physical address will the BIU produce? [2]

c. Why segmentations have been introduced in 8086? Is it possible to create a user defined segment? Explain with example. [4]

d. Describe the role of control flags in 8086 microprocessor. [4]

e. In 8086 pre-fetched instructions are stored in Instruction Byte Queue. When the queue needs to be flushed during the execution of program? Explain with example. [4]

Q2. a. A 10 byte character string is stored with starting memory location 12000H, store the given string in the reverse order at memory location starting with 15000H using string instructions. [8]

b. Write a program using procedure to find second minimum element in the given array of 8 bytes. [8]

Q3. a. Consider series of interrupt as INTR A, INTR B, DIVIDE_BY_ZERO, NMI, INTR C, these interrupt occur one by one but before completion their ISR execution. Explain the sequence in which they will complete their ISR execution. [6]

b. Describe the use of the CAS0, CAS1 and CAS2 lines in this arrangement with a cascaded 8259A & show the arrangements to enable 22 external devices to interrupt 8086 microprocessor at INTR pin with minimum hardware usages. [10]

Q4. a. For the following configuration of 8255 PPI, what control signal should be sent by 8086 for given scenarios: [8]
Port A- Input,
Port B- Output
Port C- Input
CWR- Output

b. Consider the following situation [4]

Data Segment

A dw 1111h, 1122h, 2233h 4433h,.....100 words

Data Ends

Suppose a procedure traverse the array. And the offset of A is odd. Explain how many times the memory read cycle will run. How we can get significant reduction in the number of read cycle?

c. Explain, when Macros are preferred over procedures and vice-versa. [4]

Q5. a. How processor can get the physical address of ISR while executing INT n? Justify your answer. [4]

b. Consider a stack whose base address if 25000h and size of the stack is 500 words than what is the initial values of Stack Segment register and Stack Pointer Register. [4]

c. Write a program to implement multiplication using shift and addition instruction of 8086. (Note: The MUL instruction is not supposed to be used.) [8]

Q6. a. What are the various major 8-bit microcontrollers & what criteria do designers consider in choosing them. [4]

b. Consider two modules of assembly language program named as A.asm and B.asm, where A.asm has a segments SEG_1 which contains proc_1 and B.asm has a segment SEG_2 which contains procedure proc_2. Explain the proper arrangements required to enable proc_1 to call proc_2. [8]

c. Consider an 8-bit number stored in AL=0101 1100. Performed the following tasks with single instruction: [4]

i. Clear 0th and 1st bits.
ii. Invert the 2nd, 5th, 7th bit.
iii. Find out whether 2nd, 3rd, 4th bits are 1, 1, 1 respectively without affecting the contents of AL.
iv. Send the AL value to output device at port number 84H.